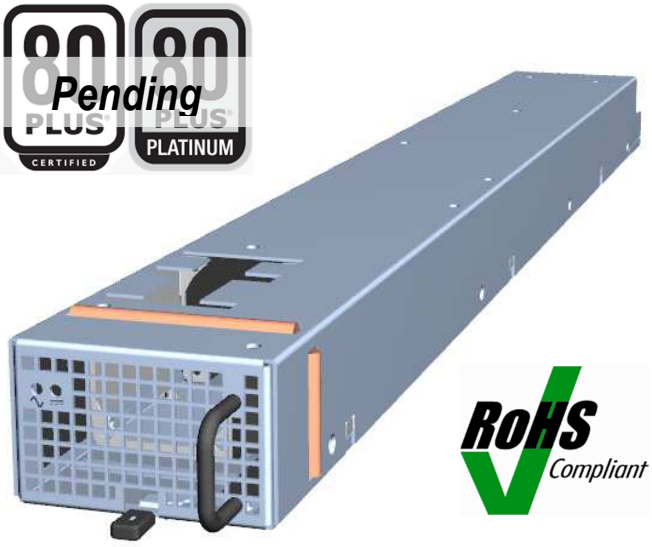
PFE3000-12-069RA Data Sheet

3000 Watts, 12 VDC Output



Features

- Best-in-class, 80 PLUS certified "Platinum" efficiency (pending)
- AC input voltage range: 180-300 VAC
- AC input with power factor correction
- DC input voltage range: 192-400 VDC
- Hot-plug capable
- Parallel operation with active analog current sharing
- Full digital controls for improved performance
- High density design: 30.5 W/in^3
- Small form factor: 69 x 42 x 555 mm
- I^{2}C communication interface for control, programming and monitoring with PMBus™ protocol
- Overtemperature, output overvoltage and overcurrent protection
- 2k Bytes of EEPROM for user information
- 2 Status LEDs: AC OK and DC OK with fault signaling
- Safety-approved to IEC/EN 60950-1 and UL/CSA 60950-1 2nd Ed. (pending)

Applications

- High performance servers, routers and switches.

Description

The PFE3000-12-069RA is a 3000 Watt AC/DC power-factor-corrected (PFC) and DC/DC power supply that converts standard AC mains power or high voltage DC bus voltages into a main output of 12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches. The PFE3000-12-069RA meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

Content

1 ORDERING INFORMATION

PFE	3000	-	12	-	069	R	A	
Product Family PFE Front-Ends	**Power Level** 3000W	**Dash**	**V1 Output** 12V	**Dash**	**Width** 69mm	**Airflow** R: reversed[1)]	**Input** A: AC	

1) front to rear

2 OVERVIEW

The PFE3000-12-069RA AC/DC-DC power supply is a fully DSP controlled, highly efficient front-end. It incorporates resonance-soft-switching technology and interleaved power trains to reduce component stresses, providing increased system reliability and very high efficiency. With a wide input operating voltage range and minimal linear derating of output power with respect to ambient temperature, the PFE3000-12-069RA maximizes power availability in demanding server, switch, and router applications. The front-end is fan cooled and ideally suited for server integration with a matching airflow path.

The PFC stage is digitally controlled using a state-of-the-art digital signal processing algorithm to guarantee best efficiency and unity power factor over a wide operating range.

The DC-DC stage uses soft switching resonant techniques in conjunction with synchronous rectification. An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems.

The always-on +12V standby output provides power to external power distribution and management controllers. Its protection with an active OR-ing device provides for maximum reliability.

Status information is provided with front-panel LEDs. In addition, the power supply can be controlled and the fan speed set via the I²C bus. It allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures.

Cooling is managed by a fan, controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I²C bus.

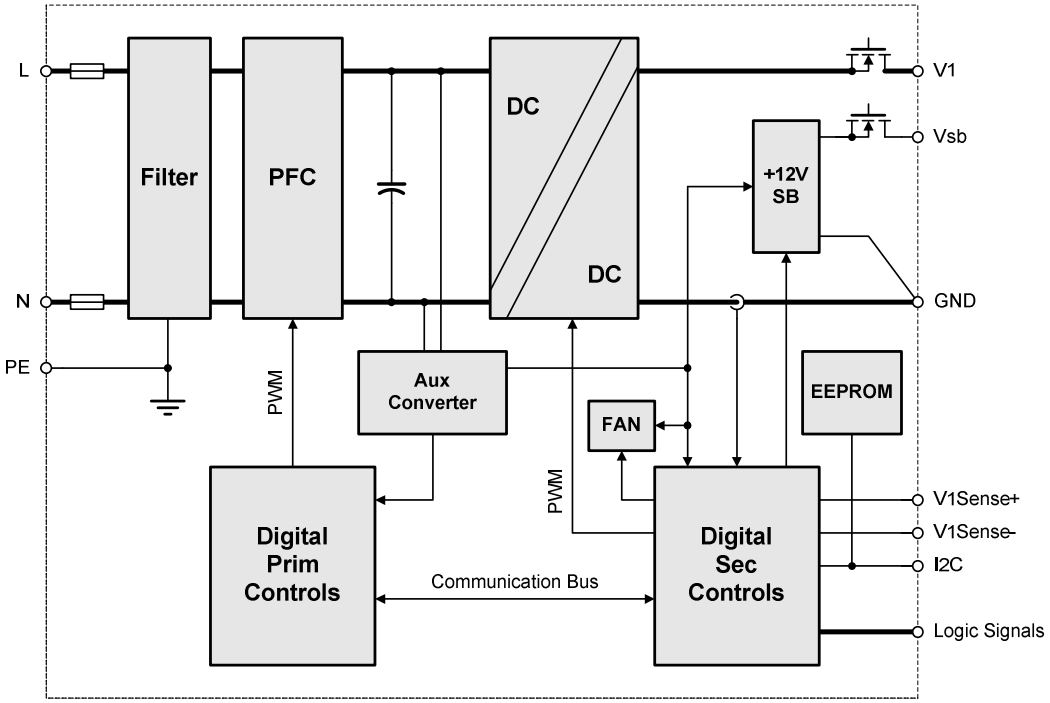


Figure 1: PFE3000-12-0069RA Block Diagram

3 ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

Parameter		Conditions / Description	Min	Nom	Max	Unit
$V_{i\,maxc}$	Max continuous input	Continuous			300	VAC

4 ENVIRONMENTAL AND MECHANICAL

Parameter		Conditions / Description	Min	Nom	Max	Unit
T_A	Ambient temperature	$V_{i\,min}$ to $V_{i\,max}$, $I_{1\,nom}$, $I_{SB\,nom}$	0		+45	°C
T_{Aext}	Extended temp range	Derated output (see Figure 20 and)	+45		+55	°C
T_S	Storage temperature	Non-operational	-20		+70	°C
N_a	Audible noise	$V_{i\,nom}$, 50% $I_{o\,nom}$, T_A = 25°C		53		dBA
	Dimensions	Width		69		mm
		Height		42		mm
		Depth		555		mm
M	Weight			2.60		kg

5 INPUT SPECIFICATIONS

General Condition: T_A = 0… 45 °C unless otherwise noted.

Parameter		Conditions / Description	Min	Nom	Max	Unit
$V_{i\,nom}$	AC Nominal input voltage		200	230	277	VAC
V_i	AC Input voltage ranges	Normal operating ($V_{i\,min}$ to $V_{i\,max}$)	180		300	VAC
$V_{i\,nomDC}$	DC Nominal input voltage		240		380	VDC
V_{iDC}	DC Input voltage ranges	Normal operating ($V_{i\,min}$ to $V_{i\,max}$)	192		400	VDC
$I_{i\,max}$	Max input current	V_i > 200 VAC			16	A_{rms}
$I_{i\,p}$	Inrush Current Limitation	$V_{i\,min}$ to $V_{i\,max}$, 0 °, T_{NTC} = 25 °C (see Figure 5)			50	A_{pk}
F_i	Input frequency		47	50/60	63	Hz
PF	Power Factor	$V_{i\,nom}$, 50 Hz, > 0.3 $I_{1\,nom}$	0.96			W/VA
$V_{i\,on}$	Turn-on input voltage	Ramping up		175		VAC
$V_{i\,off}$	Turn-off input voltage	Ramping down		160		VAC
η	Efficiency without fan	$V_{i\,nom}$, 0.1·$I_{x\,nom}$, $V_{x\,nom}$, T_A = 25 °C	90.0	91.85		%
		$V_{i\,nom}$, 0.2·$I_{x\,nom}$, $V_{x\,nom}$, T_A = 25 °C	93.0	94.40		
		$V_{i\,nom}$, 0.5·$I_{x\,nom}$, $V_{x\,nom}$, T_A = 25 °C	94.5	94.95		
		$V_{i\,nom}$, $I_{x\,nom}$, $V_{x\,nom}$, T_A = 25 °C	93.0	93.75		
T_{hold}	Hold-up Time	After last AC zero point, V_1 > 10.8 V, V_{SB} within regulation, V_i = 230 VAC, $P_{x\,nom}$	12			ms

5.1 INPUT FUSE

Quick-acting 25 A input fuses (6.3 × 32 mm) in series with both the L- and N-line inside the power supply protect against severe defects. The fuses are not accessible from the outside and are therefore not serviceable parts.

5.2 INRUSH CURRENT

The AC-DC power supply exhibits an X-capacitance of only 4.3 µF, resulting in a low and short peak current, when the supply is connected to the mains. The internal bulk capacitor will be charged through an NTC which will limit the inrush current.

Note: Do not repeat plug-in / out operations within a short time, or else the internal in-rush current limiting device (NTC) may not sufficiently cool down and excessive inrush current or component failure(s) may result.

5.3 INPUT UNDER-VOLTAGE

If the RMS value of input voltage (either AC or DC) stays below the input undervoltage lockout threshold $V_{i\,on}$, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

5.4 POWER FACTOR CORRECTION

Power factor correction (PFC) is achieved by controlling the input current waveform synchronously with the input voltage. A fully digital controller is implemented giving outstanding PFC results over a wide input voltage and load ranges. The input current will follow the shape of the input voltage. If for instance the input voltage has a trapezoidal waveform, then the current will also show a trapezoidal waveform. At DC input voltage the PFC is still in operation, but the input current will be DC in this case.

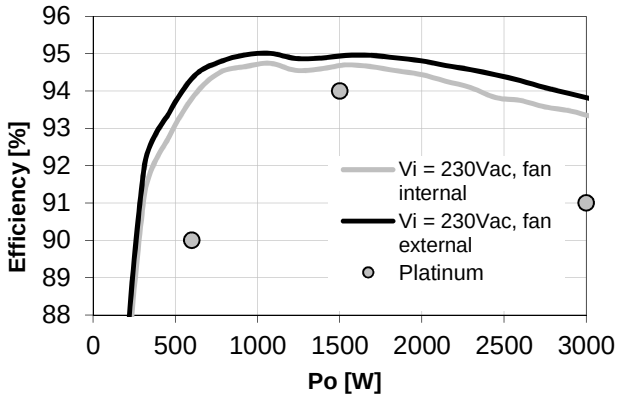


Figure 2: AC Efficiency vs. load current (ratio metric loading)

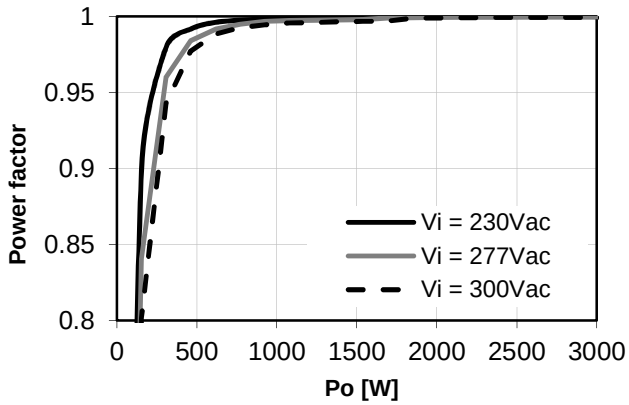


Figure 3: Power factor vs. load current

To be updated

Figure 4: DC Efficiency vs. load current (ratio metric loading)

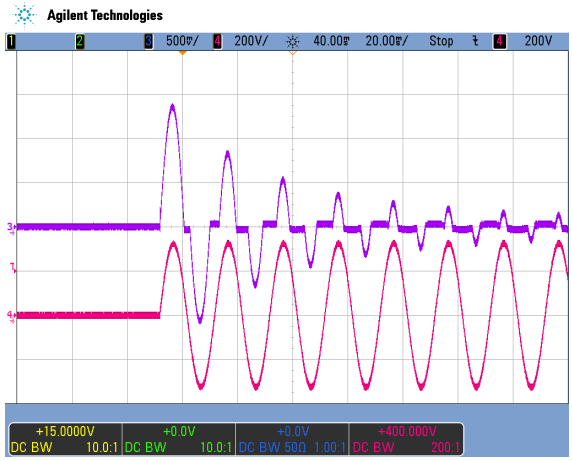


Figure 5: Inrush current, V_{in} = 230Vac, 0°phase angle
CH4: V_{in} (200V/div), CH3: I_{in} (10A/div)

5.5 EFFICIENCY

The high efficiency (see Figure 2) is achieved by using state-of-the-art silicon power devices in conjunction with soft-transition topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The rpm of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions.

Figure 4 shows efficiency when input voltage is supplied from a high voltage DC source.

6 OUTPUT SPECIFICATIONS

General Condition: T_a = 0 … +45 °C unless otherwise noted.

Parameter		Conditions / Description	Min	Nom	Max	Unit
***Main Output* V_1**						
$V_{1\ nom}$	Nominal output voltage	0.5 ·$I_{1\ nom}$, T_{amb} = 25 °C		12.3		VDC
$V_{1\ set}$	Output setpoint accuracy		-0.5		+0.5	% $V_{1\ nom}$
d$V_{1\ tot}$	Total regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$, $T_{a\ min\ to}$ $T_{a\ max}$	-1		+1	% $V_{1\ nom}$
$P_{1\ nom}$	Nominal output power	V_1 = 12.3 VDC		3000		W
$I_{1\ nom}$	Nominal output current	V_1 = 12.3 VDC		244		ADC
$I_{V1\ ol}$	Short time over load current	V_1 = 12.3 VDC, $T_{a\ min\ to}$ $T_{a\ max}$, maximum duration 20ms (see chapter 6.2)			292	A
$v_{1\ pp}$	Output ripple voltage	$V_{1\ nom}$, $I_{1\ nom}$, 20 MHz BW (See chapter 6.1)			160	mVpp
d$V_{1\ Load}$	Load regulation	V_i = $V_{i\ nom}$, 0 - 100 % $I_{1\ nom}$		170		mV
d$V_{1\ Line}$	Line regulation	V_i =$V_{i\ min}$... $V_{i\ max}$		0		mV
$I_{1\ max}$	Current limitation	T_a < 45 °C T_a = 55 °C 2)	248 186		274 212	ADC
dI_{share}	Current sharing	Deviation from $I_{1\ tot}$ / N, I_1 > 25% $I_{1\ nom}$	-5%		+5%	A
dV_{dyn}	Dynamic load regulation	ΔI_1 = 50% $I_{1\ nom}$, I_1 = 5 … 100% $I_{1\ nom}$, dI_1/dt = 1 A/µs, recovery within 1% of $V_{1\ nom}$	-0.6		0.6	V
T_{rec}	Recovery time				0.5	ms
$t_{AC\ V1}$	Start-up time from AC	V_1 = 10.8 VDC (see Figure 23)			3	sec
$t_{V1\ rise}$	Rise time	V_1 = 10…90% $V_{1\ nom}$ (see Figure 23)		2.5		ms
C_{Load}	Capacitive loading	T_a = 25 °C			30000	µF

2) see Figure 20 for linear derating > 45°C

Parameter		Conditions / Description	Min	Nom	Max	Unit
***Standby Output* V_{SB}**						
$V_{SB\ nom}$	Nominal output voltage	0.5 ·$I_{SB\ nom}$, T_{amb} = 25 °C		12		VDC
$V_{SB\ set}$	Output setpoint accuracy		-0.5		+0.5	% V_{SBnom}
d$V_{SB\ tot}$	Total regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, $T_{a\ min\ to}$ $T_{a\ max}$	-1		+1	% V_{SBnom}
$P_{SB\ nom}$	Nominal output power	V_{SB} = 12 VDC		60		W
$I_{SB\ nom}$	Nominal output current	V_{SB} = 12 VDC		5		ADC

Parameter		Conditions / Description	Min	Nom	Max	Unit
Standby Output V_{SB} (cont.)						
$v_{SB\ pp}$	Output ripple voltage	$V_{SB\ nom}$, $I_{SB\ nom}$, 20 MHz BW (See chapter 6.1)			120	mVpp
dV_{SB}	Droop	0 - 100 % $I_{SB\ nom}$		200		mV
$I_{SB\ max}$	Current limitation		6		9	ADC
dV_{SBdyn}	Dynamic load regulation	ΔI_{SB} = 50% $I_{SB\ nom}$, I_{SB} = 5 … 100% $I_{SB\ nom}$, dI_{SB}/dt = 1 A/µs, recovery within 1% of $V_{SB\ nom}$	-0.6		0.6	V_{SBnom}
T_{rec}	Recovery time				0.5	ms
$t_{AC\ VSB}$	Start-up time from AC	V_{SB} = 90% $V_{SB\ nom}$ (see Figure 23)			2	sec
$t_{VSB\ rise}$	Rise time	V_{SB} = 10…90% $V_{SB\ nom}$ (see Figure 23)		10		ms
C_{Load}	Capacitive loading	T_{amb} = 25 °C			3000	µF

6.1 OUTPUT VOLTAGE RIPPLE

The internal output capacitance at the power supply output (behind OR-ing element) is minimized to prevent disturbances during hot plug. In order to provide low output ripple voltage in the application, external capacitors should be added close to the power supply output.

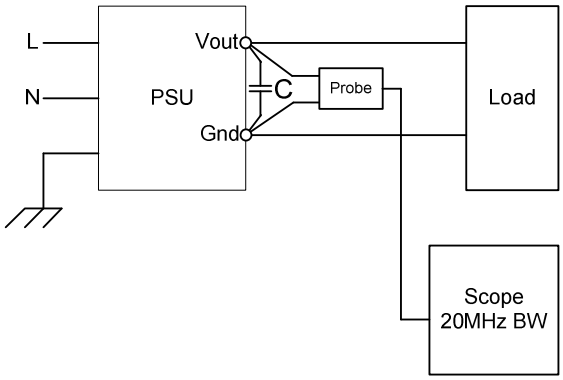


Figure 6: Output ripple test setup

The setup of Figure 6 has been used to evaluate suitable capacitor types. The capacitor combinations of Table 1 and Table 2 should be used to reduce the output ripple voltage.

The ripple voltage is measured with 20 MHz BWL, close to the external capacitors.

Note: Care must be taken when using ceramic capacitors with a total capacitance of 1 µF to 50 µF on output V1, due to their high quality factor the output ripple voltage may be increased in certain frequency ranges due to resonance effects.

Table 1: Suitable capacitors for V_1

External capacitor V1	dV_1max	Unit
2Pcs 47 µF/16 V/X5R/1210	150	mVpp
1Pcs 1000 µF/16 V/Low ESR Aluminum/ø10x20	150	mVpp
1Pcs 270 µF/16 V/Conductive Polymer/ø8x12	150	mVpp
2Pcs 47 µF/16V/X5R/1210 plus 1Pcs 270 µF Conductive Polymer OR 1Pcs 1000 µF Low ESR AlCap	90	mVpp

The output ripple voltage on VSB is influenced by the main output V1. Evaluating VSB output ripple must be done when maximum load is applied to V1.

Table 2: Suitable capacitors for V_{SB}

External capacitor VSB	dV_{SB}max	Unit
1Pcs 10 µF/16 V/X7R/1206	80	mVpp

6.2 SHORT TIME OVERLOAD

The main output has a capability to allow load current to reach 120% of the nominal output current rating for a maximum duration of 20ms. This allows the system to consume extended power for short time dynamic processes.

6.3 OUTPUT ISOLATION

Main and standby output and all signals are isolated from the chassis and protective earth connection, although the applied voltage must not exceed 100Vpeak to prevent any damage of the supply.

Internal to the supply the main output ground, standby output ground and signal ground are interconnected through 10ohm resistors to prevent any circulating current within the supply. In order to prevent any potential difference in outputs or signals within the application these 3 grounds must be directly interconnected at system level. See also section 14 for pins to be interconnected.

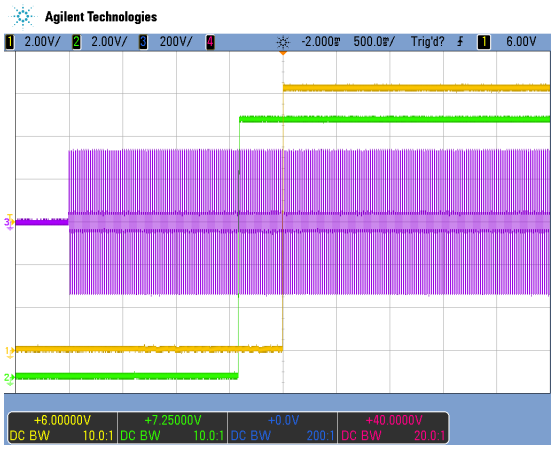


Figure 7: Turn-On AC Line 230 VAC, full load (500 ms/div)
CH1: V_1 (2 V/div); CH2: V_{SB} (2 V/div); CH3: Vin (200 V/div)

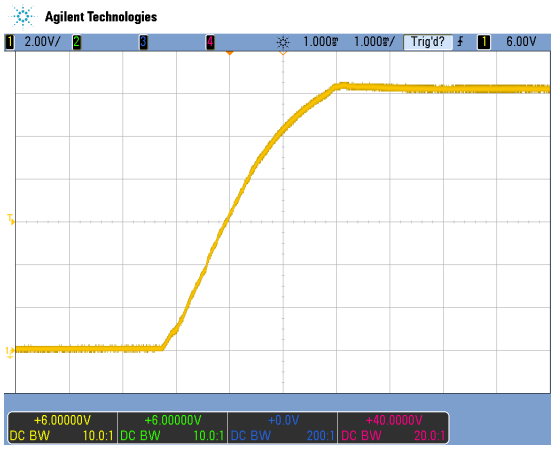


Figure 8: Turn-On AC Line 230 VAC, full load (1 ms/div)
CH1: V_1 (2 V/div)

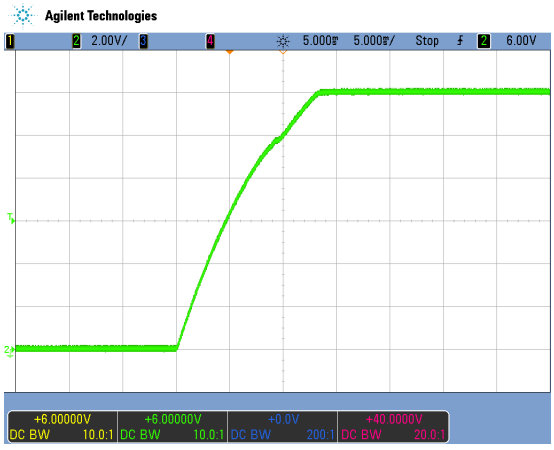


Figure 9: Turn-On AC Line 230 VAC, full load (5 ms/div)
CH2: V_{SB} (2 V/div)

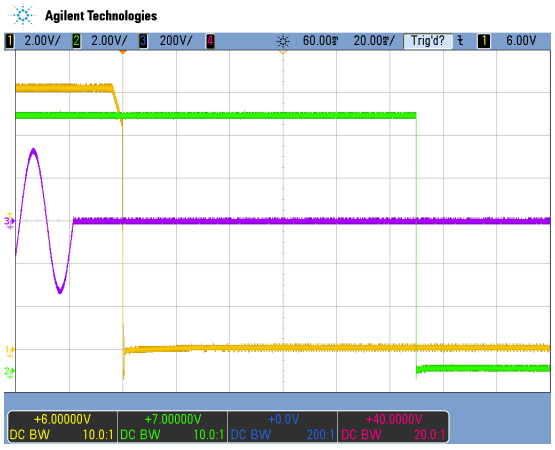


Figure 10: Turn-Off AC Line 230 VAC, full load (20 ms/div)
CH1: V_1 (2 V/div); CH2: V_{SB} (2 V/div); CH3: Vin (200 V/div)

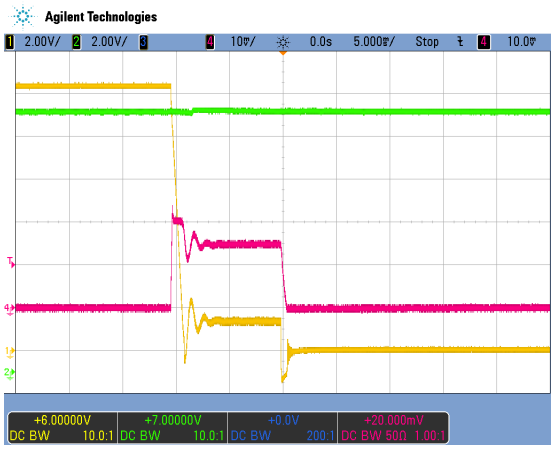


Figure 11: Short circuit on V1 (5 ms/div)
CH1: V_1 (2 V/div); CH2: V_{SB} (2 V/div); CH4: I_1 (200 A/div)

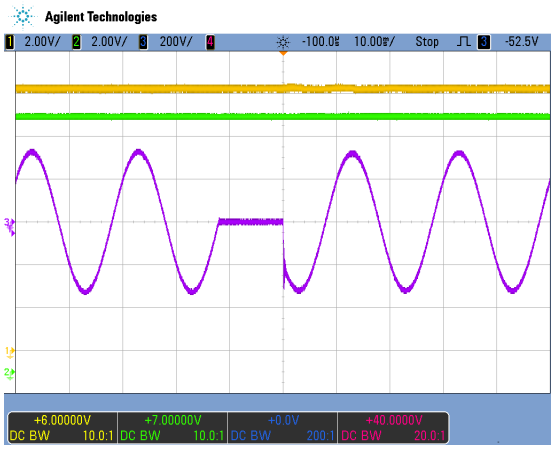


Figure 12: AC drop out 12 ms, full load (10 ms/div)
CH1: V_1 (2 V/div) ; CH2: V_{SB} (2 V/div); CH3: V_{in} (200 V/div)

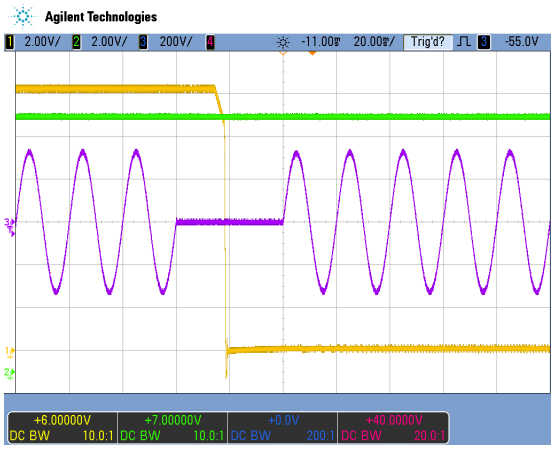


Figure 13: AC drop out 40 ms, full load (20 ms/div)
CH1: V_1 (2 V/div); CH2: V_{SB} (2 V/div); CH3: V_{in} (200 V/div)

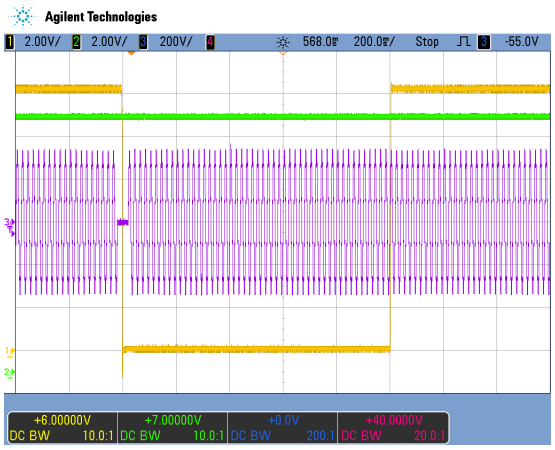


Figure 14: AC drop out 40 ms, full load (200 ms/div), V_1 restart after 1 sec
CH1: V_1 (5 V/div); CH2: V_{SB} (2 V/div); CH3: I_1 (200 V/div)

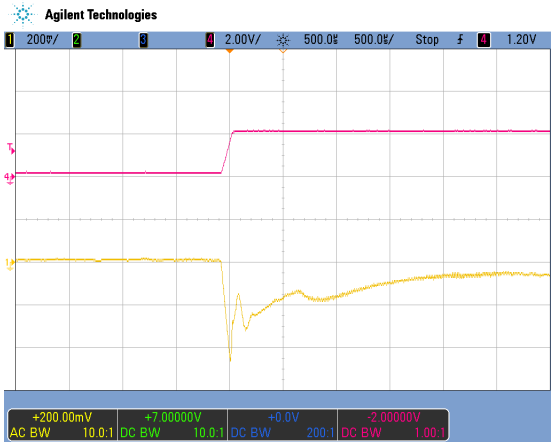


Figure 15: Load transient V_1, 3 to 125 A (500 µs/div)
CH1: V_1 (200 mV/div); CH4: I_1 (100 A/div)

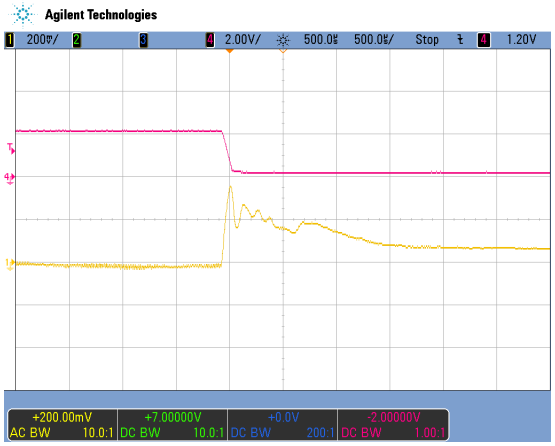


Figure 16: Load transient V_1, 125 to 3 A (500 µs/div)
CH1: V_1 (200 mV/div); CH4: I_1 (100 A/div)

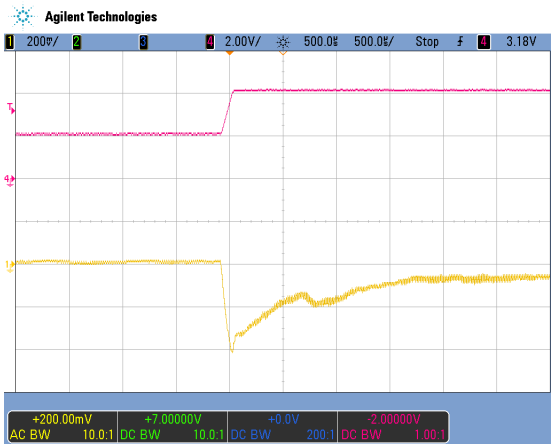


Figure 17: Load transient V_1, 122 to 244 A (500 µs/div)
CH1: V_1 (200 mV/div); CH4: I_1 (100 A/div)

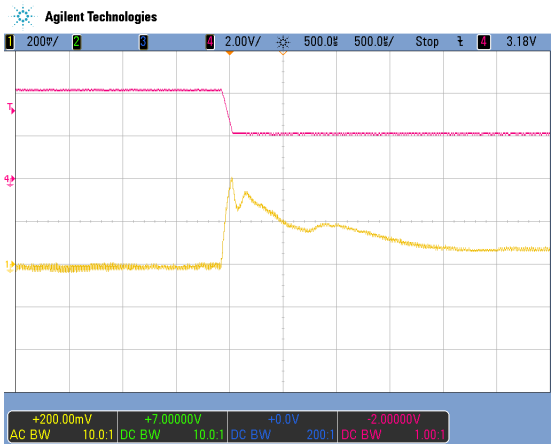


Figure 18: Load transient V_1, 244 to 122 A (500 µs/div)
CH1: V_1 (200 mV/div); CH4: I_1 (100 A/div)

7 PROTECTION

Parameter		Conditions / Description	Min	Nom	Max	Unit
F	Input fuses (L+N)	Not user accessible, quick-acting (F)		25		A
$V_{1\ OV}$	OV threshold V_1		13.6	14.2	14.8	VDC
$t_{OV}V_1$	OV latch off time V_1				1	ms
$V_{SB\ OV}$	OV threshold V_{SB}		13.3	13.9	14.5	VDC
$t_{OV}V_{SB}$	OV latch off time V_{SB}				1	ms
$I_{V1\ lim}$	Current limitation V_1	T_a < 45 °C T_a = 55 °C 2)	248 186		274 212	A
$t_{V1\ lim}$	Current limit blanking time	Time to latch off when in over current	20	22	24	A
$I_{V1\ ol\ lim}$	Current limit during short time overload V_1	Maximum duration 20ms	292	300	308	A
$I_{V1\ SC}$	Max short circuit current V_1	V_1 < 3 V			350 3)	A
$t_{V1\ SC\ off}$	Short circuit latch off time	Time to latch off when in short circuit		10		ms
$I_{VSB\ lim}$	Current limitation V_{SB}		6		9	A
$t_{VSB\ lim}$	Current limit blanking time	Time to hit hiccup when in over current			1	ms
T_{SD}	Over temperature on critical points	Inlet Ambient Temperature PFC Primary Heatsink Temperature Secondary Sync Mosfet Temperature Secondary OR-ing Mosfet Temperature			60 80 115 125	°C

2) see Figure 20 for linear derating > 45°C
3) limit set don't include effects of main output capacitive discharge.

7.1 AUTOMATIC RETRY

For all fault conditions except current limitation on Standby output, the supply will shut down for 10sec and restart automatically. The supply will restart from a fault up to 5 times, after that it will latch off. The latch and restart counter can be cleared by disconnecting the input voltage or by toggling the PSON_L input. A failure on one output will only shut down this output, while the other one will continue to operate.

7.2 OVERVOLTAGE PROTECTION

The PFE front-ends provide a fixed threshold overvoltage (OV) protection implemented with a HW comparator. Once an OV condition has been triggered, the supply will shut down and latch the fault condition.

7.3 UNDERVOLTAGE DETECTION

Both main and standby outputs are monitored. LED and PWOK_L pin signal if the output voltage exceeds ±7% of its nominal voltage.

Output undervoltage protection is provided on both outputs. When either V_1 or V_{SB} falls below 93% of its nominal voltage, the output is inhibited.

7.4 CURRENT LIMITATION

Main Output: Two different over current protection features are implemented on the main output.

A static over current protection will shut down the output, if the output current does exceed $I_{V1\ lim}$ for more than 20ms. If the output current is increased slowly this protection will shut down the supply.

The main output current limitation level I_{V1lim} will decrease if the ambient (inlet) temperature increases beyond 45 °C (see Figure 20). Note that the actual current limitation on V1 will kick in at a current level approximately 20A higher than what is shown in Figure 20 (see also chapter 10 for additional information).

The 2nd protection is a substantially rectangular output characteristic controlled by a software feedback loop. This protects the power supply and system during the 20ms blanking time of the static over current protection. If the

output current is rising fast and reaches $I_{V1\ ol\ lim}$, the supply will immediately reduce its output voltage to prevent the output current from exceeding $I_{V1\ ol\ lim}$. When the output current is reduced below $I_{V1\ ol\ lim}$, the output voltage will return to its nominal value.

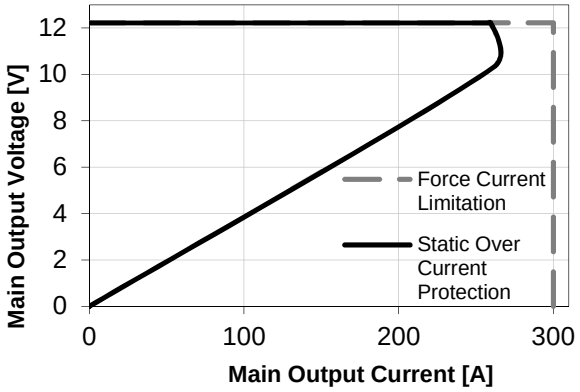


Figure 19: Current limitation on V_1

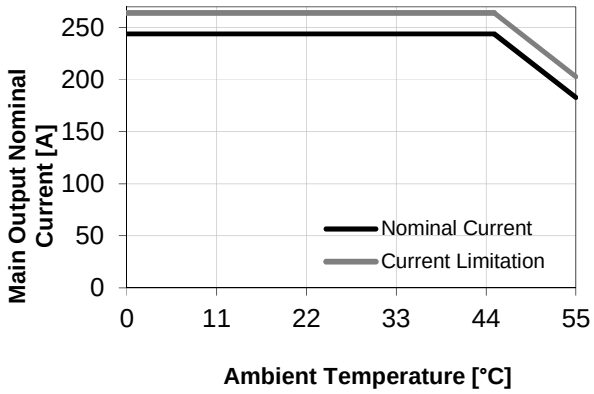


Figure 20: Derating on V_1 vs. T_a

Standby Output: On the standby output a hiccup type over current protection is implemented. This protection will shut down the standby output immediately when standby current reaches or exceeds $I_{VSB\ lim}$. After an off-time of 1s the output automatically tries to restart. If the overload condition is removed the output voltage will reach again its nominal value. At continuous overload condition the output will repeatedly trying to restart with 1s intervals

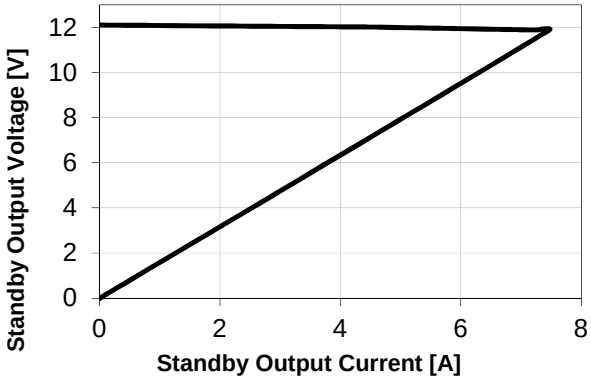


Figure 21: Current limitation on V_{SB}

8 MONITORING

See chapter 9.11 to 9.15 and PFE3000-12-069RA PMBus Communication Manual BCA.00040 for further information on communication interface.

Parameter		Conditions / Description	Min	Nom	Max	Unit
$V_{i\ mon}$	Input RMS voltage	$V_{i\ min} \le V_i \le V_{i\ max}$	-2.5		+2.5	%
$I_{i\ mon}$	Input RMS current	$I_i > 4\ A_{rms}$	-5		+5	%
		$I_i \le 4\ A_{rms}$	-0.2		+0.2	A_{rms}
$P_{i\ mon}$	True input power	$P_i > 700$ W	-5		+5	%
		$P_i \le 700$ W	-35		+35	W
$V_{1\ mon}$	V_1 voltage		-2		+2	%
$I_{1\ mon}$	V_1 current	I1 > 30 A	-2		+2	%
		I1 ≤ 30 A	-0.6		+0.6	A
$P_{o\ nom}$	Total output power	Po > 200 W	-5		+5	%
		Po ≤ 200 W	-10		+10	W
$V_{SB\ mon}$	Standby voltage		-2		+2	%
$I_{SB\ mon}$	Standby current	$I_{SB} \le I_{SB\ nom}$	-0.2		+0.2	A

9 SIGNALING AND CONTROL

9.1 ELECTRICAL CHARACTERISTICS

Parameter		Conditions	Min	Nom	Max	Unit
PSKILL / PSON_L inputs						
V_{IL}	Input low level voltage		-0.2		0.8	V
V_{IH}	Input high level voltage		2.0		3.6	V
$I_{IL,\ H}$	Maximum input sink or source current		0		1	mA
$R_{puPSKILL}$	Internal pull up resistor on PSKILL			10		kΩ
R_{puPSON_L}	Internal pull up resistor on PSON_L			10		kΩ
PWOK_L output						
V_{OL}	Output low level voltage	I_{sink} < 4 mA	-0.2		0.4	V
V_{puPWOK_L}	External pull up voltage				12	V
R_{puPWOK_L}	Recommended external pull up resistor on PWOK_L at V_{puPWOK_L} = 3.3V			10		kΩ
Low level output	All outputs are turned on and within regulation					
High level output	In standby mode or V_1/V_{SB} have triggered a fault condition					
INOK_L output						
V_{OL}	Output low level voltage	I_{sink} < 4 mA	-0.2		0.4	V
V_{puINOK_L}	External pull up voltage				12	V
R_{puINOK_L}	Recommended external pull up resistor on INOK_L at V_{puINOK_L}= 3.3V			10		kΩ
Low level output	Input voltage is within range for PSU to operate					
High level output	Input voltage is not within range for PSU to operate					

SMB_ALERT_L output						
V_{OL}	Output low level voltage	I_{sink} < 4 mA	-0.2		0.4	V
$V_{puSMB\_ALERT\_L}$	External pull up voltage				12	V
$R_{puSMB\_ALERT\_L}$	Recommended external pull up resistor on SMB_ALERT_L at $V_{puSMB\_ALERT\_L}$= 3.3V			10		kΩ
Low level output	PSU in warning or failure condition					
High level output	PSU is ok					

9.2 INTERFACING WITH SIGNALS

A 15V zener diode is added on all signal pins versus signal ground SGND to protect internal circuits from negative and high positive voltage. Signal pins of several supplies running in parallel can be interconnected directly. A supply having no input power will not affect the signals of the paralleled supplies.

ISHARE pins must be interconnected without any additional components. This in-/output also has a 15 V zener diode as a protection device and is disconnected from internal circuits when the power supply is switched off.

9.3 FRONT LED

The front-end has 2 front LEDs showing the status of the supply. LED number one is green and indicates AC power is on or off, while LED number two is bi-colored: green and yellow, and indicates DC power presence or fault situations. For the position of the LEDs see . Table 3 lists the different LED status.

Table 3: LED Status

Operating Condition	LED Signaling
AC LED	
AC Line within range	Solid Green
AC Line UV condition	Off
DC LED [4]	
PSON_L High	Blinking Yellow (1:1)
V_1 or V_{SB} out of regulation	Solid Yellow
Over temperature shutdown	
Output over voltage shutdown (V_1 or V_{SB})	
Output under voltage shutdown (V_1 or V_{SB})	
Output over current shutdown (V_1 or V_{SB})	
Over temperature warning	Blinking Yellow/Green (2:1)
Minor fan regulation error (>5%, <15%)	Blinking Yellow/Green (1:1)

[4] The order of the criteria in the table corresponds to the testing precedence in the controller.

9.4 PRESENT_L

The PRESENT_L is normally a trailing pin within the connector and will contact only once all other connector contacts are closed. This active-low pin is used to indicate to a power distribution unit controller that a supply is plugged in. The maximum sink current on PRESENT_L pin should not exceed 10 mA.

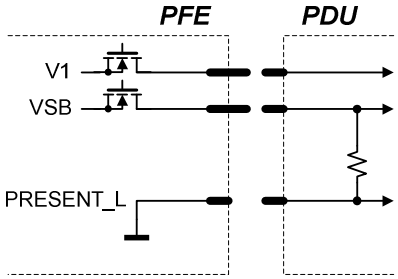


Figure 22: PRESENT_L signal pin

9.5 PSKILL INPUT

The PSKILL input is an active-low and normally a trailing pin in the connector and is used to disconnect the main output as soon as the power supply is being plugged out. This pin should be connected to SGND in the power distribution unit. The standby output will remain on regardless of the PSKILL input state.

9.6 AC TURN-ON / DROP-OUTS / INOK_L

The power supply will automatically turn-on when connected to the AC line under the condition that the PSON_L signal is pulled low and the AC line is within range. The INOK_L is an open collector output that requires an external pull-up to a maximum of 12V indicating whether the input is within the range the power supply can use and turn on. The INOK_L signal is active-low. The timing diagram is shown in Figure 23 and referenced in Table 4.

Table 4: AC Turn-on / Dip Timing

Operating Condition		Min	Max	Unit
$t_{AC\ VSB}$	AC Line to 90% V_{VSB}		2	sec
$t_{AC\ V1}$	AC Line to 90% V_1		3	sec
$t_{INOK\_L\ on1}$	INOK_L signal on delay (start-up)		1800	ms
$t_{INOK\_L\ on2}$	INOK_L signal on delay (dips)	0	100	ms
$t_{V1\ holdup}$	Effective V_1 holdup time	12	200	ms
$t_{VSB\ holdup}$	Effective V_{SB} holdup time	40	200	ms
$t_{INOK\_L\ V1}$	INOK_L to V_1 holdup	7		ms
$t_{INOK\_L\ VSB}$	INOK_L to V_{SB} holdup	27		ms
$t_{V1\ off}$	Minimum V_1 off time	1000	1200	ms
$t_{VSB\ off}$	Minimum V_{SB} off time	1000	1200	ms
$t_{V1dropout}$	Minimum V_1 dropout time	12		ms
$t_{VSBdropout}$	Minimum V_{SB} dropout time	40		ms

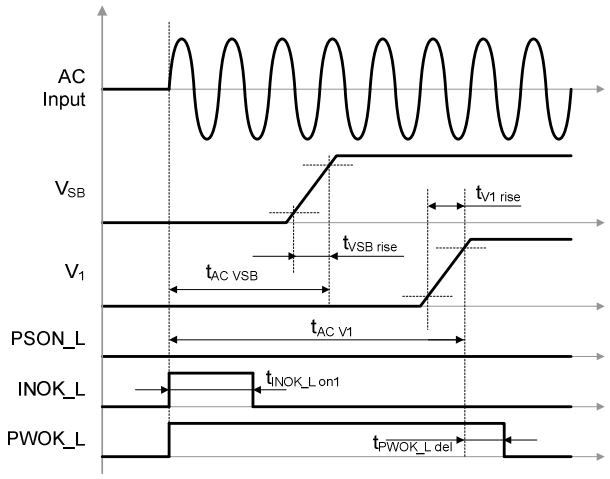


Figure 23: AC turn-on timing

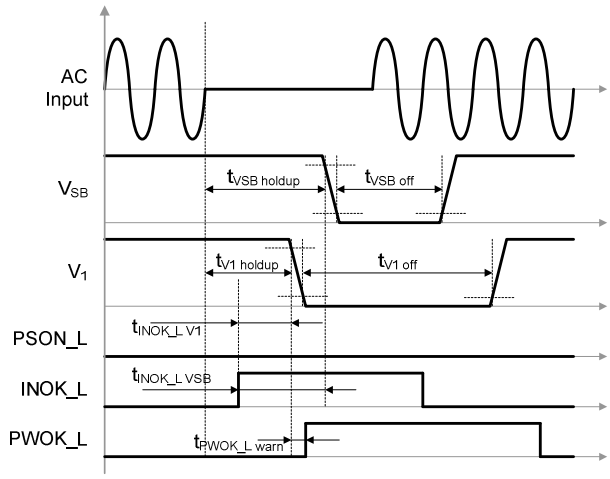


Figure 25: AC long dips

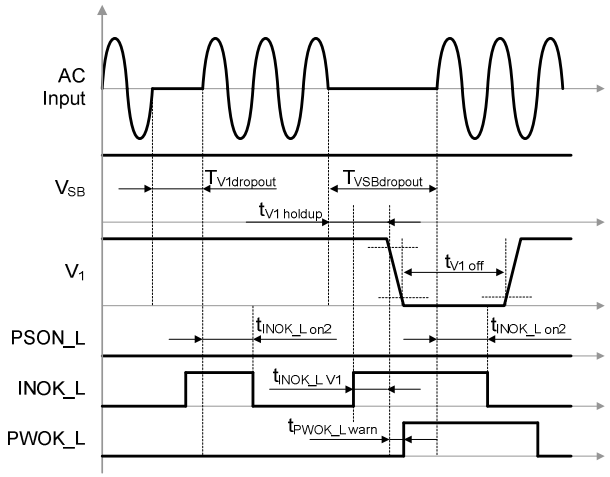


Figure 24: AC short dips

9.7 PSON_L INPUT

The PSON_L is an internally pulled-up (3.3 V) input signal to enable / disable the main output V_1 of the front-end. This active-low pin is also used to clear any latched fault condition. The timing diagram is given in Figure 26 and the parameters in Table 5.

Table 5: PSON_L timing

Operating Condition		Min	Max	Unit
$t_{PSON\_L\ V1on}$	PSON_L to V_1 delay (on)	150	250	ms
$t_{PSON\_L\ V1off}$	PSON_L to V_1 delay (off)	0	100	ms

9.8 PWOK_L SIGNAL

The PWOK_L is an open collector output that requires an external pull-up to a maximum of 12V indicating whether both V_{SB} and V_1 outputs are within regulation. This pin is active-low. The timing diagram is shown in Figure 23/Figure 26 and referenced in the

Table 6.

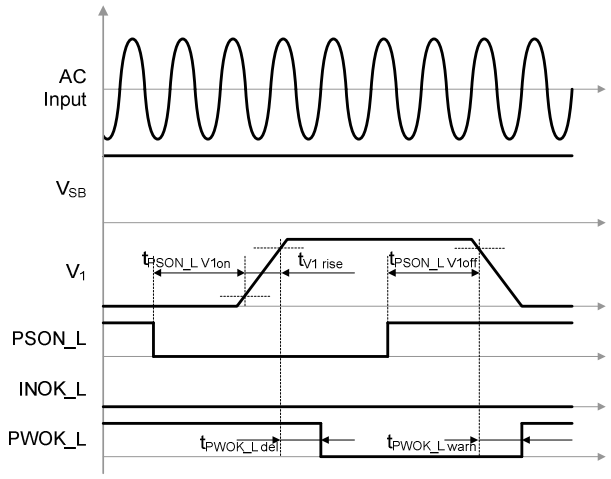


Figure 26: PSON_L turn-on/off timing

Table 6: PWOK_L timing

Operating Condition		Min	Max	Unit
$t_{PWOK\_L\ del}$	PWOK_L to V_1 delay (on)	250	350	ms
$t_{PWOK\_L\ warn}$	PWOK_L to V_1 delay (off) caused by: PSKILL PSON_L, INOK_L, OT, Fan Failure UV and OV on VSB OC on VSB (Software trigger) OC on V1 (Software trigger) OC on V1 (Hardware trigger) UV and OV on V1	0	5	ms

9.9 CURRENT SHARE

The PFE front-ends have an active current share scheme implemented for V_1. All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.

The current share function uses an analog bus. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV.

The standby output uses a passive current share method (droop output voltage characteristic).

9.10 SENSE INPUTS

Main output have sense lines implemented to compensate for voltage drop on load wires. The maximum allowed voltage drop is 200 mV on the positive rail and 100 mV on the PGND rail.

With open sense inputs the main output voltage will rise by 250 mV. Therefore if not used, these inputs should be connected to the power output and PGND close to the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

9.11 I2C / SMBUS COMMUNICATION

The interface driver in the PFE supply is referenced to the SGND. The PFE supply is a communication slave device only; it never initiates messages on the I^2C/SMBus by itself. The communication bus voltage and timing is defined in Table 7 further characterized through:

- There are 100kΩ internal pull-up resistors
- The SDA/SCL IOs must be pull-up externally to 3.3±0.3V
- Pull-up resistor should be 2 – 5kΩ to ensure SMBUS compliant signal rise times
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognizes any time Start/Stop bus conditions

The SMB_ALERT_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events.

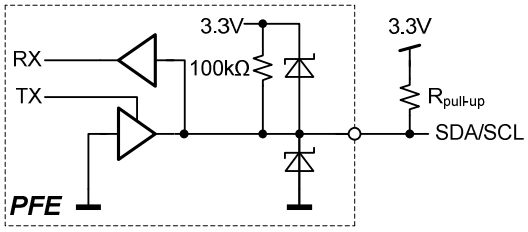


Figure 27: Physical layer of communication interface

Communication to the DSP or the EEPROM will be possible as long as the input AC (DC) voltage is provided. If no AC (DC) is present, communication to the unit is possible as long as it is connected to a live VSB output (provided e.g. by the redundant unit). If only V1 is provided, communication is not possible.

Table 7: I²C / SMBus Specification

Par	Description	Condition	Min	Max	Unit
V_{iL}	Input low voltage		-0.2	0.4	V
V_{iH}	Input high voltage		2.1	3.6	V
V_{hys}	Input hysteresis		0.15		V
V_{oL}	Output low voltage	4 mA sink current	0	0.4	V
t_r	Rise time for SDA and SCL		20+0.1C_b[1]	300	Ns
t_{of}	Output fall time ViHmin → ViLmax	10 pF < C_b[1] < 400 pF	20+0.1C_b[1]	250	Ns
I_i	Input current SCL/SDA	0.1 VDD < Vi < 0.9 VDD	-10	10	µA
C_i	Capacitance for each SCL/SDA			10	pF
f_{SCL}	SCL clock frequency		0	100	kHz
R_{pu}	External pull-up resistor	f_{SCL} ≤ 100 kHz		1000 ns / C_b[1]	Ω
t_{HDSTA}	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	4.0		µs
t_{LOW}	Low period of the SCL clock	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HIGH}	High period of the SCL clock	f_{SCL} ≤ 100 kHz	4.0		µs
t_{SUSTA}	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HDDAT}	Data hold time	f_{SCL} ≤ 100 kHz	0	3.45	µs
t_{SUDAT}	Data setup time	f_{SCL} ≤ 100 kHz	250		ns
t_{SUSTO}	Setup time for STOP condition	f_{SCL} ≤ 100 kHz	4.0		µs
t_{BUF}	Bus free time between STOP and START	f_{SCL} ≤ 100 kHz	4.7		µs
EEPROM_WP					
V_{iL}	Input low voltage		-0.2	0.4	V
V_{iH}	Input high voltage		2.1	3.6	V
I_i	Input sink or source current		-1	1	mA
R_{pu}	Internal pull-up resistor to 3.3V		10k		Ω

[1] Cb = Capacitance of bus line in pF, typically in the range of 10…400 pF

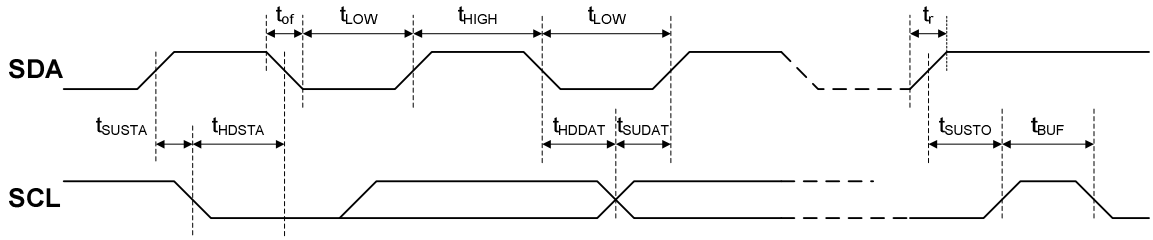


Figure 28: I²C / SMBus Timing

9.12 ADDRESS

The supply supports PMBus communication protocol, address for PMBus communication is at fixed to 0x20. The EEPROM is at fixed address = 0xA0.

9.13 CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I²C bus physical layer (see Figure 29).

In order to write to the EEPROM, the write protection needs to be disabled by setting EEPROM_WP input correctly

The EEPROM provides 2k bytes of user memory. None of the bytes are used for the operation of the power supply.

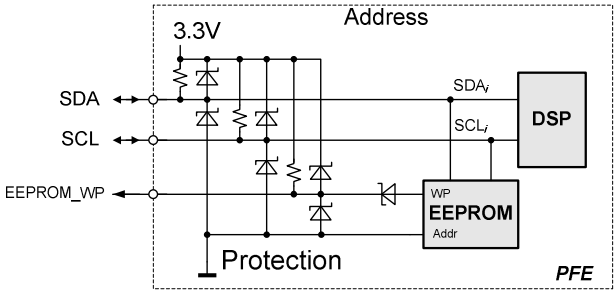


Figure 29: I²C Bus to DSP and EEPROM

9.14 EEPROM PROTOCOL

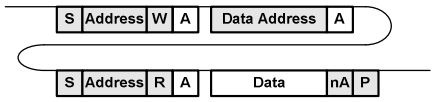
The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.

READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



9.15 PMBus™ PROTOCOL

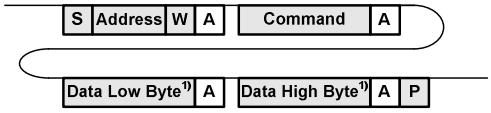
The Power Management Bus (PMBus™) is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at www.powerSIG.org.

PMBus™ command codes are not register addresses. They describe a specific command to be executed. The supply supports the following basic command structures:

- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

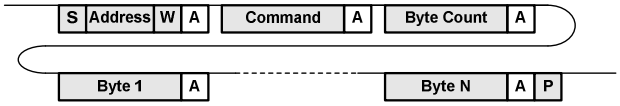
WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



1) Optional

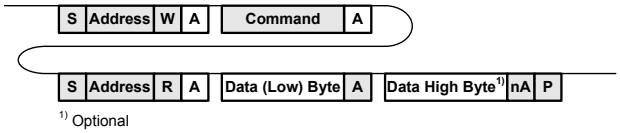
In addition, Block write commands are supported with a total maximum length of 255 bytes.



See PFE Programming Manual for further information.

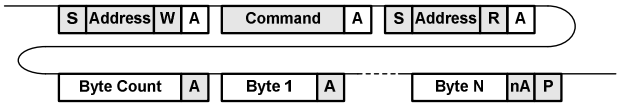
READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



1) Optional

In addition, Block read commands are supported with a total maximum length of 255 bytes.



See PFE3000-12-069RA PMBus Communication Manual BCA.00040 for further information.

9.16 GRAPHICAL USER INTERFACE

Power-One provides with its "Power-One I²C Utility" a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the PFE3000-12-069A Front-End. The utility can be downloaded on www.power-one.com and supports both the PSMI and PMBus™ protocols.

The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.

If the GUI is used in conjunction with the PFE3000-12-069RA Evaluation Kit it is also possible to control the PSON_L pin(s) of the power supply.

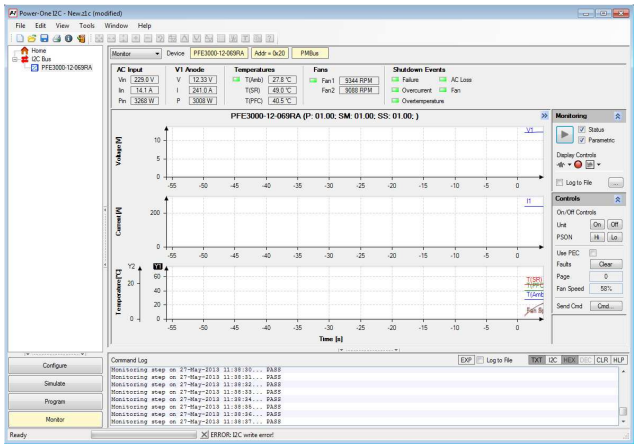


Figure 30: Monitoring dialog of the I²C Utility

10 TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. The PFE3000-12-069RA is provided with a reverse airflow, which means the air enters through the front of the supply and leaves at the rear. PFE supplies have been designed for horizontal operation.

The fan inside of the supply is controlled by a microprocessor. The rpm of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

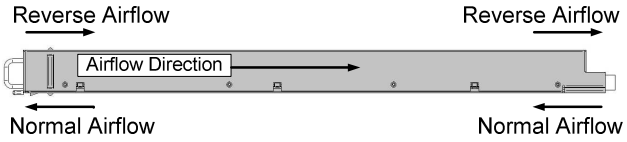


Figure 31: Airflow direction

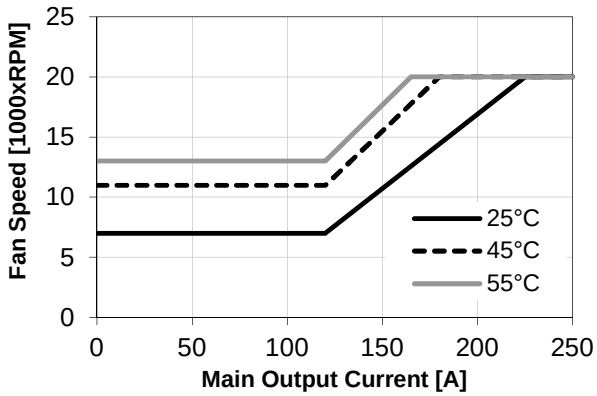


Figure 32: Fan speed vs. main output load for PFE3000-12-069RA

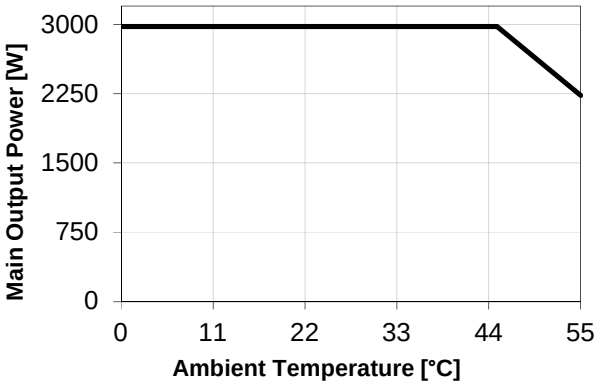


Figure 33: Thermal derating for PFE3000-12-069RA

11 ELECTROMAGNETIC COMPATIBILITY

11.1 IMMUNITY

Note: Most of the immunity requirements are derived from EN 55024:1998/A2:2003.

Test	Standard / Description	Criteria
ESD Contact Discharge	IEC / EN 61000-4-2, ±8 kV, 25+25 discharges per test point (metallic case, LEDs, connector body)	A
ESD Air Discharge	IEC / EN 61000-4-2, ±15 kV, 25+25 discharges per test point (non-metallic user accessible surfaces)	A
Radiated Electromagnetic Field	IEC / EN 61000-4-3, 10 V/m, 1 kHz/80% Amplitude Modulation, 1 µs Pulse Modulation, 10 kHz…2 GHz	A
Burst	IEC / EN 61000-4-4, level 3 AC port ±2 kV, 1 minute DC port ±1 kV, 1 minute	A
Surge	IEC / EN 61000-4-5 Line to earth: level 3, ±2 kV Line to line: level 2, ±1 kV	A
RF Conducted Immunity	IEC/EN 61000-4-6, Level 3, 10 Vrms, CW, 0.1 … 80 MHz	A
Voltage Dips and Interruptions	IEC/EN 61000-4-11 1: Vi 230Volts 50 Hertz, 100% Load, Dip 100%, Duration 12 ms 2: Vi 230Volts 50 Hertz, 100% Load, Dip 70%, Duration 1s	A

11.2 EMISSION

Test	Standard / Description	Criteria
Conducted Emission	EN55022 / CISPR 22: 0.15 … 30 MHz, QP and AVG, single unit	Class A 6 dB margin
	EN55022 / CISPR 22: 0.15 … 30 MHz, QP and AVG, 2 units in rack system	Class A 6 dB margin
Radiated Emission	EN55022 / CISPR 22: 30 MHz … 1 GHz, QP, single unit	Class A 6 dB margin
	EN55022 / CISPR 22: 30 MHz … 1 GHz, QP, 2 units in rack system	Class A 6 dB margin
Harmonic Emissions	IEC61000-3-2, Vin = 208/230 VAC, 50 Hz, 100% Load	Class A
Acoustical Noise	Sound power statistical declaration (ISO 9296, ISO 7779, IS9295) @ 50% load	53 dBA
AC Flicker	IEC / EN 61000-3-3, d_{max} < 3.3%	PASS

12 SAFETY / APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 60950, and UL 60950. Input-to-output electric strength tests should not be repeated in the field. Power-One will not honor any warranty claims resulting from electric strength field tests.

Parameter		Description / Conditions	Min	Nom	Max	Unit
	Agency Approvals	UL 60950-1 Second Edition CAN/CSA-C22.2 No. 60950-1-07 Second Edition IEC 60950-1:2005 EN 60950-1:2006	Approved by independent body (see CE Declaration)			
	Isolation strength	Input (L/N) to case (PE)	Basic			
		Input (L/N) to output	Reinforced			
		Output to case (PE)	Functional			
d_C	Creepage / clearance	Primary (L/N) to protective earth (PE)	According to safety standard			mm
		Primary to secondary				mm
	Electrical strength test	Input to case				kVAC
		Input to output				kVAC
		Output and Signals to case				kVAC

13 MECHANICAL

13.1 DIMENSIONS

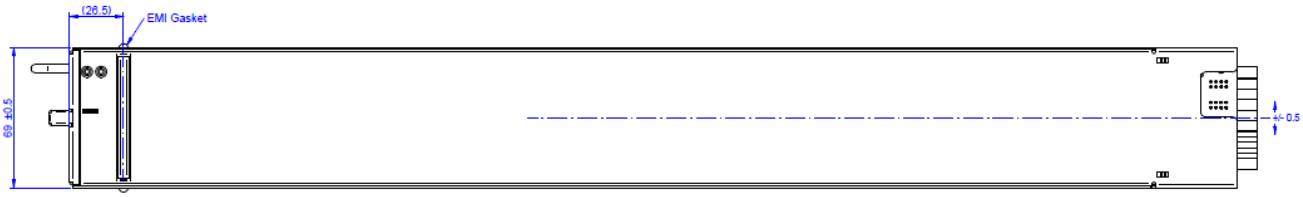


Figure 34: Bottom view

Note: A 3D step file of the power supply casing is available on request.

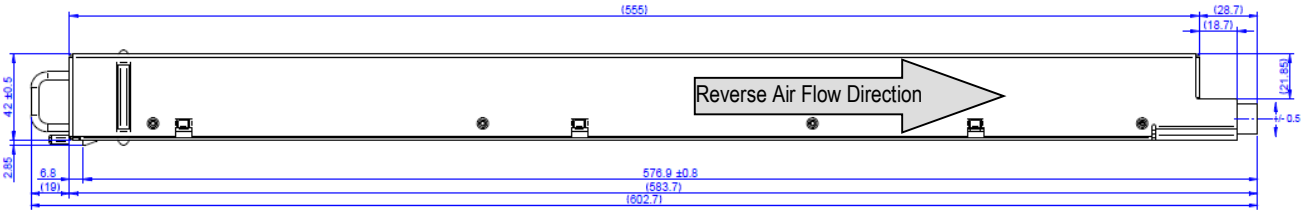


Figure 35: Side view

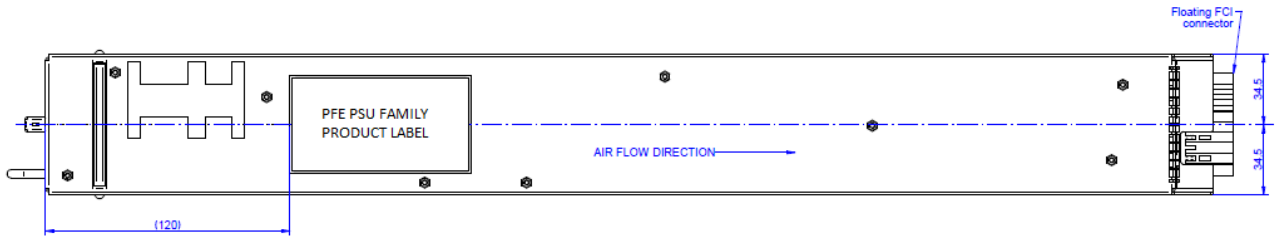


Figure 36: Top view

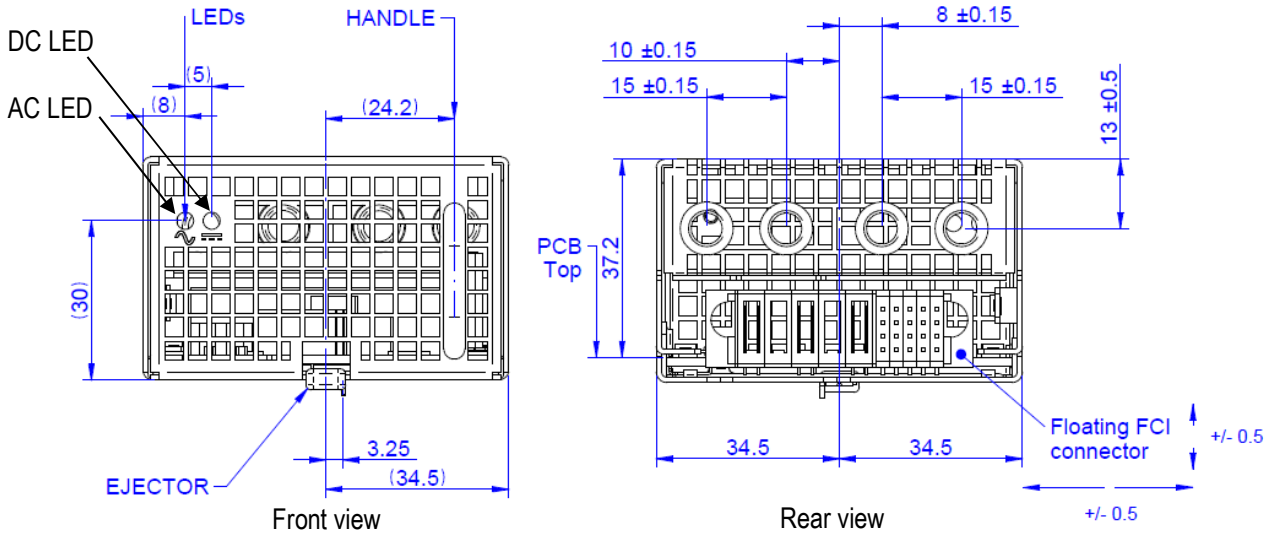
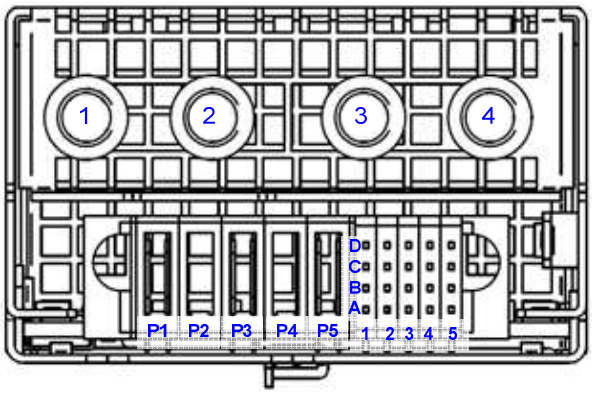


Figure 37: Front and rear view

14 CONNECTIONS



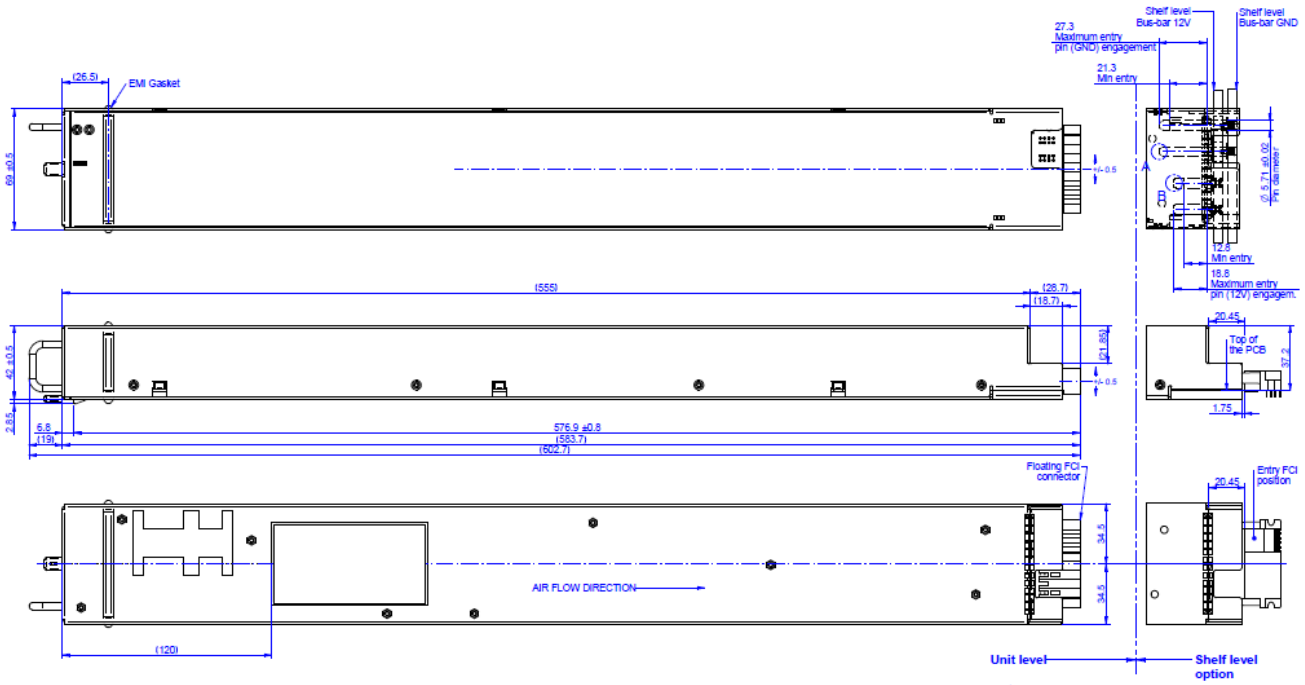
Unit: FCI Connectors P/N 51939-768LF
Counterpart: FCI Connectors P/N 51915-401LF
For Main Output Pins, see section 15

Note: A1 and A2 are Trailing Pin (short pins)

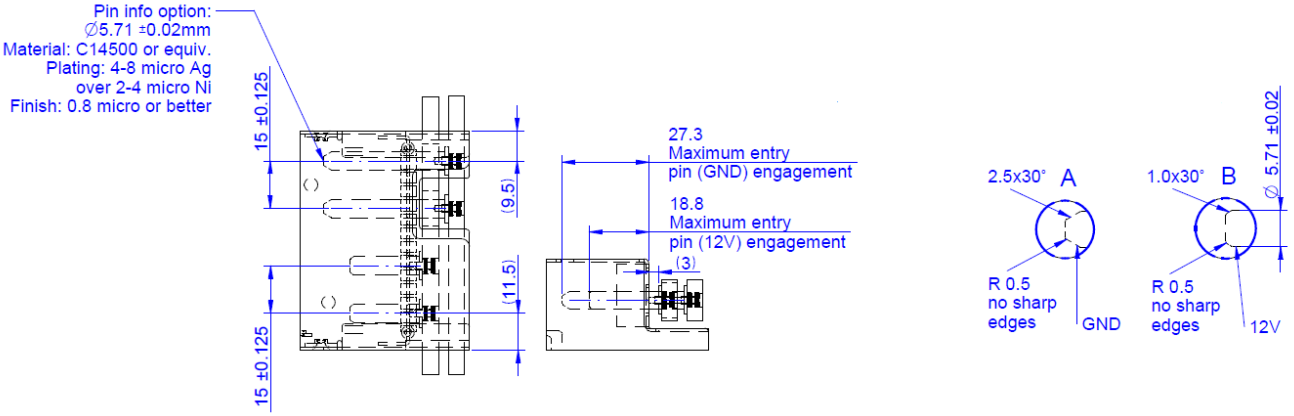
Pin	Name	Description
Output		
3,4	V1	+12 VDC main output
1,2	PGND	+12 VDC main output ground
Input Pins		
P1	LIVE	AC Live Pin
P2	N.C	No metal pin connection
P3	NEUTRAL	AC Neutral Pin
P4	N.C.	No metal pin connection
P5	P.E.	Protective Earth Pin
Control Pins		
A1	PSKILL	Power supply kill (trailing pin): active-low
B1	PWOK_L	Power OK signal output: active-low
C1	INOK_L	Input OK signal: active-low
D1	PSON_L	Power supply on input: active-low
A2	PRESENT_L	Power supply present (trailing pin): active-low
B2	SGND	Signal ground[5] (return)
C2	SGND	Signal ground[5] (return)
D2	SGND	Signal ground[5] (return)
A3	SCL	I^2C clock signal line
B3	SDA	I^2C data signal line
C3	SMB_ALERT_L	SMB Alert signal output: active-high
D3	ISHARE	V_1 Current share bus
A4	EEPROM_WP	EEPROM write protect
B4	RESERVED	Reserved
C4	V1_SENSE_R	Main output negative sense
D4	V1_SENSE	Main output positive sense
A5	VSB	Standby positive output
B5	VSB	Standby positive output
C5	VSB_GND	Standby Ground[5]
D5	VSB_GND	Standby Ground[5]

5) This pins should be connected to PGND on the system.

15 SHELF LEVEL CONFIGURATION



Main output pin configuration



16 ACCESSORIES

Item	Description	Ordering Part Number	Source
	**Power-One I²C Utility** Windows XP/Vista/7 compatible GUI to program, control and monitor PFE Front-Ends (and other I²C units)	N/A	www.power-one.com
	**USB to I²C Converter** Master I²C device to program, control and monitor I²C units in conjunction with the *Power-One I²C Utility*	ZM-00057	Power-One
	**Dual Connector Board** Connector board to parallel PFE units in parallel. Includes an on-board USB to I²C converter (use *Power-One I²C Utility* as desktop software).	TBD	Power-One

To be updated

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