An 8-V to 14-V Vin 2010 Atom™ E6xx Tunnel Creek Power System

The TPS59610EVM-634 evaluation module (EVM) is a complete solution for the 2010 Atom™ E6xx Tunnel Creek Power System from a 12-V input bus. The EVM uses the TPS59610 for Atom CPU and GPU core, TPS51120 for 5-V and 3.3-V systems, TPS54326 for Topcliff IOH, TPS59124 for DDRII 1.8 V and CPU VTT 1.05 V, TPS51100 for 0.9 V VTT, TPS74801 for CPU 1.5-V PLL, and CPU C6 RAM 1.05 V. TPS59610EVM-634 also uses the 3-mm x 3-mm Texas Instruments (TI) power block MOSFET (CSD86330Q3D) for high-power density and superior thermal performance.

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Atom is a trademark of Intel Corporation.

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1 Description

The TPS59610EVM-634 is designed to use a regulated 12-V (8-V to 14-V) bus to produce 10 regulated outputs for an Atom™ E6xx Tunnel Creek Power System. The TPS59610EVM-634 is specially designed to demonstrate the TPS59610 Atom E6xx CPU and GPU Vcore regulators while providing a number of test points to evaluate their static and dynamic performance.

1.1 Typical Applications

- 8-V to 14-V Vin Atom E6xx Tunnel Creek Power System for embedded computing platforms

1.2 Features

The TPS59610EVM-634 features:

- Complete solution for 8-V to 14-V Vin Atom Tunnel Creek Power System
- Selectable 200/300/400/500-kHz switching frequency for CPU and GPU power
- Selectable current limit for CPU and GPU power
- Selectable output overshoot reduction (OSR™) for CPU and GPU power
- Switches or jumpers for each output enable
- Onboard dynamic load for CPU, GPU Vcore output
- High efficiency and high density by using TI power block MOSFET
- Convenient test points for probing critical waveforms
- Four-layer printed-circuit board with 2 oz of copper on the outside layers

2 Atom Tunnel Creek Power System Block Diagram

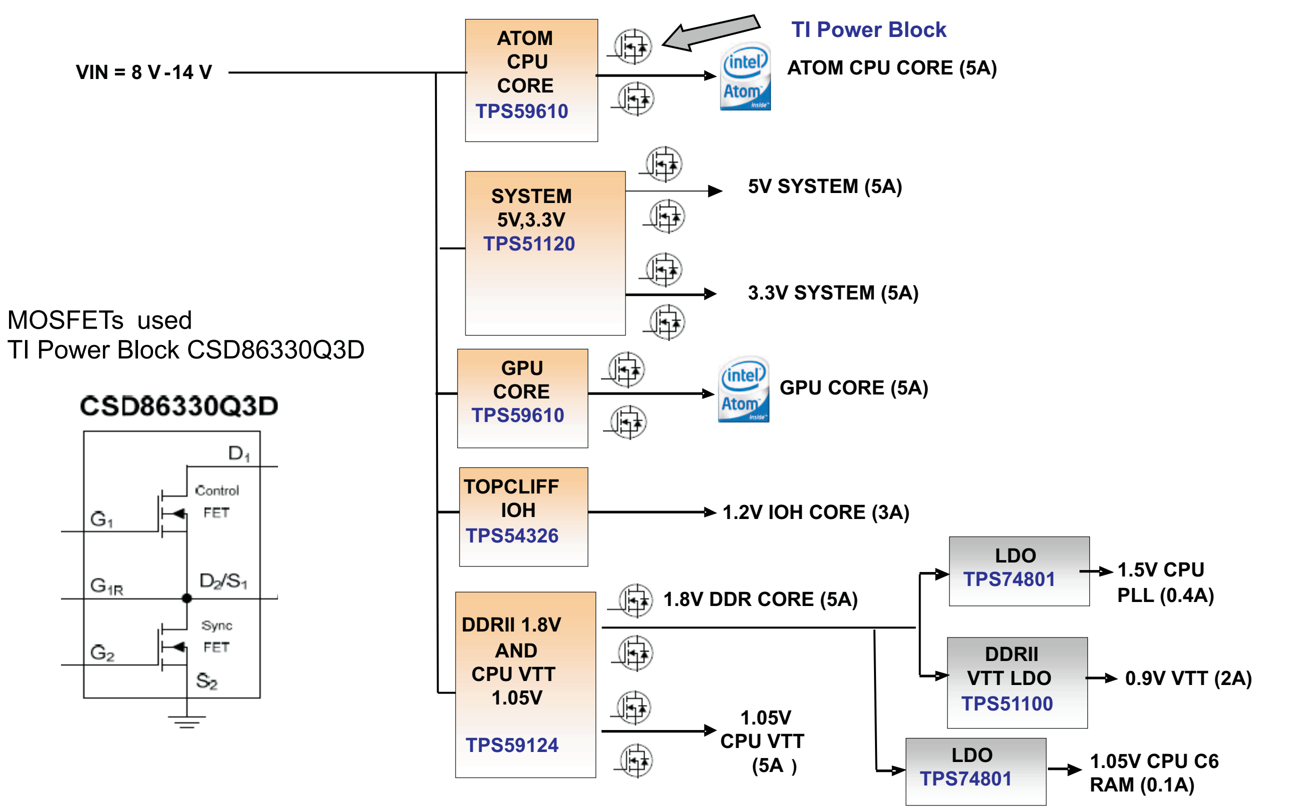


Figure 1. 8-V to 14-V Vin 2010 Atom Tunnel Creek Power System Block Diagram

3 Electrical Performance Specifications

Table 1. TPS59610EVM-634 Electrical Performance Specifications(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
VIN input voltage range	VIN	8	12	14	V
Maximum input current	VIN = 8 V, all full load			10	A
No load input current	VIN = 14 V, Io = 0 A			5	mA
OUTPUT CHARACTERISTICS					
CPU (TPS59610)					
Output voltage Vcore	VID0 = VID1 = VID2 = VID4 = VID6 = 0, VID3 = VID5 = 1		1.00		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation (droop) load line		–5.7		mΩ
Output voltage ripple	VIN = 12 V, Io = 5 A at 300 kHz		30		mVpp
Output load current		0		5	A
Output over current			7.2		A
Switching frequency	Selectable	200	300	500	kHz
Full load efficiency	VIN = 12 V, 1 V/5 A at 300 kHz		85.5%		
GPU (TPS59610)					
Output voltage Vcore	VID0 = VID2 = VID4 = VID5 = 0, VID1 = VID3 = 1, VID6 = 5 V		1.00		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation(droop) load line		–5.7		mΩ
Output voltage ripple	VIN = 12 V, Io = 5 A at 300 kHz		30		mVpp
Output load current		0		5	A
Output over current			7.2		A
Switching frequency	Selectable	200	300	500	kHz
Full load efficiency	VIN = 12 V, 1 V/5 A at 300 kHz		86.7%		
5-V AND 3.3-V SYSTEM (TPS51120)					
Output voltage			5/3.3		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation		0.1%		
Output voltage ripple	VIN = 12 V, Io = 5 A		45		mVpp
Output load current		0		5	A
Output over current			10		A
Switching frequency	Selectable		280/430		kHz
Full load efficiency	VIN = 12 V, 5 V/5 A, 3.3 V/5 A		94.7/92.1%		
DDR 1.8-V and 1.05-V CPU VTT (TPS59124)					
Output voltage			1.8/1.05		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation		1%		
Output voltage ripple	VIN = 12 V, Io = 5 A		30		mVpp
Output load current		0		5	A
Output over current			10		A
Switching frequency	Selectable		300/360		kHz
Full load efficiency	VIN = 12 V, 1.8 V/5 A, 1.05 V/5 A		90.3/85.1%		

(1) Jumpers set to default locations, see Section 6 of this user's guide.

Table 1. TPS59610EVM-634 Electrical Performance Specifications[(1)] (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1.2-V IOH(TPS54326)					
Output voltage			1.2		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation		1%		
Output voltage ripple	VIN = 12 V, 1.2 Vout, Io = 3 A		20		mVpp
Output load current		0		3	A
Output over current			4.1		A
Switching frequency			700		kHz
Full load efficiency	12 Vin, 1.2 V/3 A		75.4%		
1.5-V CPU PLL(TPS74801)					
Output voltage			1.5		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation		1%		
Output voltage ripple	VIN = 1.8 V,1.5 Vout, Io = 0.4 A		10		mVpp
Output load current		0		0.4	A
Output over current			2		A
Switching frequency			N/A		kHz
Full load efficiency			N/A%		
0.9-V VTT (TPS51100)					
Output voltage			0.9		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation		±40		mV
Output voltage ripple	VIN = 1.8 V, 0.9 VTT, Io = 2 A		10		mVpp
Output load current		0		2	A
Output over current			3		A
Switching frequency			N/A		kHz
Full load efficiency			N/A%		
1.05-V CPU C6 RAM (TPS74801)					
Output voltage			1.05		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation		1%		
Output voltage ripple	VIN = 1.8 V, 1.05 Vout, Io = 0.1 A		10		mVpp
Output load current		0		0.1	A
Output over current			2		A
Switching frequency			N/A		kHz
Full load efficiency			N/A%		
Operating temperature			25		°C

4 Schematics

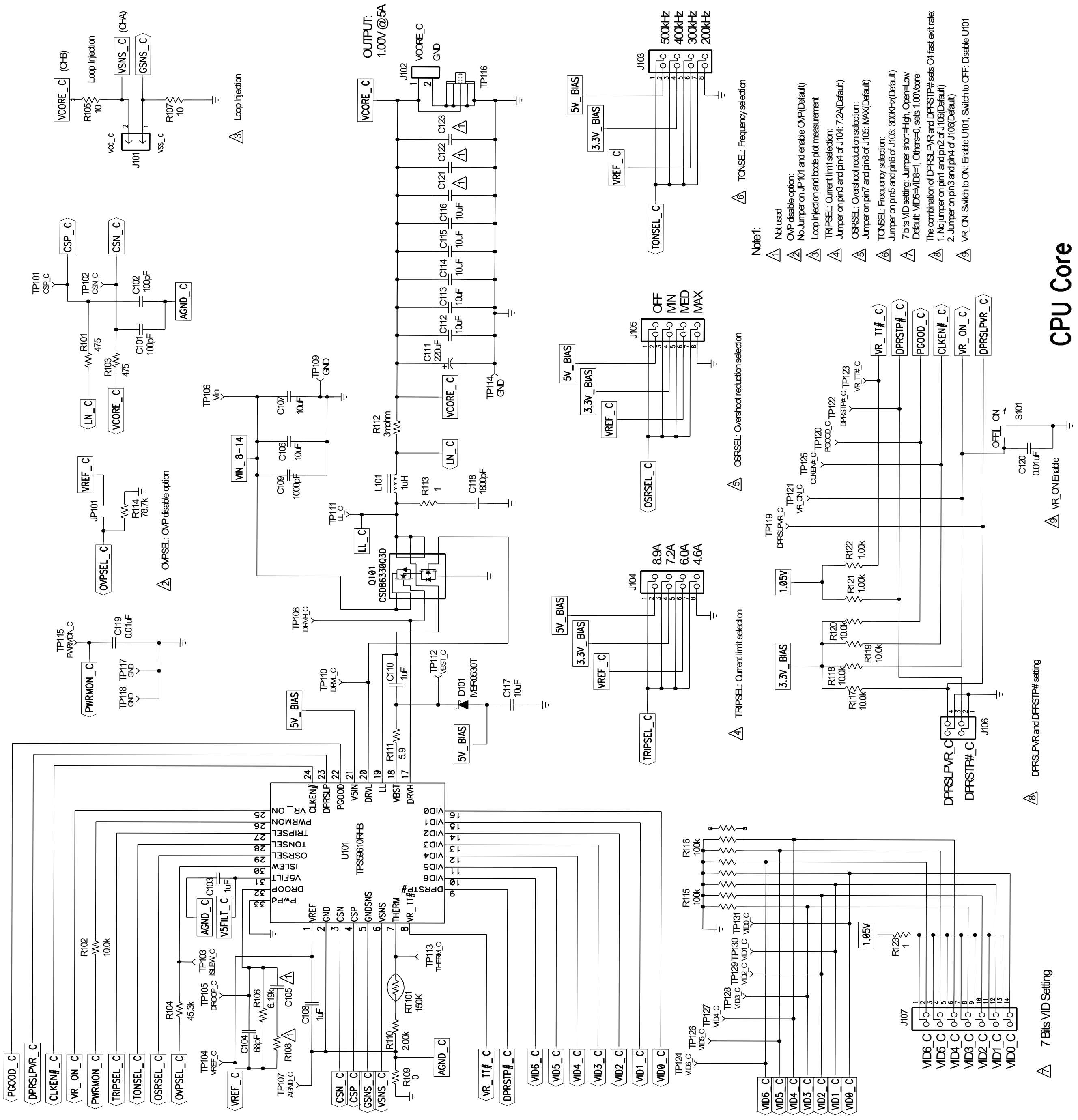


Figure 2. TPS59610EVM-634 Schematic, Sheet 1 of 5

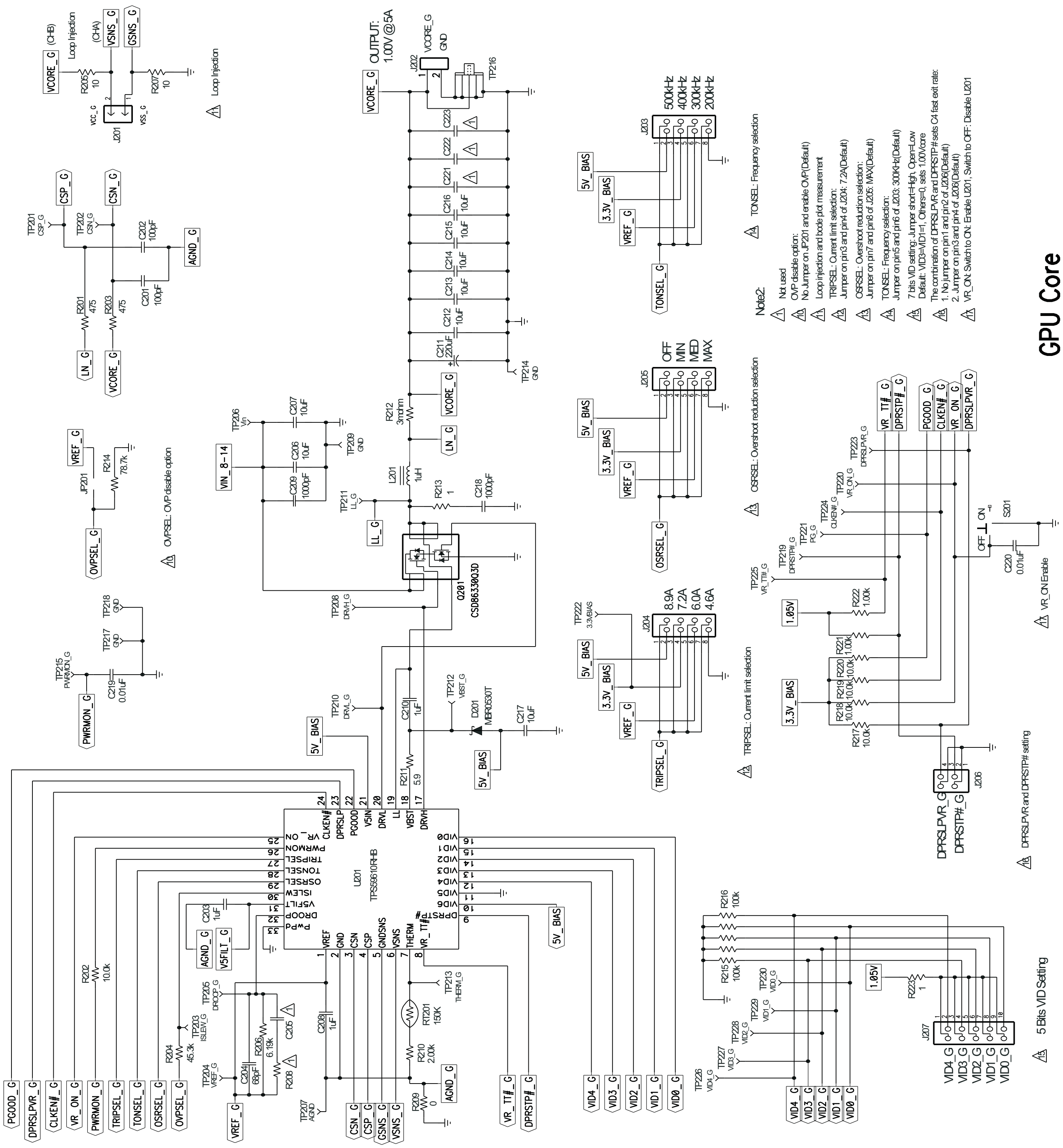


Figure 3. TPS59610EVM-634 Schematic, Sheet 2 of 5

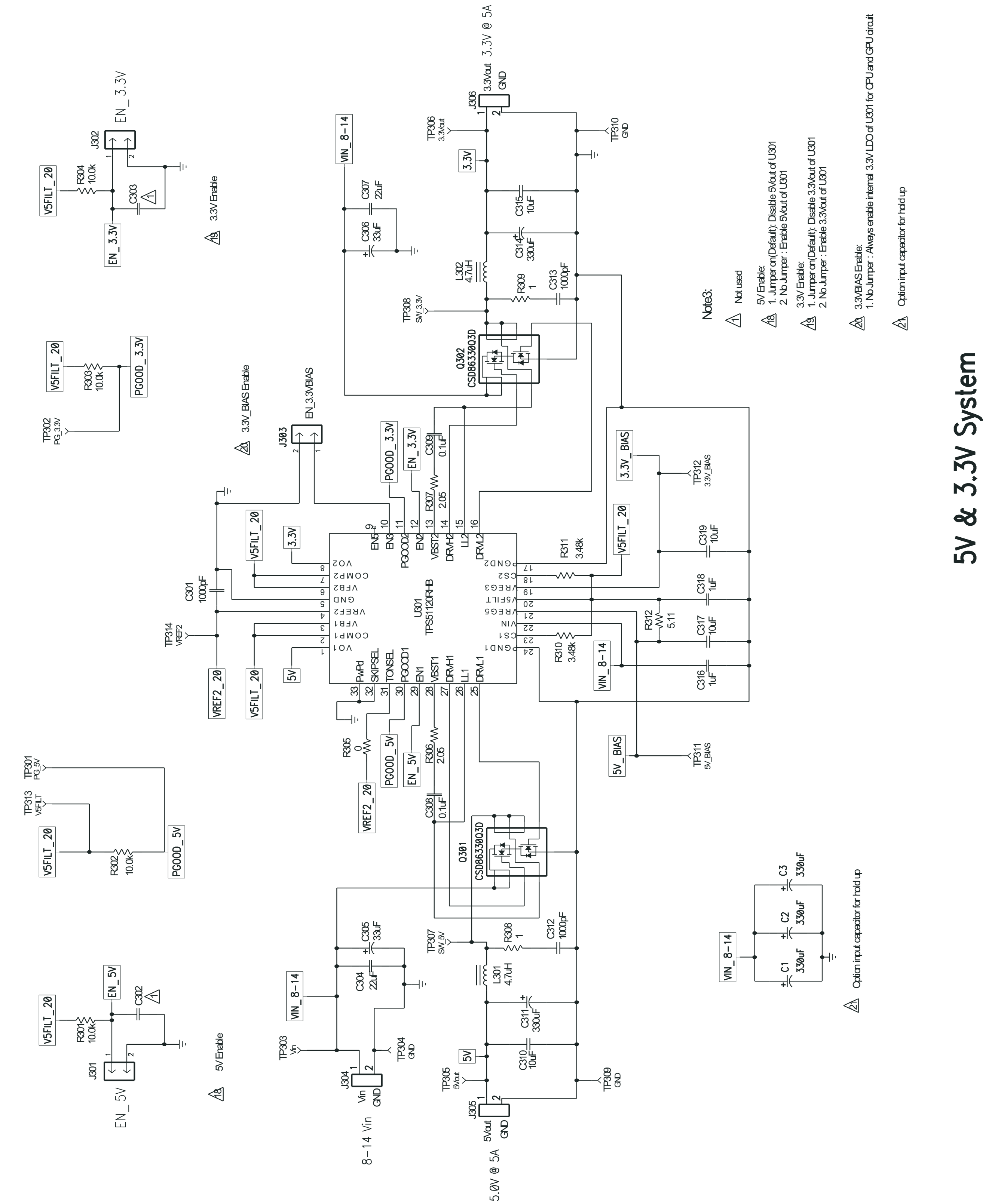


Figure 4. TPS59610EVM-634 Schematic, Sheet 3 of 5

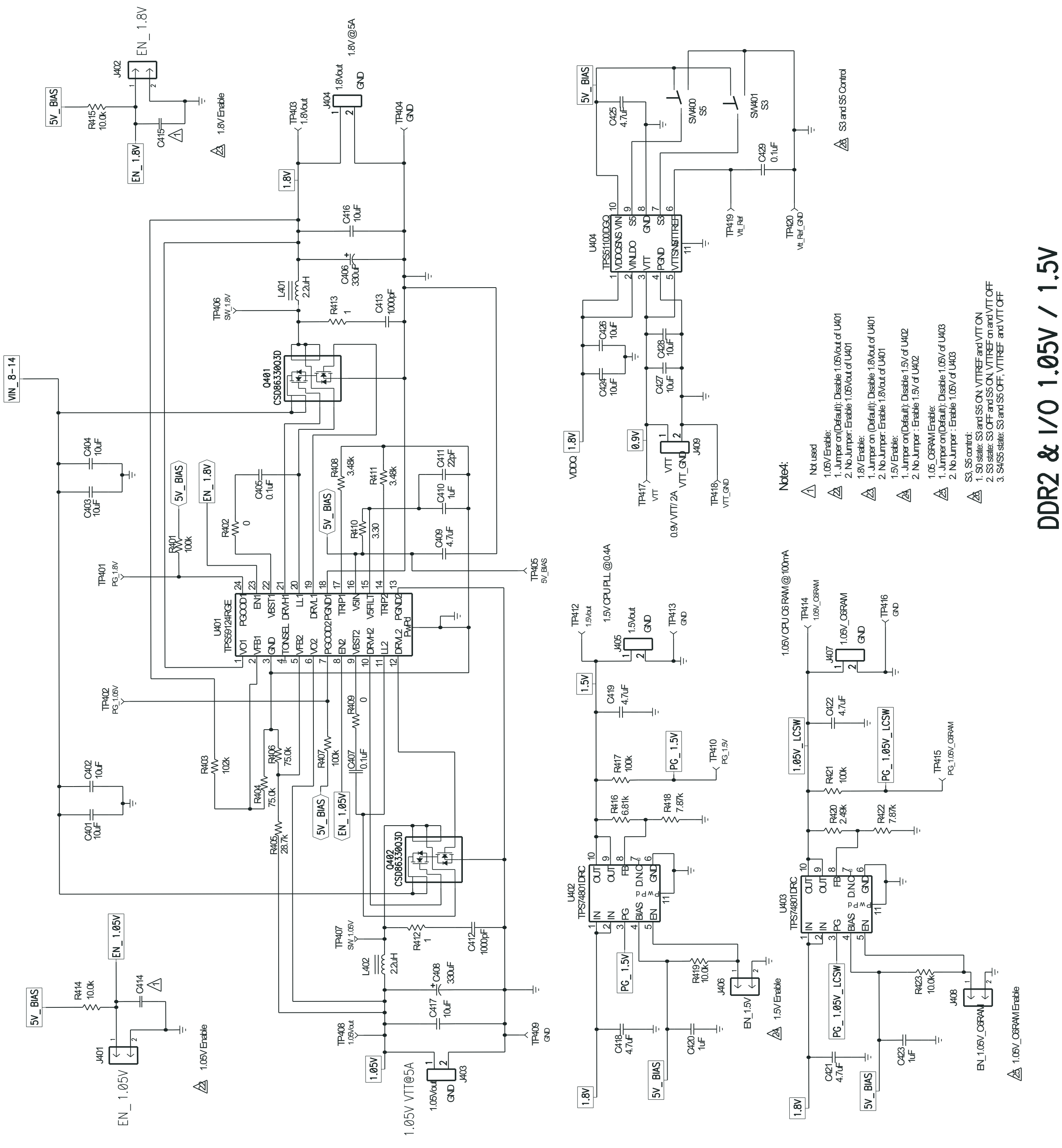


Figure 5. TPS59610EVM-634 Schematic, Sheet 4 of 5

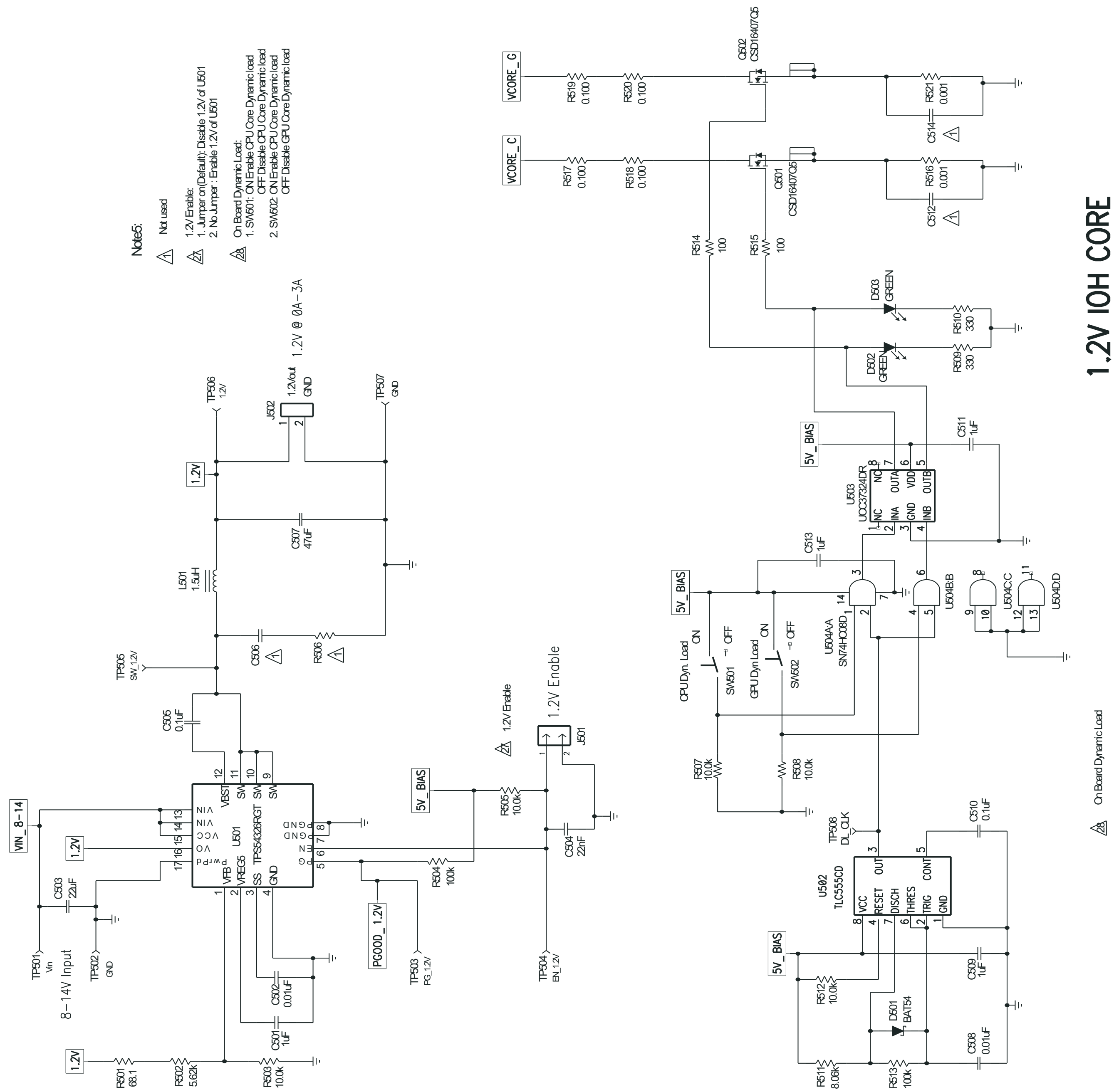


Figure 6. TPS59610EVM-634 Schematic, Sheet 5 of 5

5 Test Setup

5.1 Test Equipment

Voltage Source VIN: The input voltage source VIN must be a 0-V to 14-V variable dc source capable of supplying 10 Adc. Connect VIN to J304 as shown in Figure 7.

Multimeters:
V1: Vin at TP303 (VIN) and TP304 (GND)
V2: Vout at each output test point. For example: CPU at J101
A1: Vin input current

Output Load: The output load must be an electronic constant resistance mode load capable of 0 Adc to 10 Adc.

Oscilloscope: A digital or analog oscilloscope can be used to measure the output ripple. The oscilloscope must be set for 1-MΩ impedance, 20-MHz bandwidth, ac coupling, 2-µs/division horizontal resolution, 50-mV/division vertical resolution. Test points on each output can be used to measure the output ripple voltage. Do not use a leaded ground connection as this may induce additional noise due to the large ground loop.

Recommended Wire Gauge:

1. VIN to J304 (12-V input):
   The recommended wire size is AWG 16 per input connection, with the total length of wire less than 4 feet (2-foot input, 2-foot return).
2. Each outputs to LOAD:
   The minimum recommended wire size is AWG 16, with the total length of wire less than 4 feet (2-foot output, 2-foot return)

5.2 Recommended Test Setup

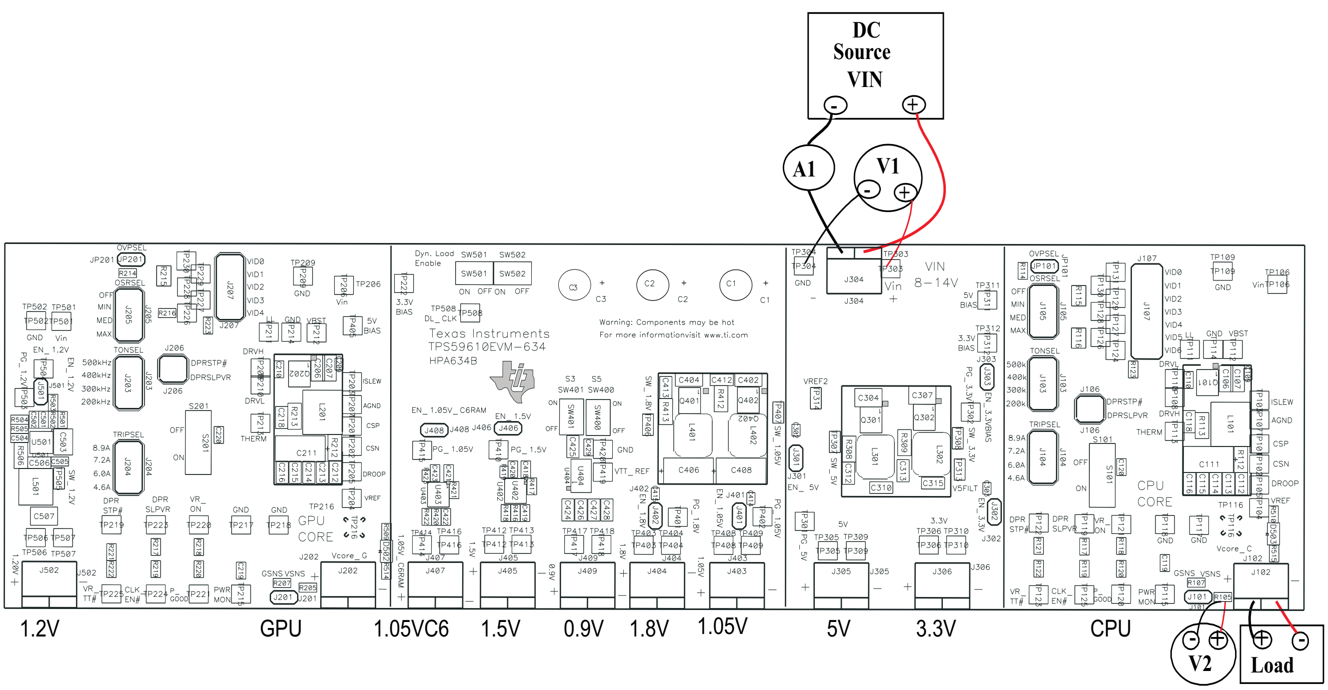


Figure 7. TPS59610EVM-634 Recommended Test Setup

Figure 7 is the recommended test setup to evaluate the TPS59610EVM-634. Working at an ESD workstation, ensure that wrist straps, bootstraps, or mats are connected referencing the user to earth ground before handling the EVM.

Input Connections:

1. Prior to connecting the dc input source VIN, it is advisable to limit the source current from VIN to 10 A maximum. Ensure that VIN is initially set to 0 V and connected as shown in Figure 7.
2. Connect a voltmeter V1 at TP303 (VIN) and TP304 (GND) to measure VIN input voltage.
3. Connect a current meter A1 between VIN dc source and J304.

Output Connections (For example, CPU testing)

1. Connect the load to J102, and set the load to constant resistance mode to sink 0 Adc before VIN is applied.
2. Connect a voltmeter V2 at J101 to measure CPU 1-Vcore voltage as shown in Figure 7.

6 Configuration

All jumper selections must be made prior to applying power to the EVM. Users can configure this EVM per the following configurations.

6.1 CPU and GPU Configuration

6.1.1 Current-Limit Trip Selection (J104 for CPU and J204 for GPU)

The current-limit trip can be set by J104 and J204 TRIPSEL.
Default setting: 7.2 A.

Table 2. Current-Limit Trip Selection

Jumper set to	TRIPSEL	OCP Limit, Typ. (A)
Top (1-2 pin shorted)	5VFILT	8.9
Second (3-4 pin shorted)	**3.3VBIAS**	**7.2**
Third (5-6 pin shorted)	VREF	6
Bottom (7-8 pin shorted)	GND	4.6

6.1.2 Frequency Selection (J103 for CPU and J203 for GPU)

The operating frequency can be set by J103 and J203 TONSEL.
Default setting: 300 kHz.

Table 3. Frequency Selection

Jumper set to	TONSEL	Frequency (kHz)
Top (1-2 pin shorted)	5VFILT	500
Second (3-4 pin shorted)	3.3VBIAS	400
Third (5-6 pin shorted)	**VREF**	**300**
Bottom (7-8 pin shorted)	GND	200

6.1.3 Overshoot Reduction Selection (J105 for CPU and J205 for GPU)

The overshoot reduction can be set by J105 and J205 OSRSEL.
Default setting: Maximum

Table 4. Overshoot Reduction Selection

Jumper set to	OSR	Overshoot Voltage Reduction
Top(1-2 pin shorted)	5VFILT	OFF
Second (3-4 pin shorted)	3.3VBIAS	Minimum
Third (5-6 pin shorted)	VREF	Medium
Bottom (7-8 pin shorted)	**GND**	**Maximum**

6.1.4 VID Bits Selection

The CPU Vcore voltage can be set by J107(7-Bit CPU VID).
Default setting: 0101000 for 1.000V
Jumper = 1
No Jumper = 0

Table 5. CPU VID Bits Selection

7-Bit VID Table (1 = 1.05 V, 0 = GND)							
VID6	**VID5**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**Vcore(V)**
0	0	0	0	0	0	0	1.500
0	0	1	1	0	0	0	1.200
0	**1**	**0**	**1**	**0**	**0**	**0**	**1.000**
0	1	1	1	0	0	0	0.800
1	0	0	1	0	0	0	0.600
1	0	1	1	0	0	0	0.400
1	1	0	0	0	0	0	0.300

See data sheet for details.

The GPU Vcore voltage can be set by J207 (5-bit GPU VID).
Default setting: 01010 for 1.000V

Table 6. GPU VID Bits Selection

5-Bit VID Table (1 = 1.05 V, 0 = GND)					
VID4	**VID3**	**VID2**	**VID1**	**VID0**	**Vcore(V)**
0	0	0	0	0	1.250
0	0	1	1	0	1.100
0	**1**	**0**	**1**	**0**	**1.000**
1	0	0	1	0	0.800
1	1	0	1	0	0.600
1	1	1	1	1	0.400

See data sheet for details.

6.1.5 Deep Sleep Mode Selection (DPRSLPVR)

The combination of DPRSTP# and DPRSLPVR sets C4 exit rate. These can be set by J106 for CPU and J206 for GPU.
Default setting: Jumper on DPRSLPVR and no jumper on DPRSTP# of J106 and J206

Table 7. C4 Exit Rate Selection

Jumper set to	C4 exit rate
Jumper on DPRSLPVR **No jumper on DPRSTP#**	**C4 exit fast**
No jumper on DPRSLPVR No jumper on DPRSTP#	C4 exit slow

6.1.6 Overvoltage Protection Selection (JP101 for CPU and JP201 for GPU)

The overvoltage protection selection can be set by JP101 and JP201, OVPSEL
Default setting: No jumper shorts on JP101 and JP201 to enable OVP

Table 8. Overvoltage Protection selection

Jumper set to	Selection
No jumper	**OVP enabled**
Jumper shorted	**OVP disabled**

6.1.7 Onboard Dynamic Load Selection (SW501 for CPU and SW502 for GPU)

The onboard dynamic load can be set by SW501 and SW502.
Default setting: Push SW501 and SW502 to the right to disable the onboard dynamic load.

Table 9. Onboard Dynamic Load Selection

Switch set to	Dynamic Load Selection
Push SW501 to left (On position)	Enable 5-A onboard dynamic load at CPU
Push SW501 to right (Off position)	**Disable 5-A onboard dynamic load at CPU**
Push SW502 to left (On position)	Enable 5-A onboard dynamic load at GPU
Push SW502 to right (Off position)	**Disable 5-A onboard dynamic load at GPU**

6.1.8 Enable Selection (S101 for CPU and S201 for GPU)

The Vcore of CPU and GPU can be enabled and disabled by S101 and S201.
Default setting: Push S101 and S201 to the TOP(Off position) to disable both CPU and GPU

Table 10. Enable Selection

Switch set to	Dynamic Load Selection
Push S101 to bottom (On position)	Enable CPU Vcore
Push S101 to top (Off position)	**Disable CPU Vcore**
Push S201 to bottom (On position)	Enable GPU Vcore
Push S201 to top (Off position)	**Disable GPU Vcore**

6.2 5-V/3.3-V System Configuration

6.2.1 3.3VBIAS Enable Selection (J303)

3.3VBIAS Enable can be set by J303, EN_3.3VBIAS
Default setting: No Jumper shorts on J303 to enable the 3.3VBIAS
Note: 3.3VBIAS needs to always be enabled for CPU and GPU circuit

6.2.2 5-V/3.3-V Enable Selection (J301 for 5 V and J302 for 3.3 V)

5-V/3.3-V Enable can be set by J301 and J302, EN_5V and EN_3.3V
Default setting: Jumper shorts on J301 and J302 to disable 5 V/3.3 V.

Table 11. 5-V/3.3-V Enable Selection

Jumper set to	Selection
Jumper on J301	**5-V Disabled**
No jumper on J301	5-V Enabled
Jumper on J302	**3.3-V Disabled**
No jumper on J302	3.3-V Enabled

6.3 DDR 1.8-V/1.05-V CPU VTT Configuration

6.3.1 1.8-V/1.05-V Enable can be set by J402 for 1.8 V and J401 for 1.05 V, EN_1.8V and EN_1.05V

Default setting: Jumper shorts on J402 to disable 1.8 V. No Jumper on J401 to enable 1.05 V

Note: 1.05V enable is for VID setting of CPU and GPU

Table 12. 1.8-V/1.05-V Enable Selection

Jumper set to	Selection
Jumper on J402	**1.8V Disabled**
No Jumper on J402	1.8V Enabled
Jumper on J401	1.05V Disabled
No Jumper on J401	**1.05V Enabled**

6.4 0.9-V VTT and 0.9-V VTTREF Configuration

6.4.1 0.9-V VTT and 0.9-V VTTREF Enable Selection (SW401 for S3, SW400 for S5)

Default setting: Push SW400 and SW401 to bottom to disable both 0.9VTT and 0.9VTTREF.

Table 13. SW400(S5), SW401(S3) Enable Selection

State	SW401 set to	SW400 set to	VTT, VTTREF
S0	S3 Top(on)	S5 Top(on)	VTT and VTTREF on
S3	S3 Bottom(off)	S5 Top(on)	VTT off and VTTREF on
S4/S5	**S3 Bottom(off)**	**S5 Bottom(off)**	**VTT and VTTREF off**

6.5 1.5-V CPU PLL Configuration

6.5.1 1.5-V Enable Selection (J406)

1.5-V Enable can be set by J406, EN_1.5V
Default setting: Jumper shorts on J406 to disable 1.5 V

Table 14. 1.5-V Enable Selection

Jumper set to	Selection
No Jumper	1.5V Enabled
Jumper on	**1.5V Disabled**

6.6 1.05-V CPU C6 RAM Configuration

6.6.1 1.05-V CPU C6 RAM Enable Selection (J408)

1.05-V Enable can be set by J408, EN_1.05V_C6RAM
Default setting: Jumper shorts on J408 to disable 1.05-V CPU C6 RAM

Table 15. 1.05-V CPU C6 RAM Enable Selection

Jumper set to	Selection
No Jumper	1.05V CPU R6 RAM Enabled
Jumper on	**1.05V CPU C6 RAM Disabled**

6.7 1.2-V IOH Configuration

6.7.1 1.2-V Enable Selection (J501)

1.2-V Enable can be set by J501, EN_1.2V
Default setting: Jumper shorts on J501 to disable 1.2 V

Table 16. 1.2-V Enable selection

Jumper set to	Selection
No Jumper	1.2V Enabled
Jumper on	**1.2V Disabled**

7 Test Procedure

7.1 Line/Load Regulation and Efficiency Measurement Procedure

The CPU measurement is performed in the following manner.

1. Set up EVM as described in Section 5.1 and Figure 7.
2. Ensure that the Load is set to constant resistance mode and sink 0 A.
3. Ensure that all the jumper configuration settings are per Section 6
4. Ensure that the S101 VR_ON enable switch is set to OFF before VIN is applied.
5. Increase VIN from 0 V to 12 V. Use V1 to measure VIN voltage.
6. Set switch S101 to ON to enable the controller.
7. Use V2 to measure Vcore_c voltage.
8. Vary Load from 0 Adc to 5 Adc; Vcore_c must remain in load regulation.
9. Vary VIN from 8 V to 14 V; Vcore_c must remain in line regulation.
10. Set switch S101 to OFF to disable the controller.
11. Decrease Load to 0 A.
12. Decrease VIN to 0 V.
    Other output testing is the same.

7.2 Onboard Transient Response Measurement

CPU and GPU Only

1. Set up EVM as described in Section 5.1 and Figure 7.
2. Ensure that all the jumper configuration settings are per Section 6
3. Remove the load from J102 for CPU or J202 for GPU
4. Ensure that VR_ON (S101 for CPU and S201 for GPU) is on OFF before VIN is applied.
5. Increase VIN from 0 V to 12 V. Use V1 to measure VIN voltage.
6. Use TP508 (DL_CLK) and TP209 (GND) to measure transient timing signal.
7. Push switch SW501 (CPU) or SW502 (GPU) to ON position (left), and dynamic load LED D503 for CPU and D502 for GPU illuminate.
8. Measure the Vcore_c or Vcore_G transient response by using TP116 (CPU) or TP216 (GPU).

7.3 Loop Gain/Phase Measurement

CPU and GPU Only

1. Set up EVM as described in Section 5.1 and Figure 7.
2. CPU: Connect the isolation transformer to VSNS of J101 (CPU) and Vcore_C (+)(CPU) of J102.
   GPU: Connect the isolation transformer to VSNS of J201 (GPU) and Vcore_G (+)(GPU) of J202
3. CPU: Connect input signal CHA to VSNS pin of J101 and connect output signal CHB to Vcore_C(+) of J102.
   GPU: Connect input signal CHA to VSNS pin of J201, and connect output signal CHB to Vcore_G(+) of J202.
4. Connect the GND lead of CHA and CHB to GND of TP116 (CPU) and TP216 (GPU).
5. Inject around 50-mV or less signal through the isolate transformer.
6. Sweep the frequency from 100 Hz to 1 MHz with 10-Hz or lower post filter. The control loop gain and phase margin can be measured.
7. Disconnect isolate transformer from the bode plot setup before making other measurements (signal injection into feedback may interfere with accuracy of other measurement).

7.4 Equipment Shutdown

1. Shut down Load.
2. Shut down VIN.

8 Performance Data and Typical Characteristic Curves

Figure 8 through Figure 68 present typical performance curves for TPS59610EVM-634.

Jumpers set to default locations; see Section 6 of this user's guide

8.1 CPU

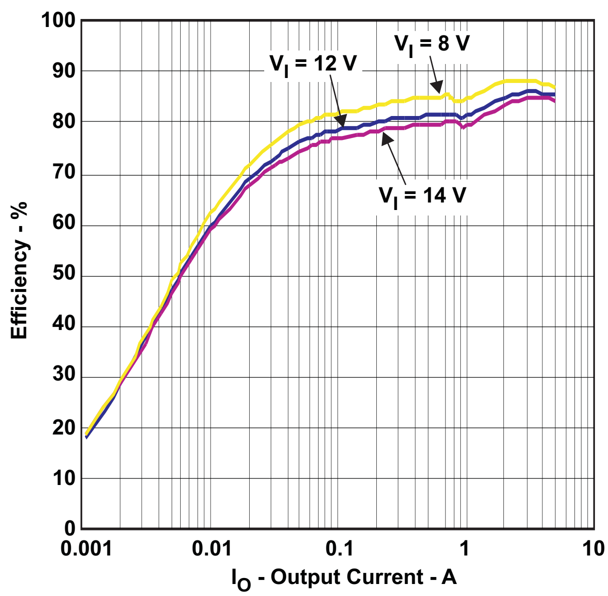


Figure 8. CPU Efficiency

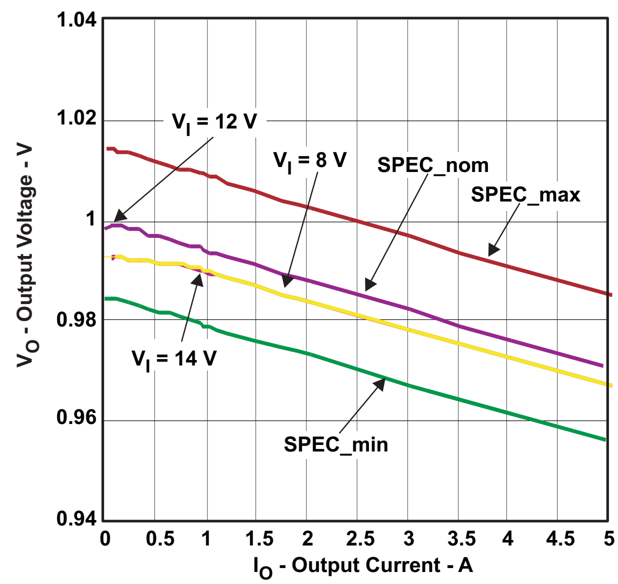


Figure 9. CPU Load Regulation

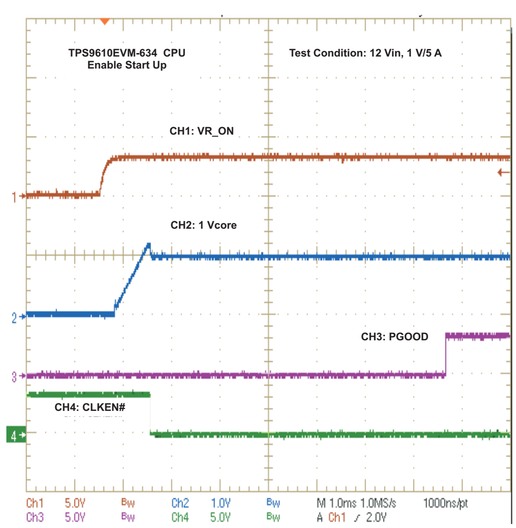


Figure 10. CPU Enable Turnon

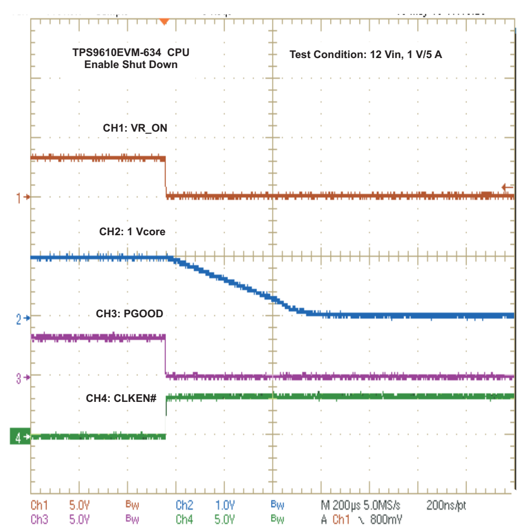


Figure 11. Enable Turnoff

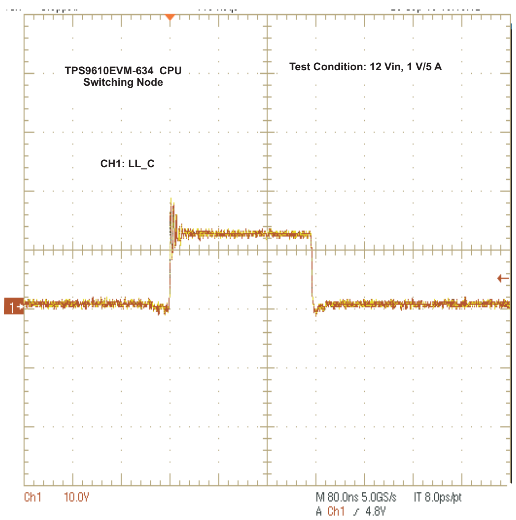


Figure 12. CPU Switching Node

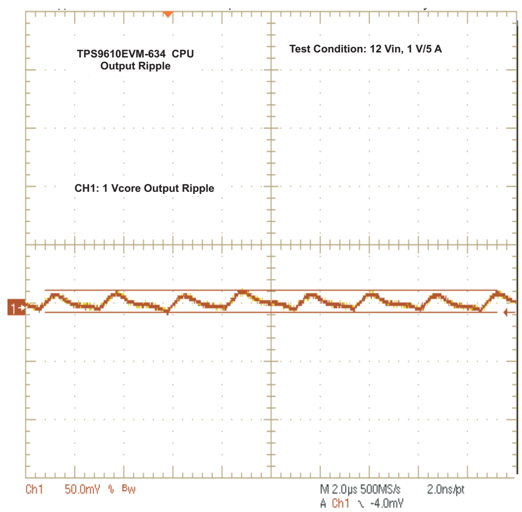


Figure 13. CPU Vcore Ripple

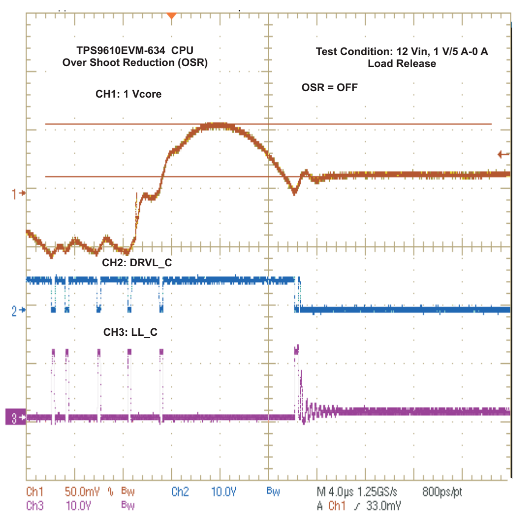


Figure 14. CPU Output Load Release Without Overshoot Reduction

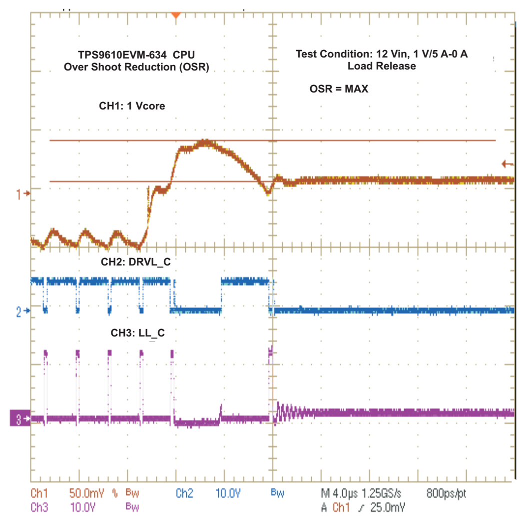


Figure 15. CPU Output Load Release With Maximum Overshoot Reduction

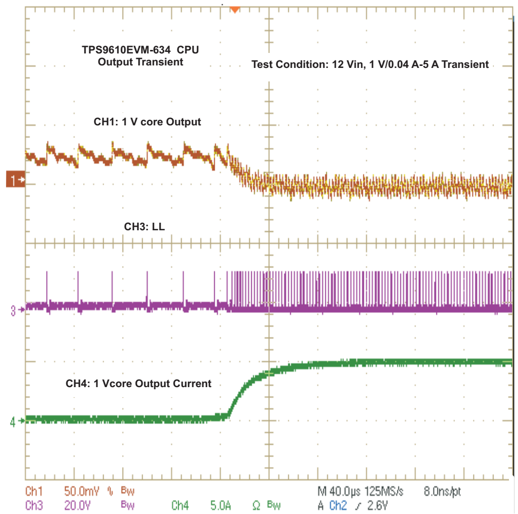


Figure 16. CPU Transient From DCM to CCM

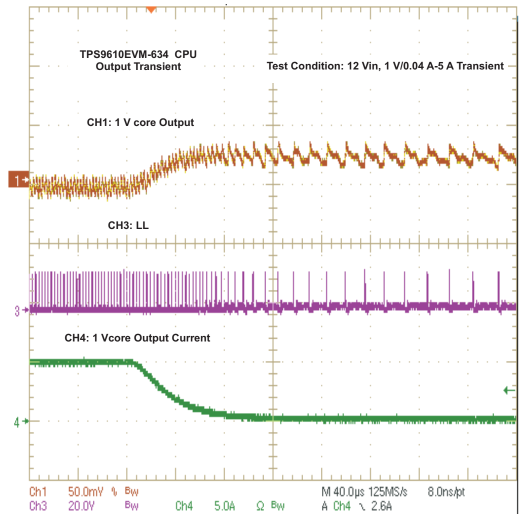


Figure 17. CPU Transient From CCM to DCM

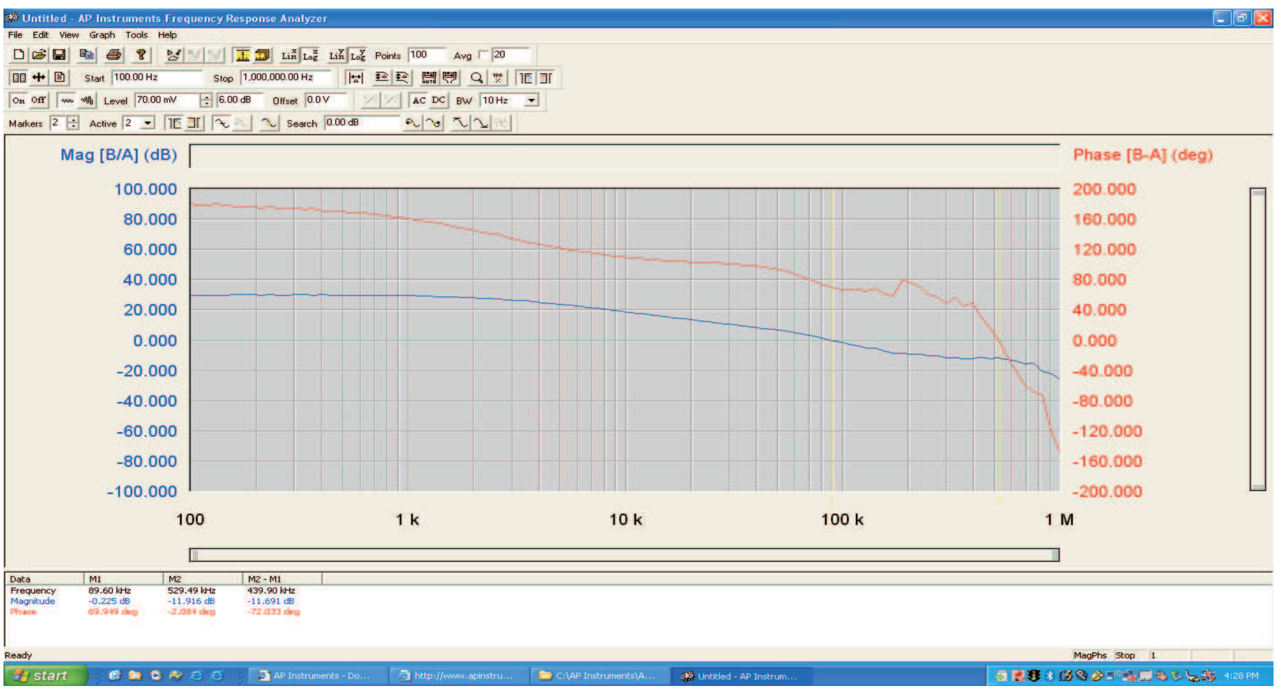


Figure 18. CPU Bode Plot 12 Vin, 1 V/5 A

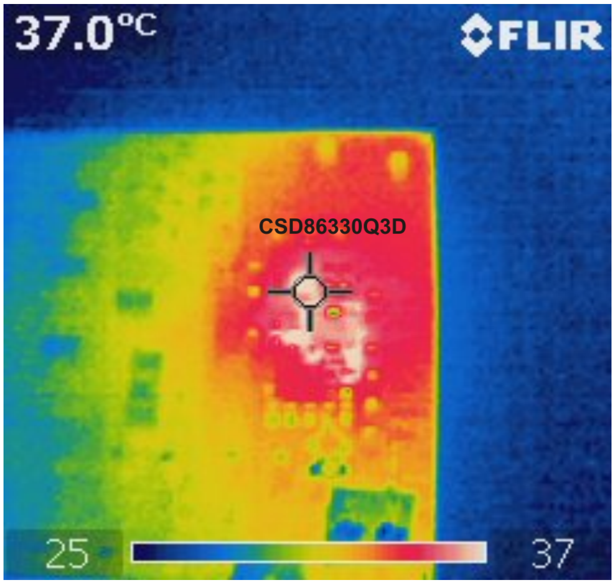


Figure 19. CPU Top Board

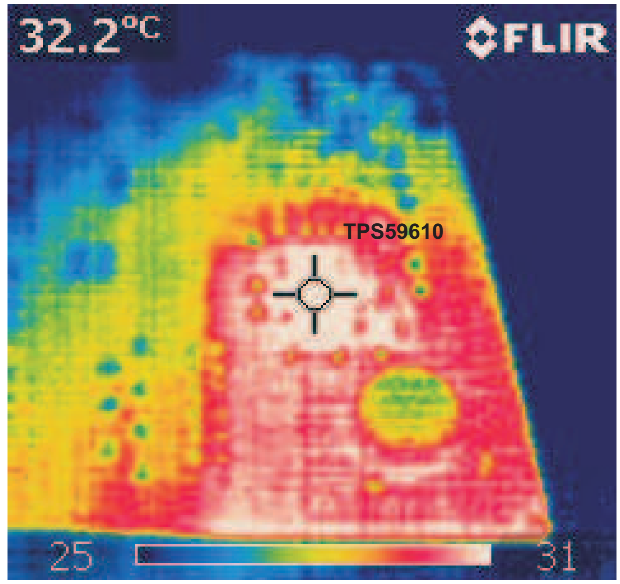


Figure 20. CPU Bottom Board

Test condition: 12 Vin, 1 V/5 A, no airflow

8.2 GPU

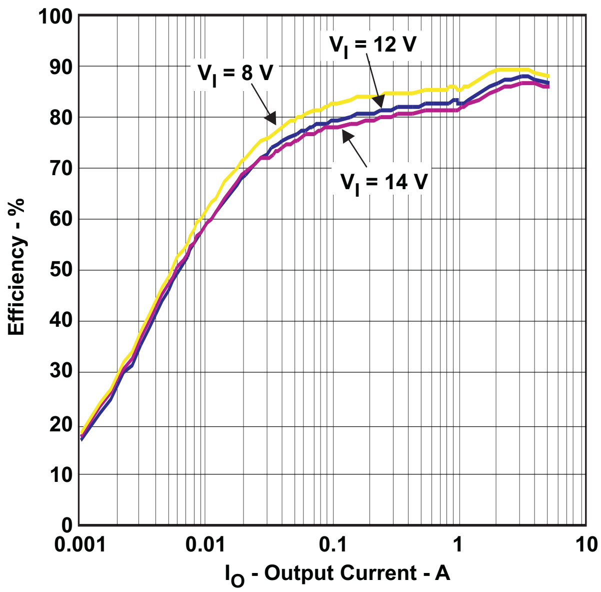
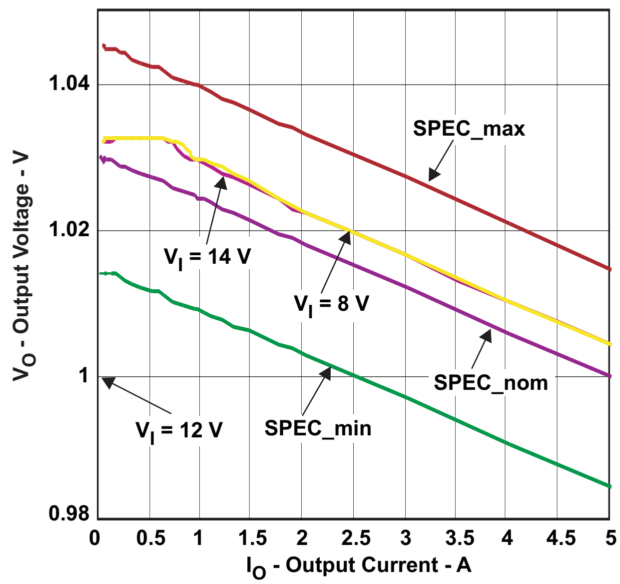


Figure 21. CPU Efficiency



NOTE: Intel spec calls for 3% offset at the VID setting

Figure 22. GPU Load Regulation

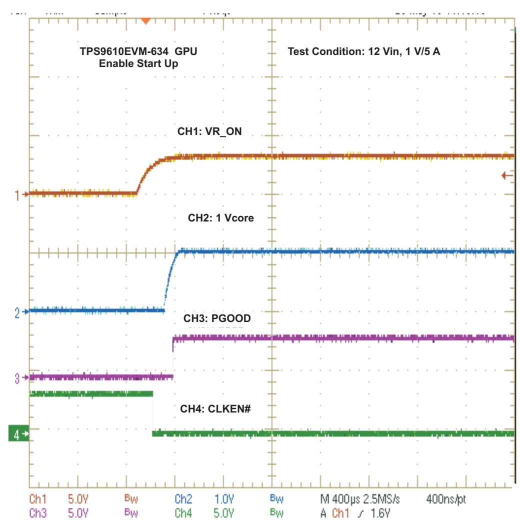


Figure 23. GPU Enable Turnon

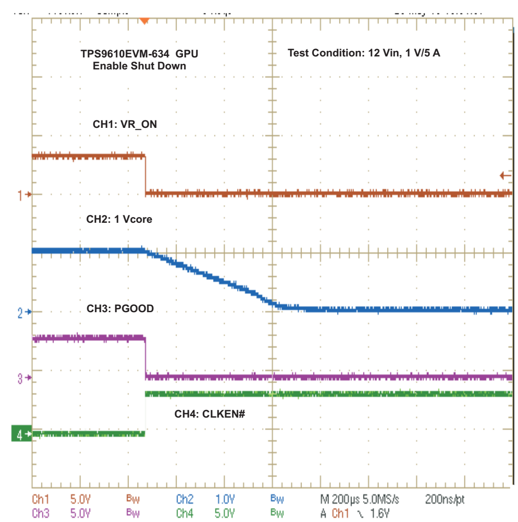


Figure 24. GPU Enable Turnoff

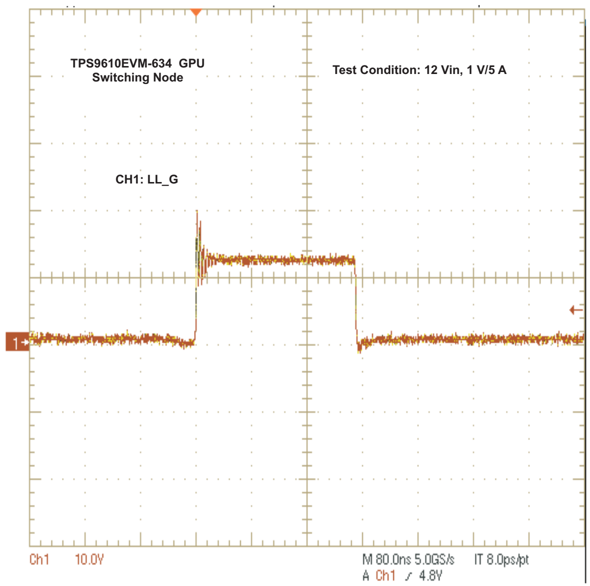


Figure 25. GPU Switching Node

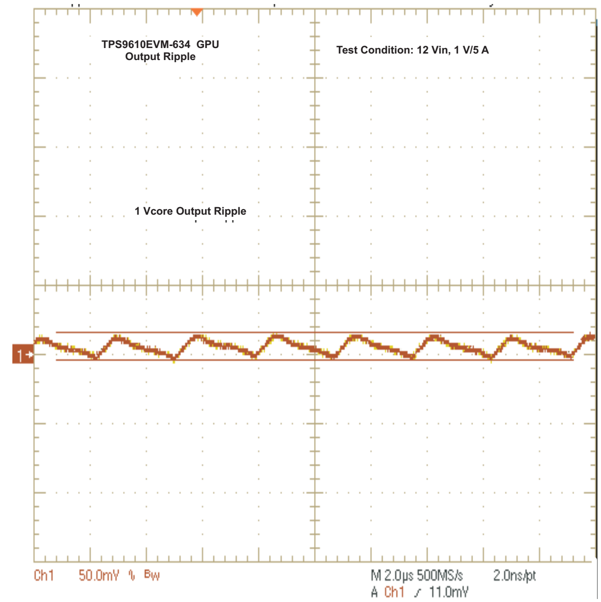


Figure 26. GPU Vcore Ripple

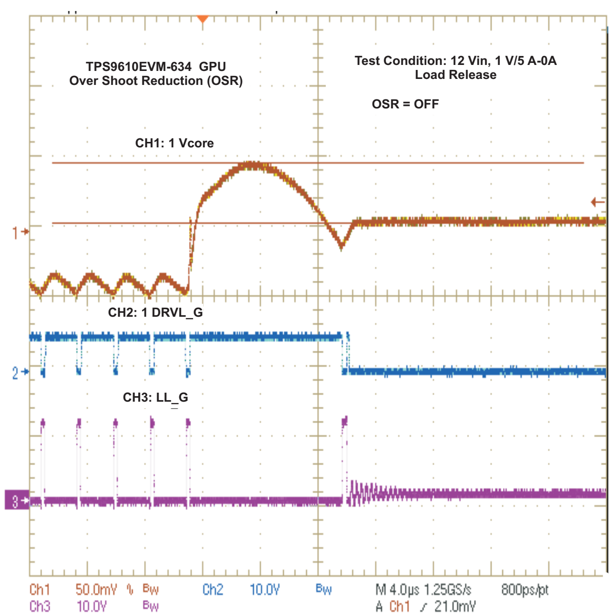


Figure 27. GPU Output Load Release Without Overshoot Reduction

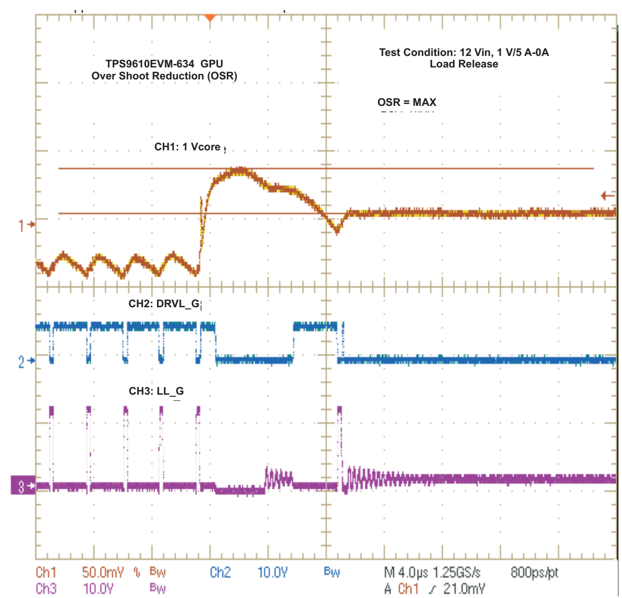


Figure 28. GPU Output Load Release With Maximum Overshoot Reduction

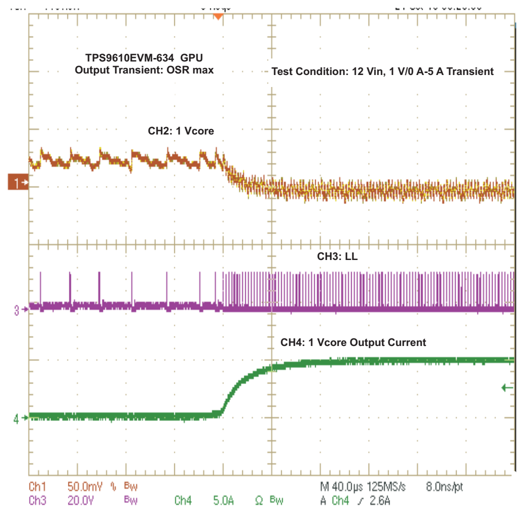


Figure 29. GPU Transient From DCM to CCM

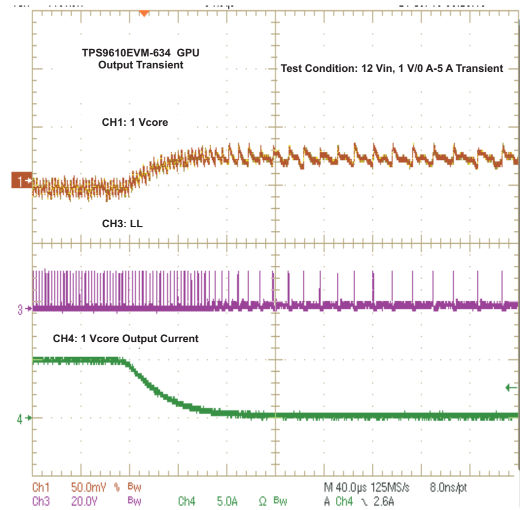


Figure 30. GPU Transient From CCM to DCM

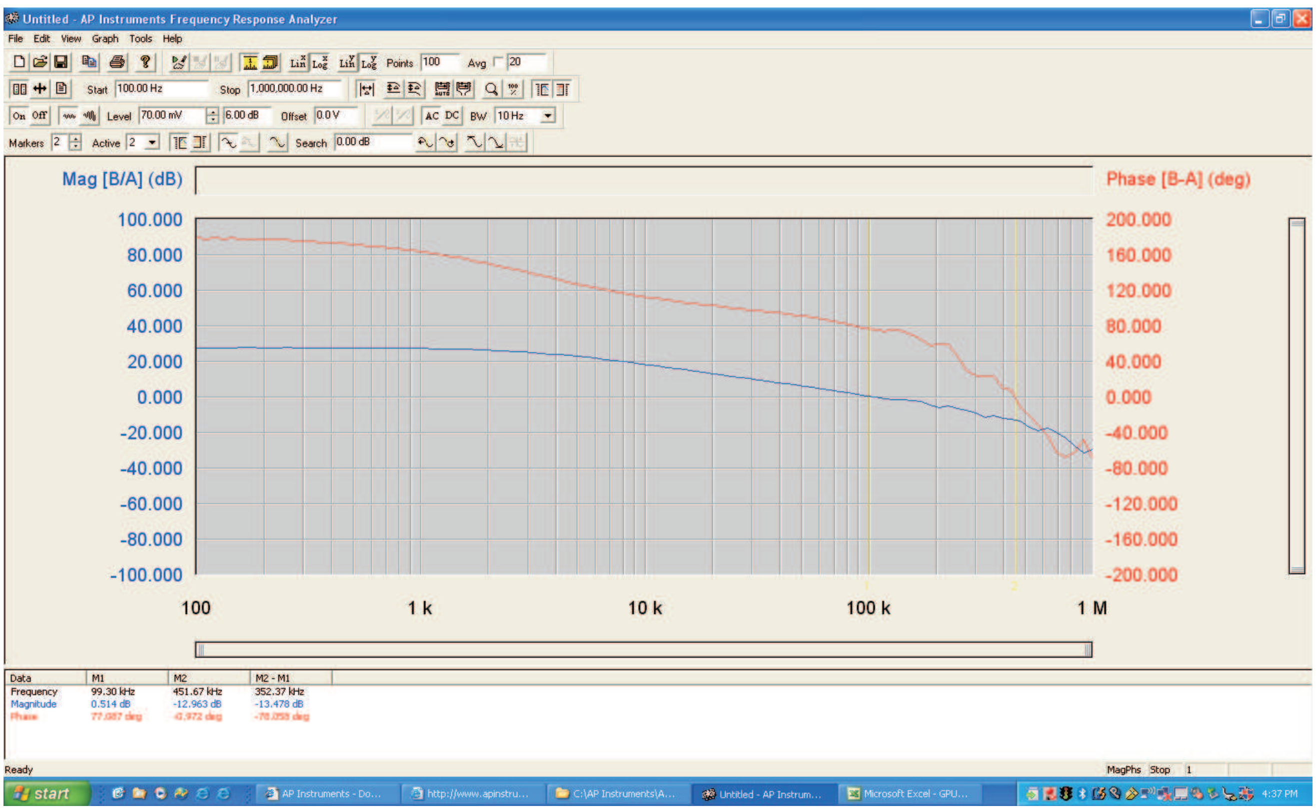


Figure 31. GPU Bode Plot 12 Vin, 1 V/5 A

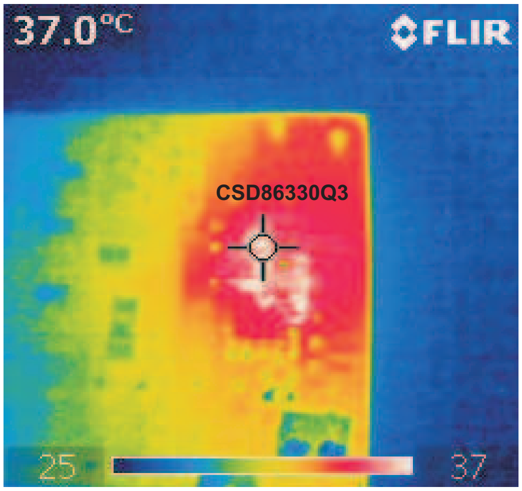


Figure 32. CPU Top Board

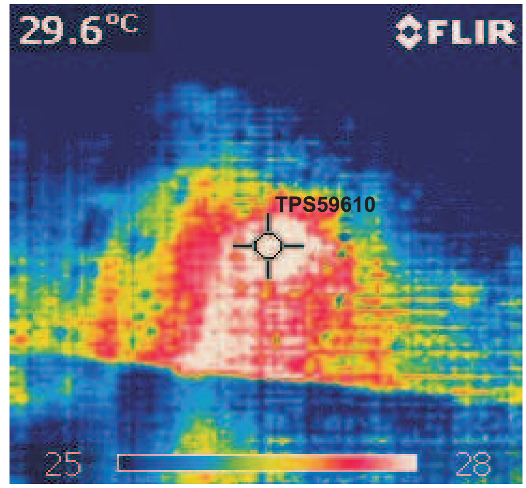


Figure 33. CPU Bottom Board

Test condition: 12 Vin, 1 V/5 A, no airflow

8.3 5-V/3.3-V System

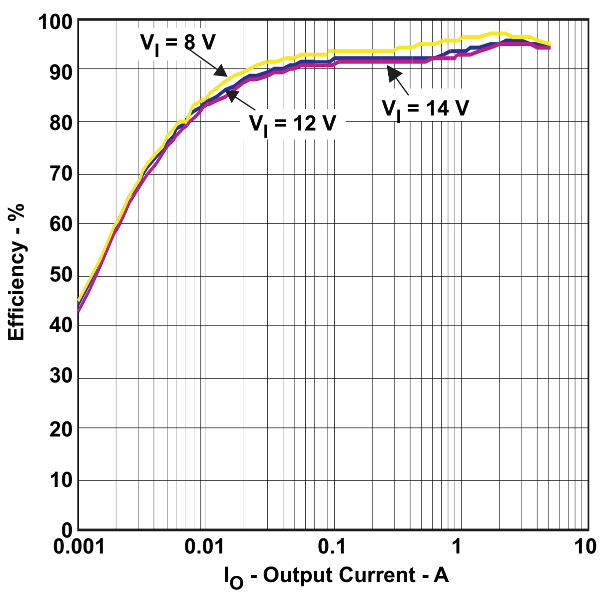


Figure 34. 5-V Efficiency

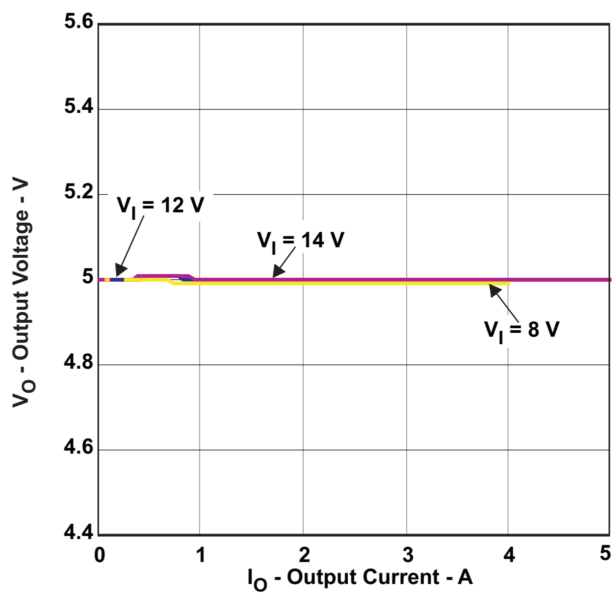


Figure 35. 5-V Load Regulation

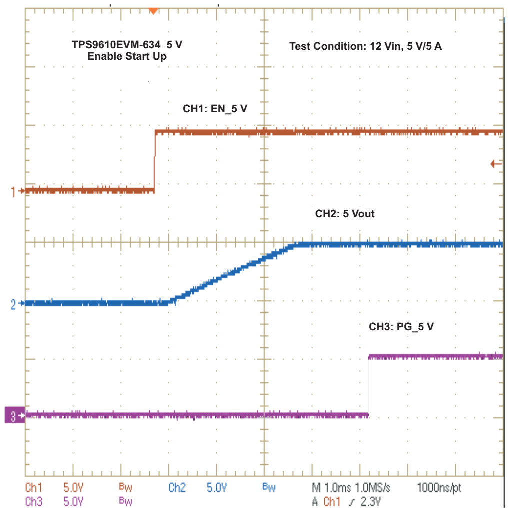


Figure 36. 5-V Enable Turnon

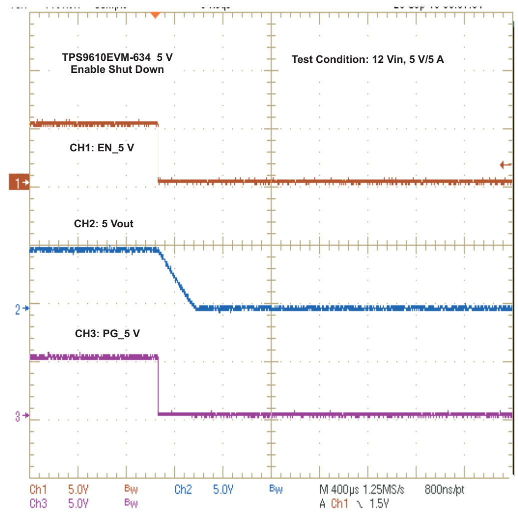


Figure 37. 5-V Enable Turnoff

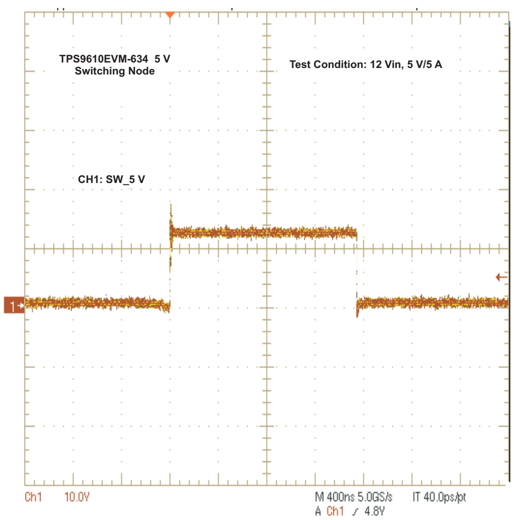


Figure 38. 5-V Switching Node

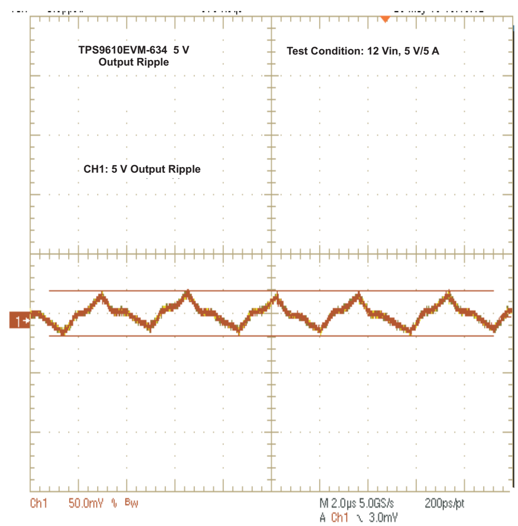


Figure 39. 5-V Vo Ripple

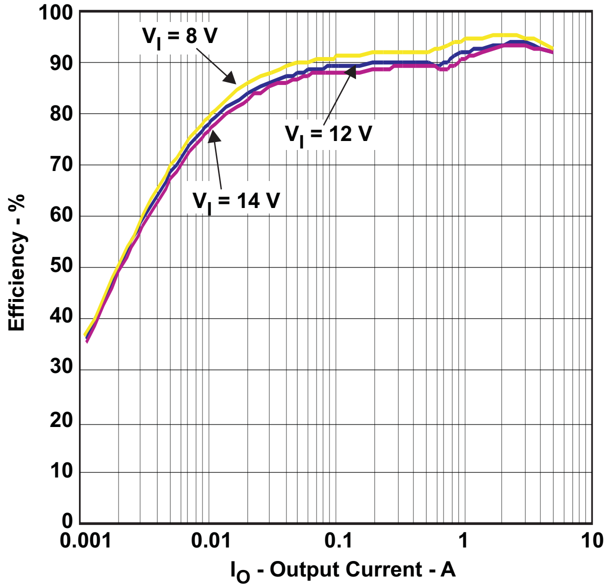


Figure 40. 3.3-V Efficiency

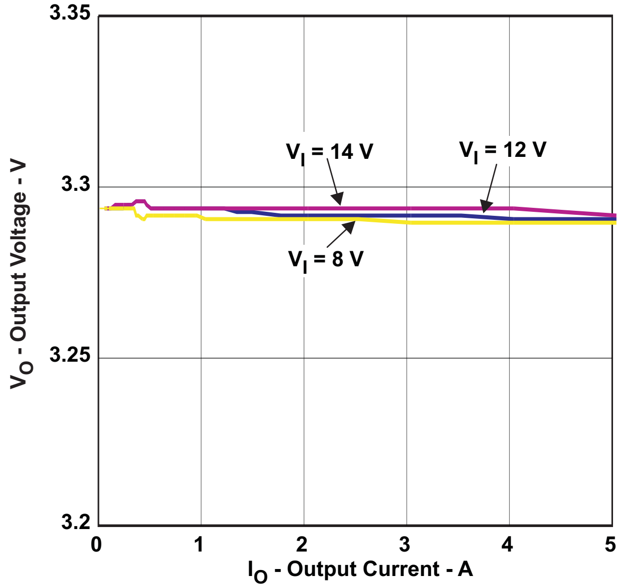


Figure 41. 3.3-V Load Regulation

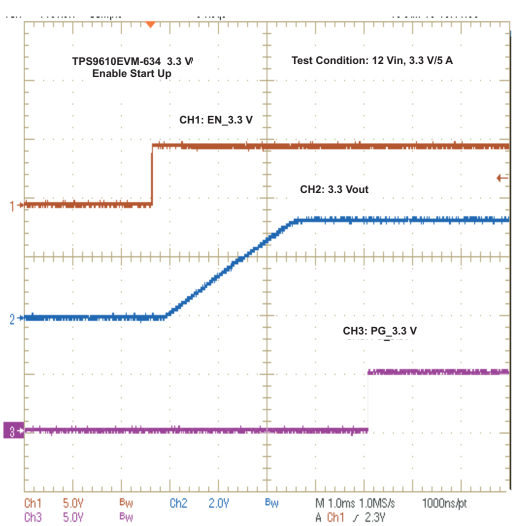


Figure 42. 3.3-V Enable Turnon

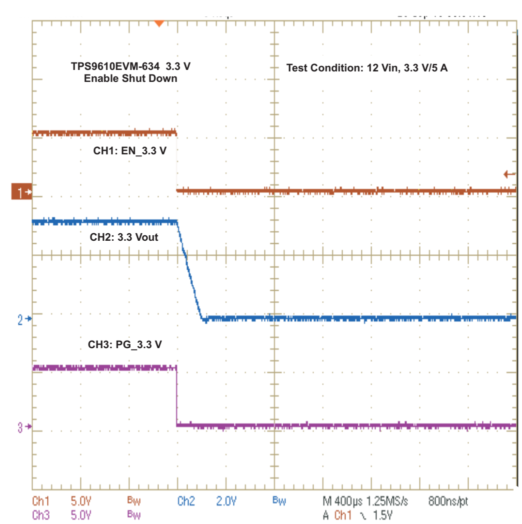


Figure 43. 3.3-V Enable Turnoff

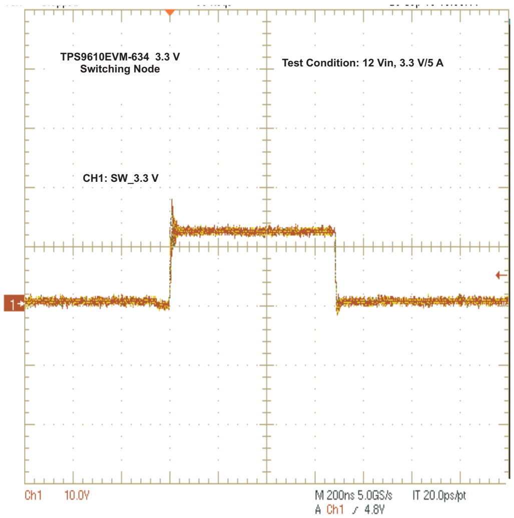


Figure 44. 3.3-V Switching Node

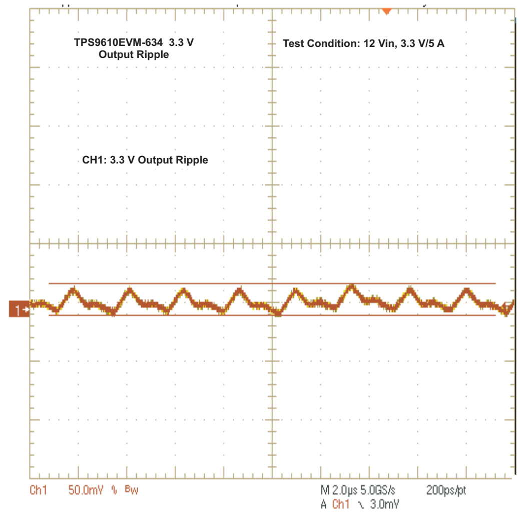


Figure 45. 3.3-V Vo Ripple

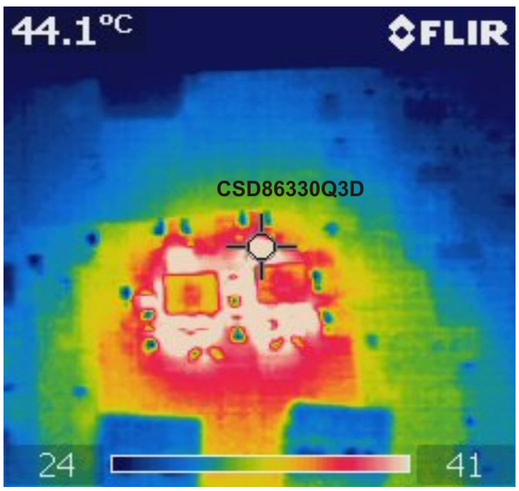


Figure 46. 5-V/3.3-V TOP Board

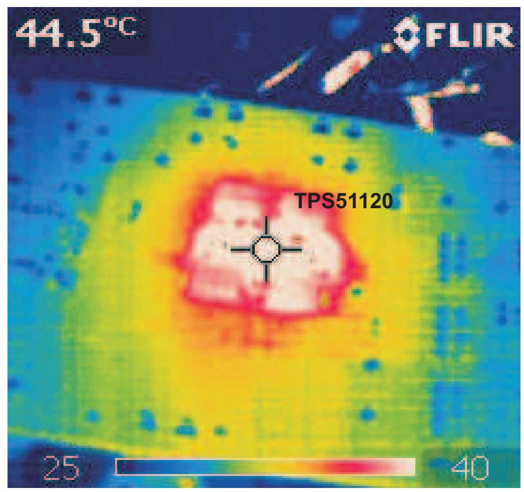


Figure 47. 5-V/3.3-V Bottom Board

Test condition: 12 Vin, 5 V/5 A and 3.3 V/5 A, no airflow

8.4 1.8-V DDR/1.05-V CPU VTT

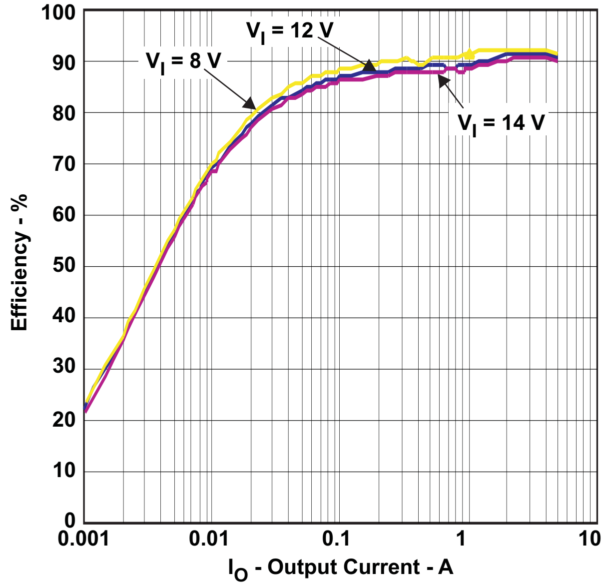


Figure 48. 1.8-V Efficiency

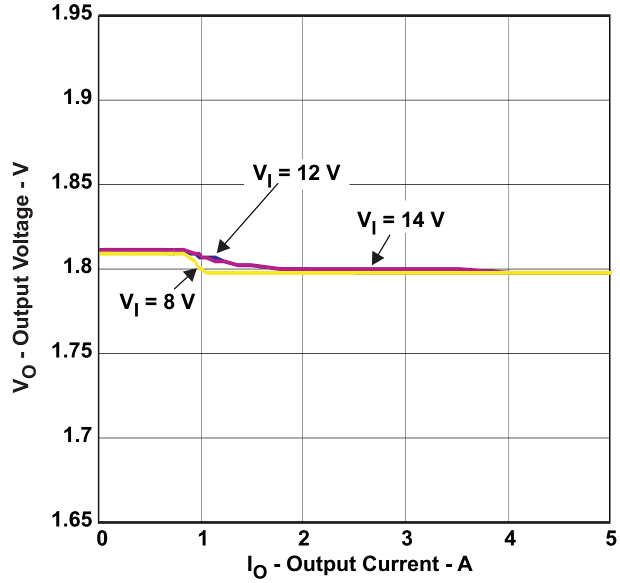


Figure 49. 1.8-V Load Regulation

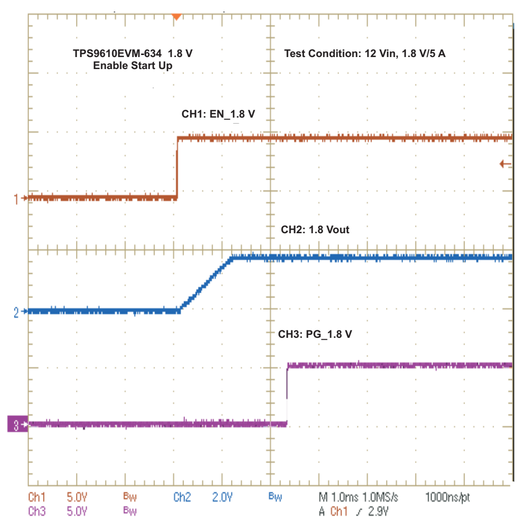


Figure 50. 1.8-V Enable Turnon

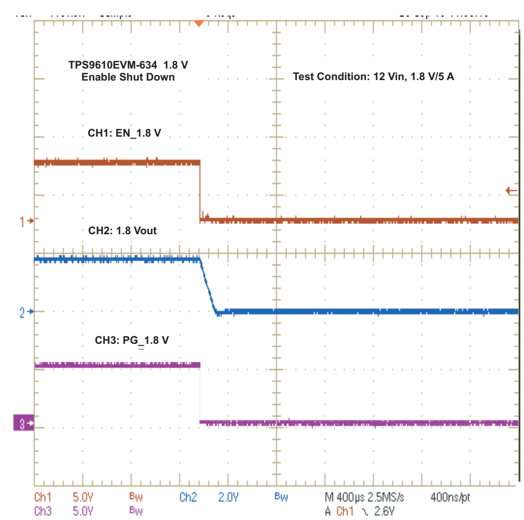


Figure 51. 1.8-V Enable Turnoff

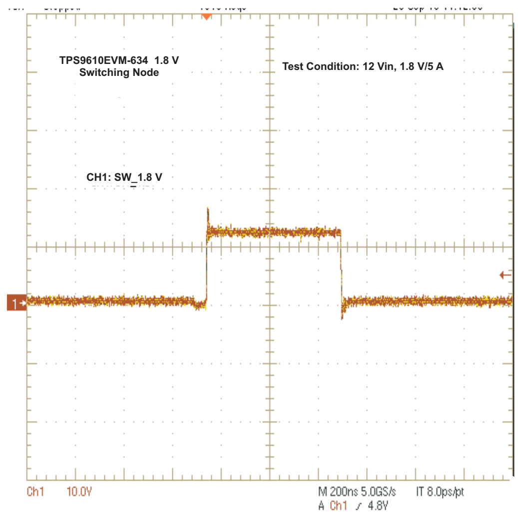


Figure 52. 1.8-V Switching Node

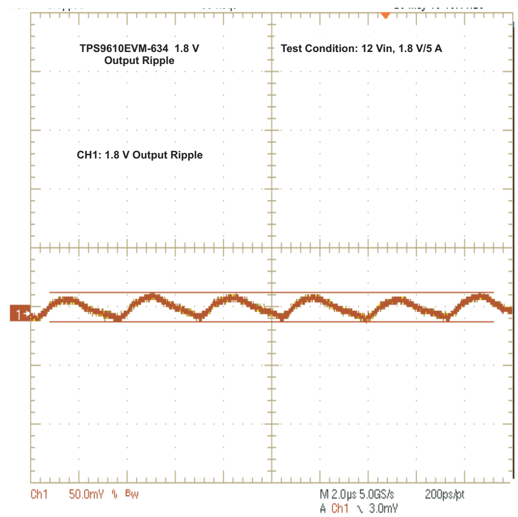


Figure 53. 1.8-V Vo Ripple

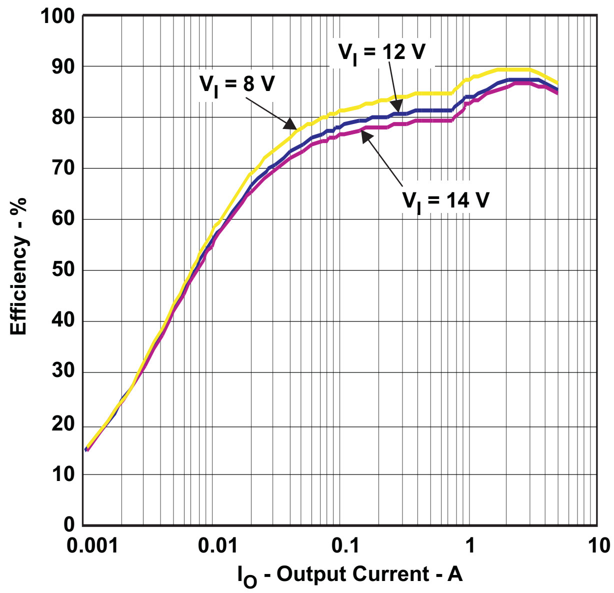


Figure 54. 1.05-V Efficiency

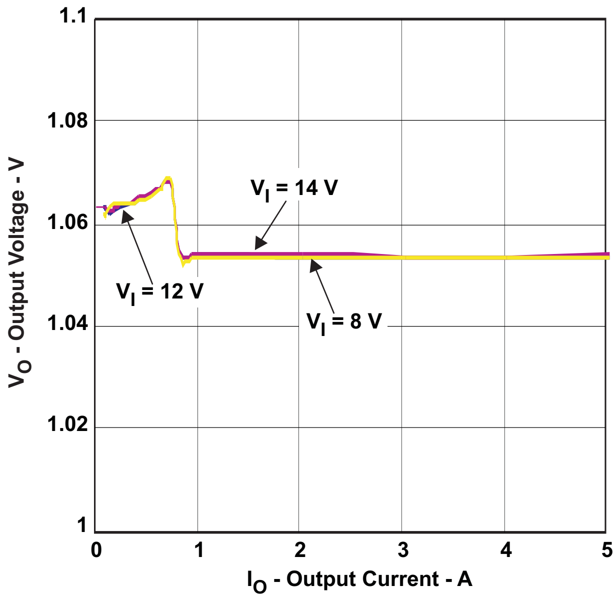


Figure 55. 1.05-V Load Regulation

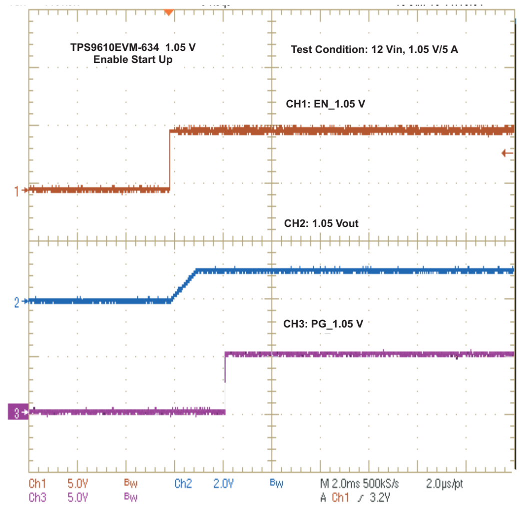


Figure 56. 1.05-V Enable Turnon

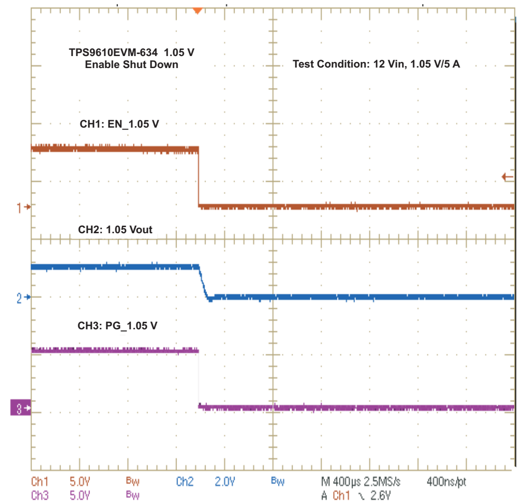


Figure 57. 1.05-V Enable Turnoff

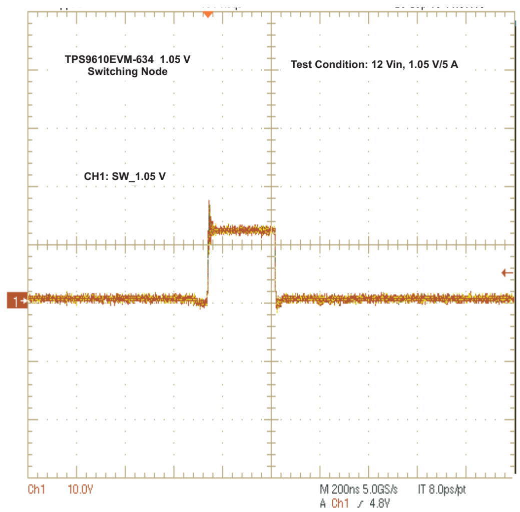


Figure 58. 1.05-V Switching Node

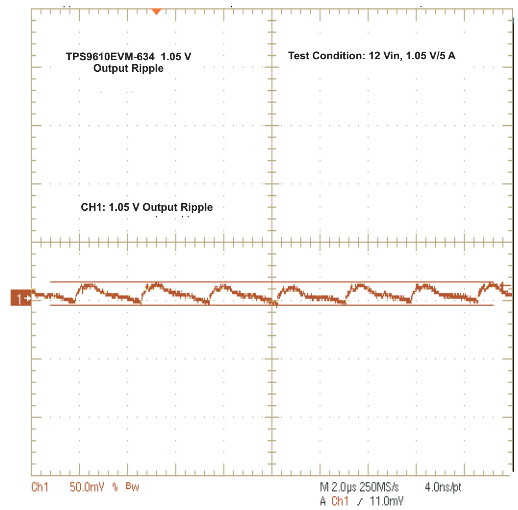


Figure 59. 1.05-V Vo Ripple

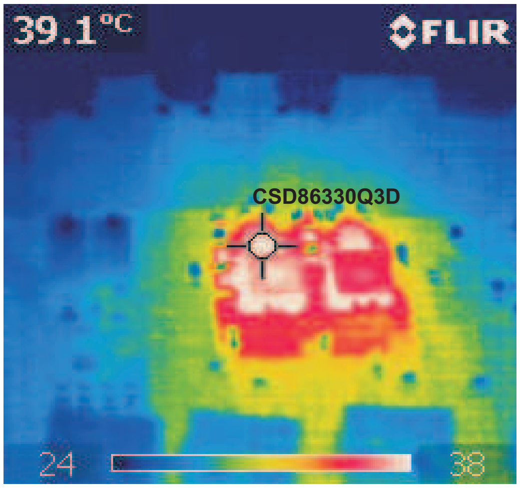


Figure 60. 1.8-V/1.05-V Top Board

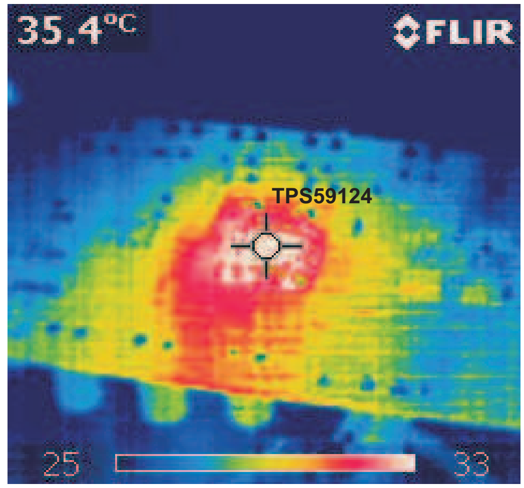


Figure 61. 1.8-V/1.05-V Bottom Board

Test condition: 12 Vin, 1.8 V/5 A and 1.05 V/5 A, no airflow

8.5 1.2-V IOH

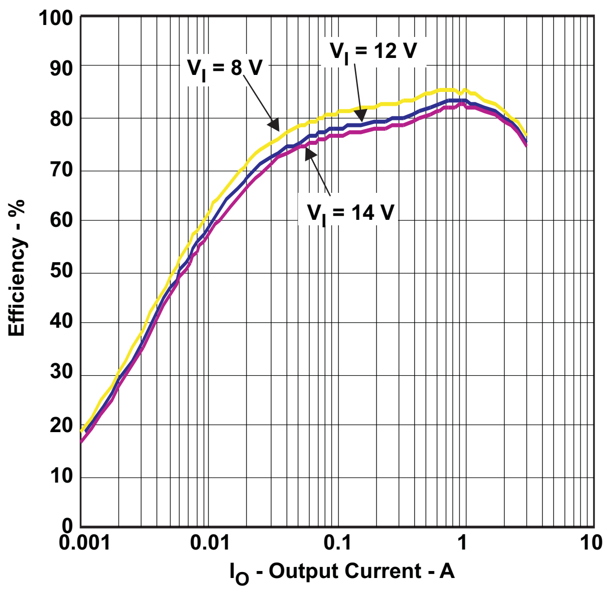


Figure 62. 1.2-V Efficiency

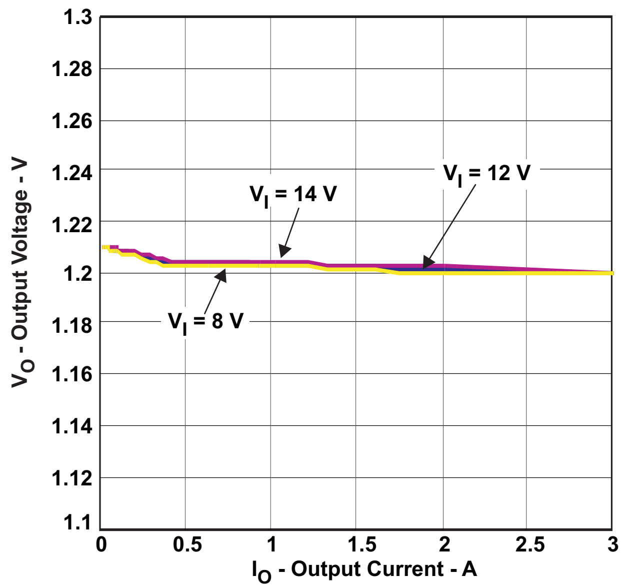


Figure 63. 1.2-V Load Regulation

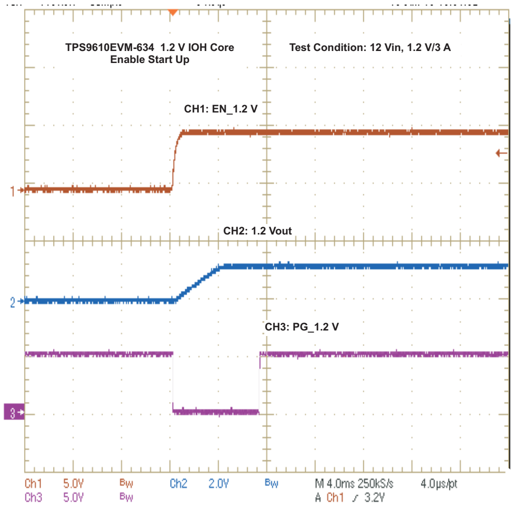


Figure 64. 1.2-V Enable Turnon

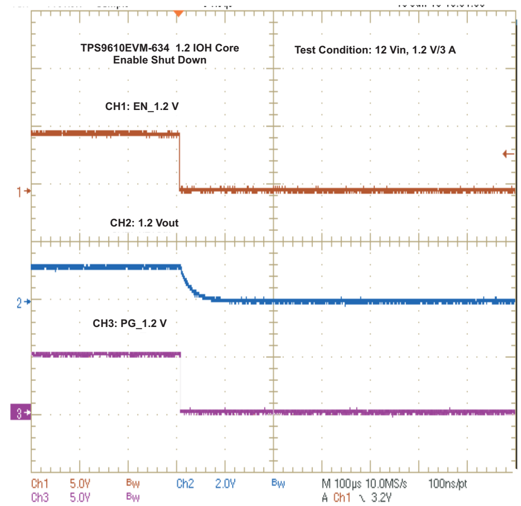


Figure 65. 1.2-V Enable Turnoff

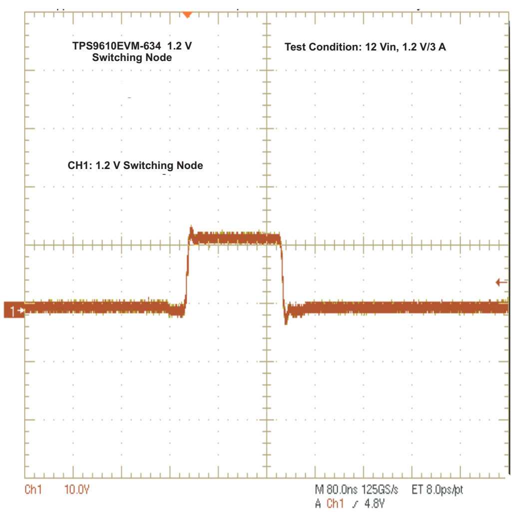


Figure 66. 1.2-V Switching Node

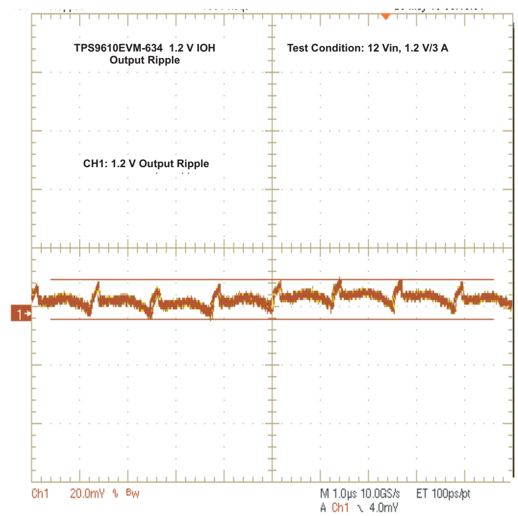


Figure 67. 1.2-V Vo Ripple

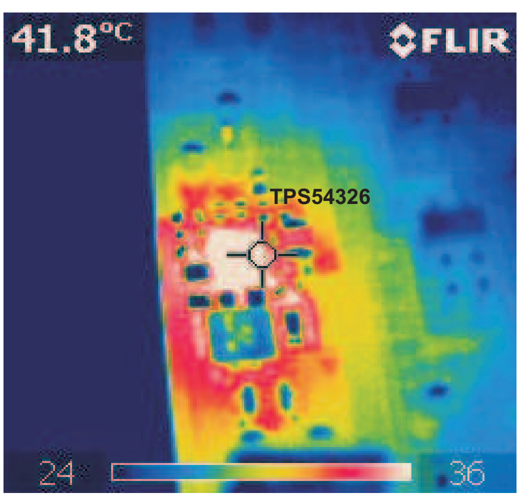


Figure 68. 1.2-V Top Board
Test Condition: 12 Vin, 1.2 V/3 A, No Airflow

9 EVM Assembly Drawings and PCB Layout

The following figures (Figure 69 through Figure 74) show the design of the TPS59610EVM-634 printed circuit board. The EVM has been designed using 4 Layers circuit board with 2oz copper on outside layers.

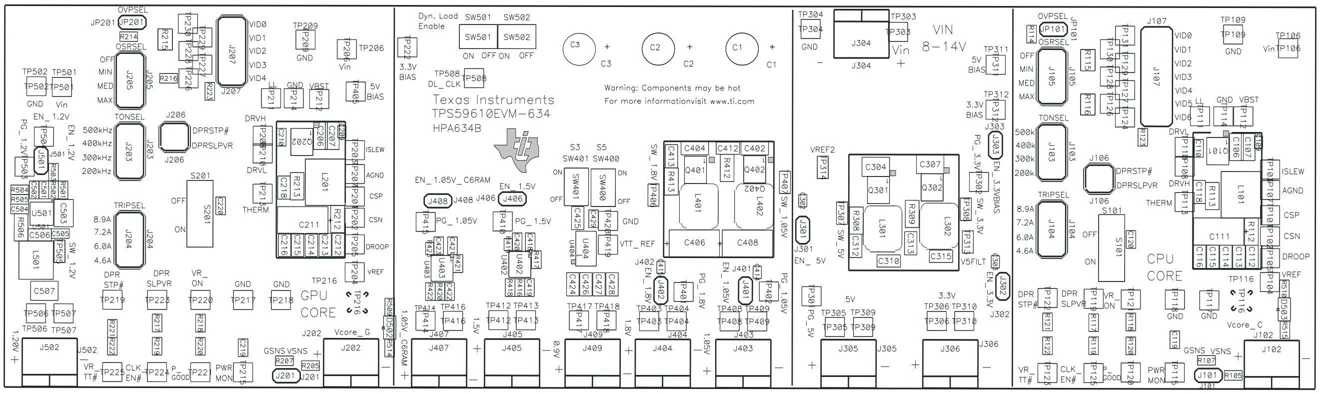


Figure 69. TPS59610EVM-634 Top Layer Assembly Drawing, Top View

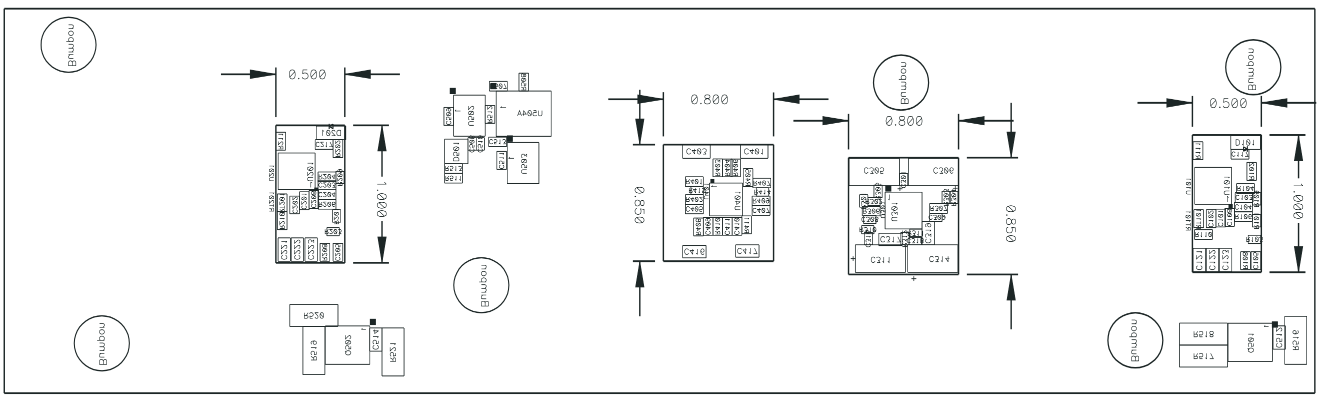


Figure 70. TPS59610EVM-634 Bottom Assembly Drawing, Bottom View

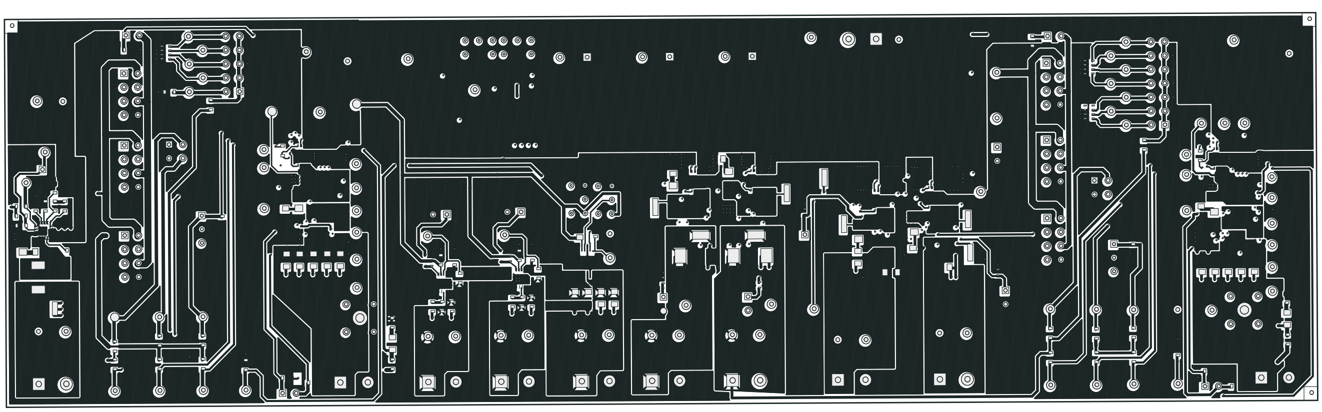


Figure 71. TPS59610EVM-634 Top Copper, Top View

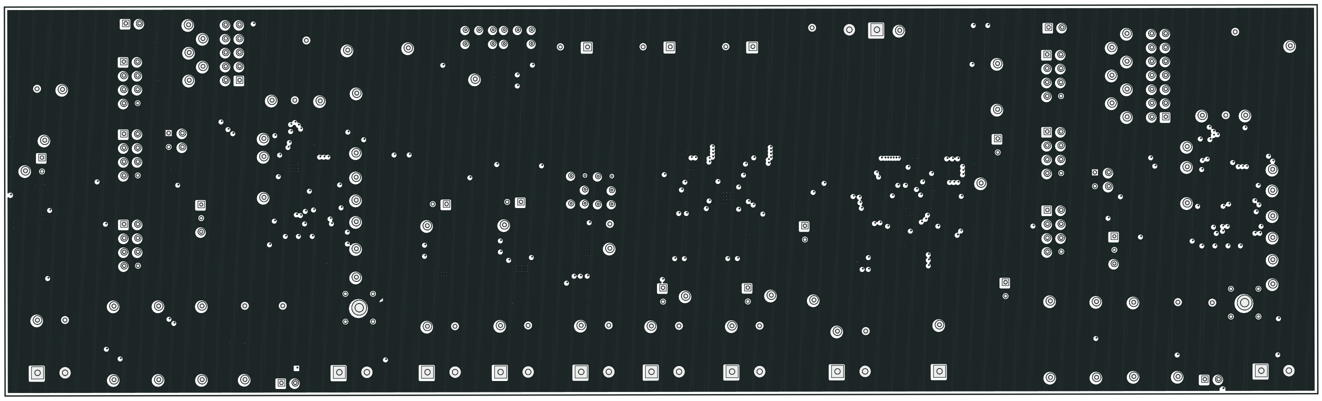


Figure 72. TPS59610EVM-634 Internal Layer 2, Top View

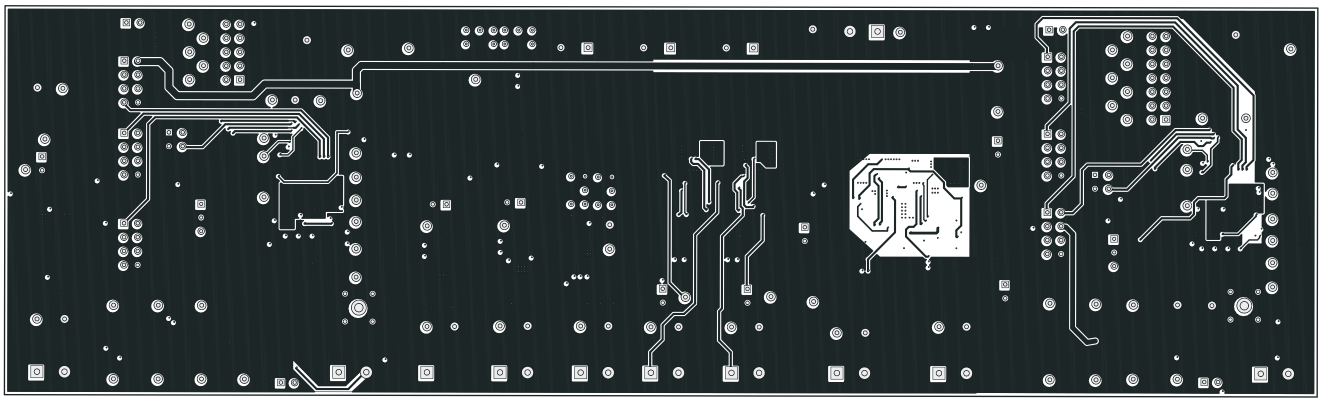


Figure 73. TPS59610EVM-634 Internal Layer 3, Top View

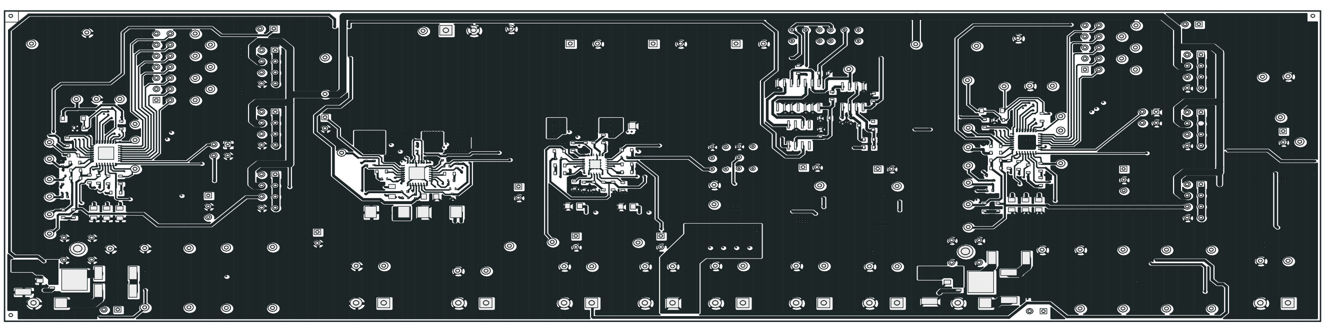


Figure 74. TPS59610EVM-634 Bottom Layer, Bottom View

10 Bill of Materials

Table 17 shows the EVM major components list according to the schematic shown in Figure 2 through Figure 6.

Table 17. Bill of Materials

Qty	RefDes	Description	MFR	Part Number
3	C1, C2, C3	Capacitor, Aluminum, 330uF, 16V, 20%, –40-85°C	Panasonic-ECG	ECA-1CM331B
4	C101, C102, C201, C202	Capacitor, Ceramic, 100pF, 50V, C0G, 10%, 0603	STD	STD
6	C103, C108, C110, C203, C208, C210	Capacitor, Ceramic, 1uF, 16V, X7R, 20%, 0603	STD	STD
2	C104, C204	Capacitor, Ceramic, 68pF, 50V, C0G, 10%, 0603	STD	STD
8	C106, C107, C206, C207, C401– C404	Capacitor, Ceramic, 10uF, 25V, X5R, 20%, 1206	STD	STD
3	C109, C209, C301	Capacitor, Ceramic, 1000pF, 50V, X7R, 20%, 0402	STD	STD
2	C111, C211	Capacitor, Aluminum, 220uF, 2V, 20%, 9mohm, 7343	Panasonic-ECG	EEF-SX0D221R
20	C112–C116, C212–C216, C310, C315, C317, C319, C416, C417, C424, C426–C428,	Capacitor, Ceramic, 10uF, 6.3V, X5R, 20%, 0805	STD	STD
2	C117, C217	Capacitor, Ceramic, 10uF, 6.3V, X5R, 20%, 0603	STD	STD
1	C118	Capacitor, Ceramic, 1800pF, 50V, X7R, 20%, 0805	STD	STD
5	C119, C120, C219, C220, C502	Capacitor, Ceramic, 0.01uF, 50V, X7R, 20%, 0603	STD	STD
5	C218, C312, C313, C412, C413	Capacitor, Ceramic, 1000pF, 50V, X7R, 20%, 0805	STD	STD
3	C304, C307, C503	Capacitor, Ceramic, 22uF, 16V, X5R, 20%, 1210	STD	STD
2	C305, C306	Capacitor, Tant cap, 33uF, 16V, 0.045ohms, 20%, 7343D	KEMET	T520V336M016ATE045
3	C308, C309, C510	Capacitor, Ceramic, 0.1uF, 16V, X7R, 20%, 0402	STD	STD
2	C311, C314	Capacitor, Tant cap, 330uF, 6.3V, 0.010ohms, 20%, 7343D	KEMET	T530D337M006ATE010
2	C316, C318	Capacitor, Ceramic, 1uF, 16V, X5R, 20%, 0402	STD	STD
4	C405, C407, C429, C505	Capacitor, Ceramic, 0.1uF, 25V, X7R, 20%, 0603	STD	STD
2	C406, C408	Capacitor, SP cap, 330uF, 2.5V, 0.015ohms, 20%, 7343D	Panasonic-ECG	EEF-CX0E331R
1	C409	Capacitor, Ceramic, 4.7uF, 10V, X5R, 20%, 0603	STD	STD
7	C410, C420, C423, C501, C509, C511, C513	Capacitor, Ceramic, 1uF, 16V, X7R, 20%, 0603	STD	STD
1	C411	Capacitor, Ceramic, 22pF, 50V, C0G, 20%, 0603	STD	STD
4	C418, C419, C421, C422	Capacitor, Ceramic, 4.7uF, 6.3V, X5R, 20%, 0603	STD	STD
1	C425	Capacitor, Ceramic, 4.7uF, 6.3V, X5R, 20%, 0805	STD	STD
1	C504	Capacitor, Ceramic, 22nF, 16V, X7R, 20%, 0603	STD	STD
1	C507	Capacitor, Ceramic, 47uF, 6.3V, X5R, 20%, 1210	STD	STD
1	C508	Capacitor, Ceramic, 0.01uF, 25V, X7R, 20%, 0402	STD	STD
2	D101, D201	Diode, Schottky, 0.5A, 30V, SOD-123,	On Semi	MBR0530T
1	D501	Diode, Schottky, 200mA, 30V, SOT-23,	Vishay-Liteon	BAT54-V-GS08
2	D502, D503	Diode, LED, Green Clear, 20mcd, 0.079x0.049	Lite On	LTST-C170GKT
2	L101, L201	Inductor, SMT, 1uH, 11.1A , 7.81mohm, 0.256" x 0.280"	TDK	SPM6530T-1R0M120
2	L301, L302	Inductor, SMT, 4.7uH, 6.0A, 25mohm, 6.8mm x 6.8mm	Coiltronics	HCP0704-4R7-R
2	L401, L402	Inductor, SMT, 2.2uH, 10A, 13.6mohm, 0.255" x 0.270"	Vishay	IHLP2525EZER2R2M01
1	L501	Inductor, SMT, 1.5uH, 5.5A, 40.4mohm, 0.204" x 0.216"	Vishay	IHLP2020CZER1R5M11
6	Q101, Q201, Q301,Q302, Q401, Q402	MOSFET, Synchronous Buck NexFET Power Block SON 3.3 x 3.3mm	TI	CSD86330Q3D
2	Q501, Q502	MOSFET, Nchan, 25V, 31A, 2.5mohm, QFN5X6mm	TI	CSD16407Q5
4	R101, R103, R201, R203	Resistor, Chip, 475, 1/16W, 1%, 0402	STD	STD
15	R102, R117–R120, R202, R217–R220, R503, R505, R507, R508, R512	Resistor, Chip, 10k, 1/16W, 1%, 0603	STD	STD
2	R104, R204	Resistor, Chip, 45.3k, 1/16W, 1%, 0603	STD	STD
4	R105, R107, R205, R207	Resistor, Chip, 10, 1/16W, 1%, 0603	STD	STD
2	R514, R515	Resistor, Chip, 100, 1/16W, 1%, 0603	STD	STD

Table 17. Bill of Materials (continued)

Qty	RefDes	Description	MFR	Part Number
2	R106, R206	Resistor, Chip, 6.19k, 1/16W, 1%, 0603	STD	STD
3	R109, R209, R305	Resistor, Chip, 0, 1/16W, 5%, 0402	STD	STD
2	R110, R210	Resistor, Chip, 2.00k, 1/16W, 1%, 0603	STD	STD
2	R111, R211	Resistor, Chip, 5.90, 1/16W, 1%, 0603	STD	STD
2	R402, R409	Resistor, Chip, 0, 1/16W, 1%, 0603	STD	STD
2	R112, R212	Resistor, Metal Film, 0.003, 1/4W, 1%, 1206	STD	STD
6	R113, R213, R308, R309, R412, R413	Resistor, Metal Film, 1, 1/4W, 5%, 1206	STD	STD
2	R114, R214	Resistor, Chip, 78.7k, 1/16W, 1%, 0603	STD	STD
3	R115, R116, R215	Resistor, Chip Array, 100k, 62.5mW, 5%, 612	Yageo	TC164-JR-07100KL
4	R121, R122, R221, R222	Resistor, Chip, 1.00k, 1/16W, 1%, 0603	STD	STD
2	R123, R223	Resistor, Chip, 1, 1/16W, 5%, 0603	STD	STD
7	R216, R401, R407, R417, R421, R504, R513	Resistor, Chip, 100k, 1/16W, 1%, 0603	STD	STD
8	R301, R302, R303, R304, R414, R415, R419, R423	Resistor, Chip, 10.0k, 1/16W, 1%, 0402	STD	STD
2	R306, R307	Resistor, Chip, 2.05, 1/16W, 5%, 0603	STD	STD
2	R310, R311	Resistor, Chip, 3.48k, 1/16W, 1%, 0402	STD	STD
1	R312	Resistor, Chip, 5.11, 1/16W, 5%, 0402	STD	STD
1	R403	Resistor, Chip, 102k, 1/16W, 1%, 0603	STD	STD
2	R404, R406	Resistor, Chip, 75.0k, 1/16W, 1%, 0603	STD	STD
1	R405	Resistor, Chip, 28.7k, 1/16W, 1%, 0603	STD	STD
1	R416	Resistor, Chip, 6.81k, 1/16W, 1%, 0603	STD	STD
2	R408, R411	Resistor, Chip, 3.48k, 1/16W, 1%, 0603	STD	STD
1	R410	Resistor, Chip, 3.3, 1/16W, 5%, 0603	STD	STD
2	R418, R422	Resistor, Chip, 7.87k, 1/16W, 1%, 0603	STD	STD
1	R420	Resistor, Chip, 2.49k, 1/16W, 1%, 0603	STD	STD
1	R501	Resistor, Chip, 68.1, 1/16W, 1%, 0603	STD	STD
1	R502	Resistor, Chip, 5.62k, 1/16W, 1%, 0603	STD	STD
2	R509, R510	Resistor, Chip, 330, 1/16W, 1%, 0603	STD	STD
1	R511	Resistor, Chip, 8.06k, 1/16W, 1%, 0603	STD	STD
2	R516, R521	Resistor, Chip, 0.001, 2W, 1%, 2512	STD	STD
4	R517–R520	Resistor, Chip, 0.100, 2W, 1%, 2512	STD	STD
2	RT101, RT210	NTC Thermistor, 150k, 0603, 5%	Panasonic-ECG	ERTJ1VV154J
2	U101, U210	IC, Single phase, D-CAP Synchronous Buck Controller, QFN-32	TI	TPS59610RHB
1	U301	IC, Dual Synchronous PWM Controller, QFN-32	TI	TPS51120RHB
1	U401	IC, Dual Synchronous Step down Controller, QFN-24	TI	TPS59124RGE
2	U402, U403	IC, 1.5A LDO Regulator with soft start, SON-10	TI	TPS74801DRC
1	U404	IC, High performance DDRI&II 3A LDO &buffered reference, MSOP-Power PAD	TI	TPS51100DGQ
1	U501	IC, 4.5-18V Input, 3A Step down Regulator with integrated Switcher, QFN-16	TI	TPS54326RGT
1	U502	IC, Timer, Lower power CMOS, SO-8	TI	TLC555CD
1	U503	IC, Dual 4A high speed low side MOSFET driver, SO-8	TI	UCC37324DR
1	U504	IC, Quadruple 2 Input positive And Gates, SO-14	TI	SN74HC08D

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 8 V to 14 V and the output voltage range of 0.9 V to 5 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

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REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited
(address) 24-1, Nishi-Shinjuku 6 chome, Shinjuku-ku, Tokyo, Japan

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日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿６丁目２４番１号
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EVALUATION BOARD/KIT/MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

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