NCV8141

Linear Regulator - ENABLE, RESET, Watchdog

5.0 V, 500 mA

The NCV8141 is a linear regulator suited for microprocessor applications in automotive environments.

This ON Semiconductor part provides the power for the microprocessors along with many of the control functions needed in today's computer based systems. Incorporating all of these features saves both cost, and board space.

The NCV8141 provides a low sleep mode current as compared to the CS8141. Consult your local sales representative for a low sleep mode current version of the CS8140.

Features

- 5.0 V ± 3.0%, 500 mA Output Voltage
- Lower Quiescent Current
- Improved Filtering for /RESET Functionality
- μP Compatible Control Functions
  - Watchdog
  - $\overline{\text{RESET}}$
  - ENABLE
- Low Dropout Voltage (1.25 V @ 500 mA)
- Low Quiescent Current (7.0 mA @ 500 mA)
- Low Noise, Low Drift
- Low Current SLEEP Mode 50 μA (max)
- Fault Protection
  - Thermal Shutdown
  - Short Circuit
  - 60 V Peak Transient Voltage
- These are Pb−Free Devices
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes

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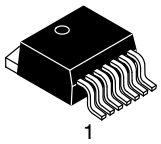
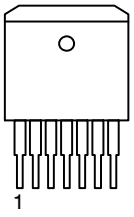
MARKING DIAGRAM



D²PAK−7
DPS SUFFIX
CASE 936AB

A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

PIN CONNECTIONS



Tab = GND
Pin 1. V_{IN}
2. ENABLE
3. $\overline{\text{RESET}}$
4. GND
5. Delay
6. WDI
7. V_{OUT}

ORDERING INFORMATION

Device	Package	Shipping†
NCV8141D2TG	D²PAK (Pb−Free)	50 Units/Rail
NCV8141D2TR4G	D²PAK (Pb−Free)	750/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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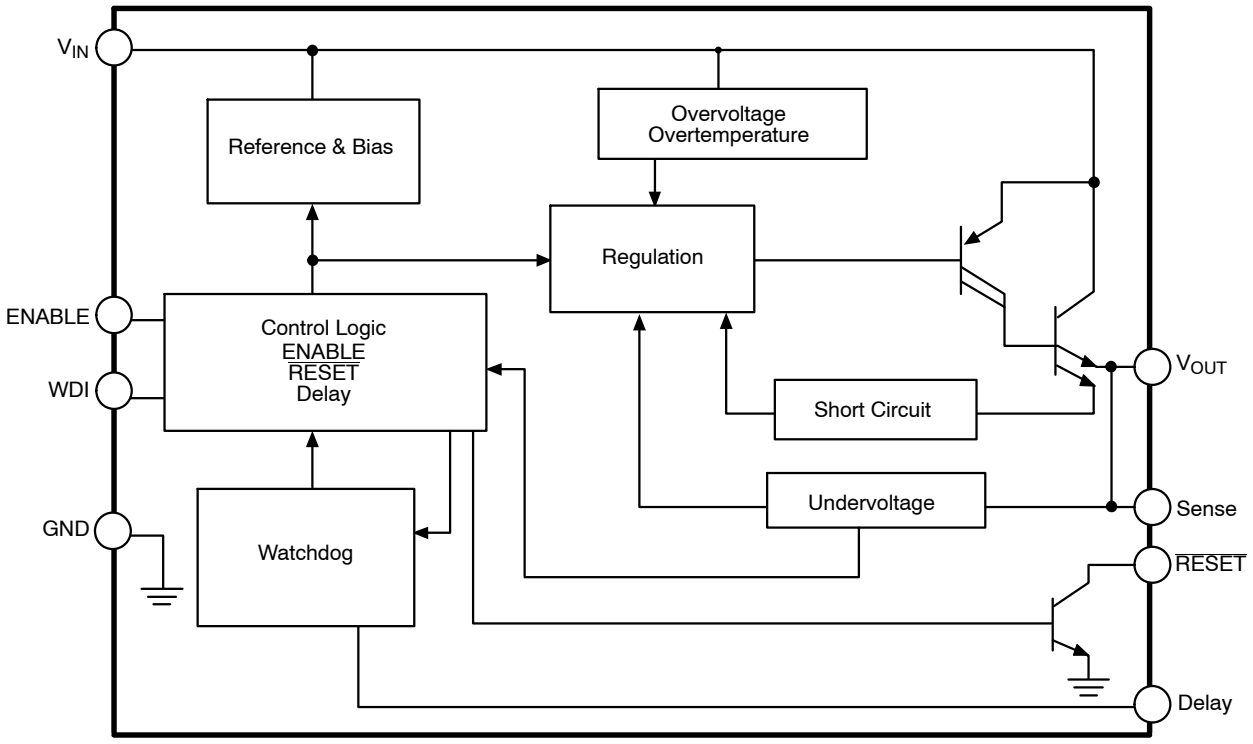


Figure 1. Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Symbol	Function
1	V_{IN}	Supply voltage to IC, usually direct from the battery.
2	ENABLE	CMOS compatible logical input. V_{OUT} is disabled when ENABLE is LOW and WDI is invalid.
3	$\overline{\text{RESET}}$	CMOS compatible output lead. $\overline{\text{RESET}}$ goes low whenever V_{OUT} drops 4.5% below its typical value for more than 2.0 μs or WDI signal falls below the watchdog threshold frequency.
4	GND	Ground Connection.
5	Delay	Timing capacitor for Watchdog and $\overline{\text{RESET}}$ functions.
6	WDI	CMOS compatible input lead. The Watchdog function monitors the falling edge of the incoming digital pulse train. The signal is usually generated by the system microprocessor.
7	V_{OUT}	Regulated output voltage, 5.0 V (typ).

MAXIMUM RATINGS

Rating	Value	Unit
Input Operating Range	−0.5 to 26	V
Peak Transient Voltage (46 V Load Dump @ 14 V V_{BAT})	60	V
Electrostatic Discharge (Human Body Model)	4.0	kV
WDI Input Signal Range	−0.3 to 7.0	V
Internal Power Dissipation	Internally Limited	–
Junction Temperature Range (T_J)	−40 to +150	°C
Storage Temperature Range	−65 to +150	°C
ENABLE	−0.3 to V_{IN}	V
Package Thermal Resistance, D^2PAK 7−Pin Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$	 1.5 10−50†	 °C/W °C/W
Lead Temperature Soldering: Reflow (SMD styles only) (Note 1)	225 peak (Note 2)	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Depending on thermal properties of substrate $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$.

1. 60 seconds max above 183°C.
2. −5.0°C/+0°C allowable conditions.

ELECTRICAL CHARACTERISTICS ($7.0 \le V_{IN} \le 26$ V, $5.0\text{ mA} \le I_{OUT} \le 500$ mA, $-40°C \le T_J \le 150°C$, $-40°C \le T_A \le 125°C$, unless otherwise noted.) (Note 3)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output Stage (V_{OUT})					
Output Voltage, V_{OUT}	$7.0\text{ V} \le V_{IN} \le 26$ V, $5.0\text{ mA} < I_{OUT} < 500$ mA	4.85	5.0	5.15	V
Dropout Voltage ($V_{IN} - V_{OUT}$)	$I_{OUT} = 500$ mA	–	1.25	1.50	V
Line Regulation	$I_{OUT} = 50$ mA, $7.0\text{ V} \le V_{IN} \le 26$ V,	–	5.0	25	mV
Load Regulation	$V_{IN} = 14$ V, $50\text{ mA} \le I_{OUT} \le 500$ mA	–	5.0	80	mV
Output Impedance, R_{OUT}	500 mA DC and 10 mA AC, $100\text{ Hz} \le f \le 10$ kHz	–	200	–	mΩ
Quiescent Current, (I_Q) Active Mode Sleep Mode	 $0 \le I_{OUT} \le 500$ mA, $7.0\text{ V} \le V_{IN} \le 26$ V $I_{OUT} = 0$ mA, $V_{IN} = 13$ V, ENABLE = 0 V	 – –	 7.0 25	 15 50	 mA μA
Ripple Rejection	$7.0\text{ V} \le V_{IN} \le 17$ V, $I_{OUT} = 250$ mA, f = 120 Hz	60	75	–	dB
Current Limit	$V_{IN} = 7.0$ V, $V_{OUT} = 4.5$ V	600	1200	2000	mA
Thermal Shutdown	Guaranteed by Design	150	180	–	°C
Overvoltage Shutdown	$V_{OUT} < 1.0$ V	30	34	38	V
ENABLE					
Threshold HIGH LOW	 $V_{OUT} \ge 0.5$ V, ($V_{OUT(ON)}$) $V_{OUT} < 0.5$ V, ($V_{OUT(OFF)}$)	 – 3.5	 4.05 3.95	 4.50 –	 V V
Input Current HIGH LOW	 ENABLE = 5.0 V ENABLE = 0 V	 – −1.0	 35 0	 75 1.0	 μA μA
Threshold Hysteresis	(HIGH − LOW)	–	80	–	mV

3. To observe safe operating junction temperatures, low duty cycle pulse testing is used in tests where applicable.

ELECTRICAL CHARACTERISTICS (continued) ($7.0 \le V_{IN} \le 26$ V, 5.0 mA $\le I_{OUT} \le 500$ mA, $-40°C \le T_J \le 150°C$, $-40°C \le T_A \le 125°C$, unless otherwise noted.) (Note 4)

Characteristic	Test Conditions	Min	Typ	Max	Unit
$\overline{\text{RESET}}$					
Threshold HIGH $V_{R(HI)}$	V_{OUT} Increasing	4.65	4.90	V_{OUT} – 0.05	V
Threshold LOW $V_{R(LOW)}$	V_{OUT} Decreasing	4.50	4.70	4.90	V
Threshold Hysteresis (V_{RH})	(HIGH – LOW)	150	200	250	mV
$\overline{\text{RESET}}$ Output Leakage $\overline{\text{RESET}}$ = HIGH	$V_{OUT} \ge V_{R(HI)}$	–	–	25	μA
Output Voltage Low ($V_{L(LOW)}$)	$1.0 \text{ V} \le V_{OUT} \le V_{R(LOW)}$, R_P = 2.7 kΩ (Note 5)	–	0.1	0.4	V
Output Voltage Low (V_{Rpeak})	V_{OUT}, Power up, Power down	–	0.6	1.0	V
Delay Time t_{POR}	C_{DELAY} = 0.1 μF	30	47.5	65	ms
Delay Time $t_{WDI(\overline{RESET})}$	C_{DELAY} = 0.1 μF	0.5	1.0	1.5	ms
Watchdog					
Input Voltage High	–	2.0	–	–	V
Input Voltage Low	–	–	–	0.8	V
Input Current	$WDI \le V_{OUT}$	–	0	10	μA
Threshold Frequency f_{WDI}	C_{DELAY} = 0.1 μF	64	77	105	Hz

4. To observe safe operating junction temperatures, low duty cycle pulse testing is used in tests where applicable.
5. R_P is connected to $\overline{\text{RESET}}$ and V_{OUT}.

TYPICAL PERFORMANCE CHARACTERISTICS

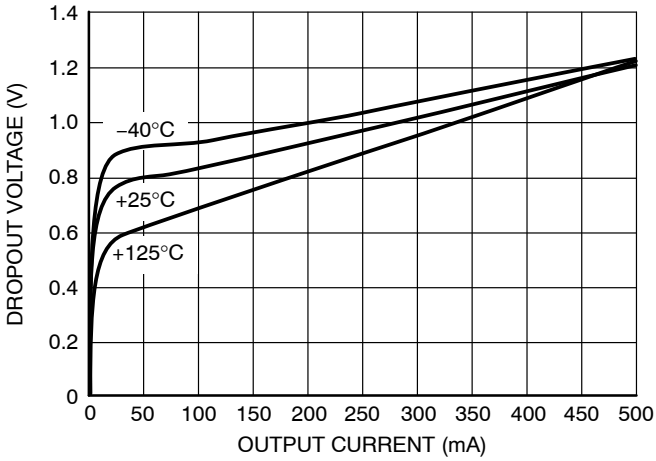


Figure 2. Dropout Voltage vs. Output Current over Temperature

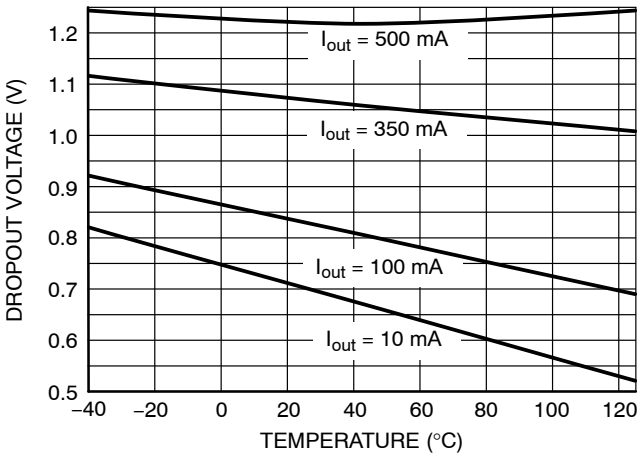


Figure 3. Dropout Voltage vs. Temperature

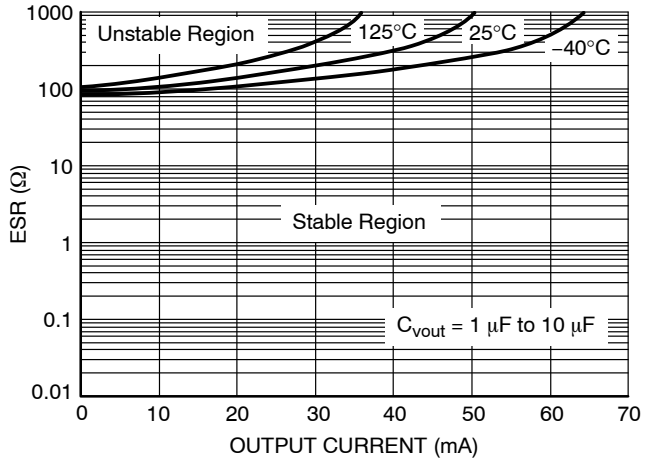


Figure 4. Output Stability

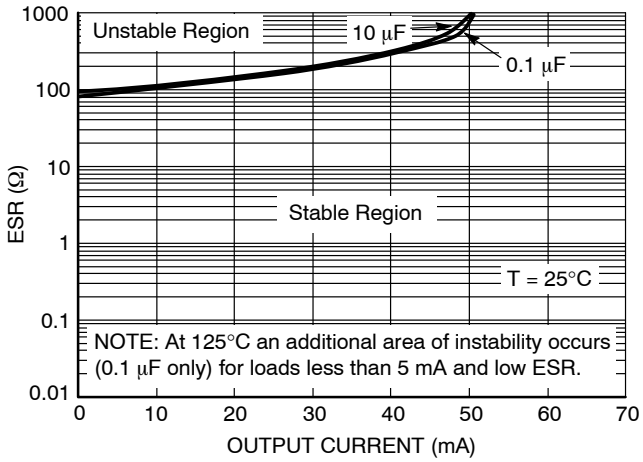


Figure 5. Output Stability with Capacitor Change

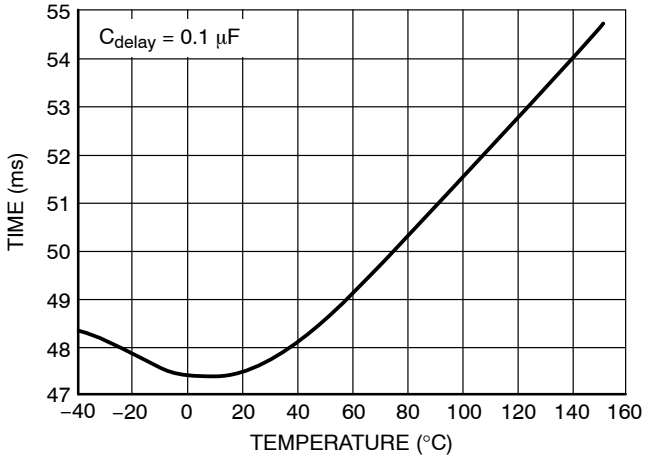


Figure 6. Delay Time

DEFINITION OF TERMS

Dropout Voltage: The input−output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak−to−peak input ripple voltage to the peak−to−peak output ripple voltage.

Current Limit: Peak current that can be delivered to the output.

CIRCUIT DESCRIPTION

The NCV8141 is a 5.0 V Watchdog Regulator with protection circuitry and three logic control functions that allow a microprocessor to control its own power supply. The NCV8141 is designed for use in automotive, switch mode power supply post regulator, and battery powered systems.

Basic regulator performance characteristics include a low noise, low drift, 5.0 V ±3.0% precision output voltage with low dropout voltage (1.25 V @ I_{OUT} = 500 mA) and low quiescent current (7.0 mA @ I_{OUT} = 500 mA). On board short circuit, thermal, and overvoltage protection make it possible to use this regulator in particularly harsh operating environments.

The Watchdog logic function monitors an input signal (WDI) from the microprocessor or other signal source. When the signal frequency goes below the externally programmable limit, a $\overline{\text{RESET}}$ signal is generated ($\overline{\text{RESET}}$). Proper operation has been verified at a frequency up to 100 kHz. No abnormal $\overline{\text{RESET}}$ signals will occur with frequencies lower than 100 kHz and the maximum Threshold Frequency (96 Hz). An external capacitor (C_{DELAY}) programs the watchdog frequency limit as well as the power on reset (POR) and $\overline{\text{RESET}}$ delay.

The $\overline{\text{RESET}}$ function is activated by any of three conditions: the watchdog signal moves outside of its preset limits; the output voltage drops out of regulation by more than 4.5%; or the IC is in its power up sequence. The $\overline{\text{RESET}}$ signal is independent of V_{IN} and reliable down to V_{OUT} = 1.0 V.

In conjunction with the Watchdog, the ENABLE function controls the regulator's power consumption. The NCV8141's output stage and its attendant circuitry are enabled by setting the ENABLE lead high. The regulator goes into sleep mode when the ENABLE lead goes low and the watchdog signal moves outside its preset limit. This unique combination of control functions in the NCV8141 gives the microprocessor control over its own power down sequence: i.e. it gives the microprocessor the flexibility to perform housekeeping functions before it powers down.

VOLTAGE REFERENCE AND OUTPUT CIRCUITRY

Precision Voltage Reference

The regulated output voltage depends on the precision band gap voltage reference in the IC. By adding an error amplifier into the feedback loop, the output voltage is maintained within ±3.0% over temperature and supply variation.

Output Stage

The composite PNP−NPN output structure (Figure 7) provides 500 mA (min) of output current while maintaining a low drop out voltage (1.25 V) and drawing little quiescent current (7.0 mA).

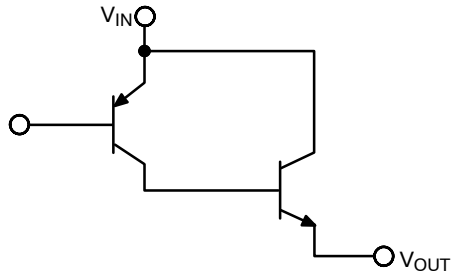


Figure 7. Composite Output Stage of the NCV8141

The NPN pass device prevents deep saturation of the output stage which in turn improves the IC's efficiency by preventing excess current from being used and dissipated by the IC.

Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 8).

If the input voltage rises above 30 V (e.g. load dump), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients.

Using an emitter sense scheme, the amount of current through the NPN pass transistor is monitored. Feedback circuitry insures that the output current never exceeds a preset limit.

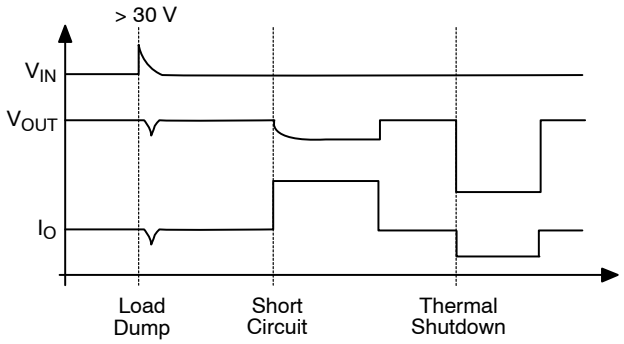


Figure 8. Typical Circuit Waveforms for Output Stage Protection

Should the junction temperature of the power device exceed 180°C (typ), the power transistor is turned off. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the IC.

REGULATOR CONTROL FUNCTIONS

The NCV8141 differs from all other linear regulators in its unique combination of control features.

Watchdog and ENABLE Function

V_{OUT} is controlled by the logic functions ENABLE and Watchdog (Table 1).

Table 1. V_{OUT} as a Function of ENABLE and Watchdog

V_{OUT} (V)				
	WDI			
ENABLE	Slow	Normal	High	Low
H	5	5	5	5
L	0	5	0	0

As long as ENABLE is high or ENABLE is low and the Watchdog signal is normal, V_{OUT} will be at 5.0 V (typ). If ENABLE is low and the frequency of the Watchdog input goes below the threshold frequency, the output transistor turns off and the IC goes into SLEEP mode. Only the ENABLE circuitry in the IC remains powered up, drawing a quiescent current of less than 50 μA.

The Watchdog monitors the frequency of an incoming WDI signal. If the signal falls below the WDI limit, a frequency programmable pulse train is generated at the $\overline{\text{RESET}}$ lead (Figure 9) until the correct Watchdog input signal reappears at the lead (ENABLE = HIGH).

The threshold limit of the watchdog function is set by the value of C_{DELAY}. The limit is determined according to the following equation for the NCV8141:

$$t_{WDI} = (1.3 \times 10^5) C_{DELAY} \text{ or}$$

The capacitor C_{DELAY} also determines the frequency of the $\overline{\text{RESET}}$ signal and the POWER−ON−$\overline{\text{RESET}}$ (POR) delay period.

$\overline{\text{RESET}}$ Function

The $\overline{\text{RESET}}$ function is activated when the Watchdog frequency signal is below the watchdog threshold (Figure 9), when the regulator is in its power up state (Figure 10) or when V_{OUT} drops below V_{OUT} −4.5% for more than 2.0 μs (Figure 11)

If the Watchdog signal falls outside of the preset voltage or below the frequency threshold, a frequency programmable pulse train is generated at the $\overline{\text{RESET}}$ lead (Figure 9) until the correct Watchdog input signal reappears at the lead. The duration of the $\overline{\text{RESET}}$ pulse is determined by C_{DELAY} according to the following equation:

$$t_{WDI(\overline{\text{RESET}})} = (1.0 \times 10^4) C_{DELAY}$$

$\overline{\text{RESET}}$ CIRCUIT WAVEFORMS WITH DELAYS INDICATED

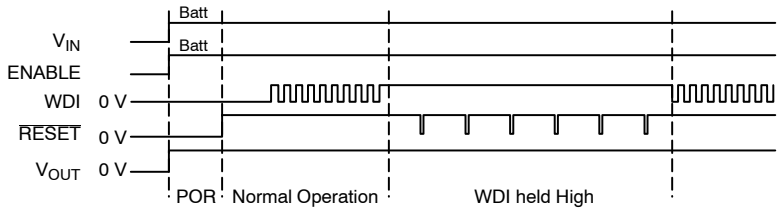
If an undervoltage condition exists, the voltage on the $\overline{\text{RESET}}$ lead goes low and the delay capacitor, C_{DELAY}, is discharged. $\overline{\text{RESET}}$ remains low until output is in regulation, the voltage on C_{DELAY} exceeds the upper threshold and the Watchdog input signal is valid (Figures 10 and 11). The delay after the output is in regulation is:

$$t_{POR(typ)} = (4.75 \times 10^5) C_{DELAY}$$

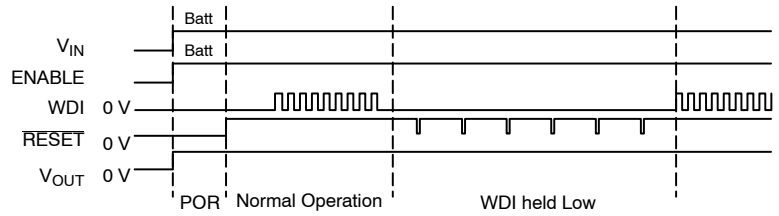
The $\overline{\text{RESET}}$ delay circuit is also programmed with the external cap C_{DELAY}.

The output of the reset circuit is an open collector NPN. $\overline{\text{RESET}}$ is operational down to V_{OUT} = 1.0 V. Both $\overline{\text{RESET}}$ and its delay are governed by comparators with hysteresis to avoid undesirable oscillations.

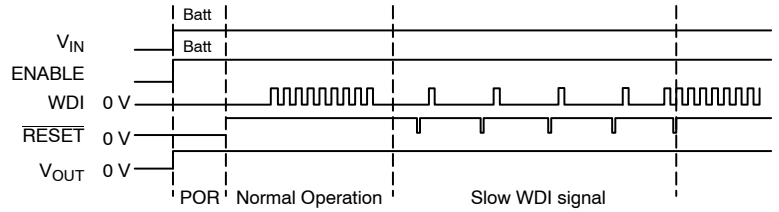
V_{OUT} When Watchdog is Held High and ENABLE = HIGH



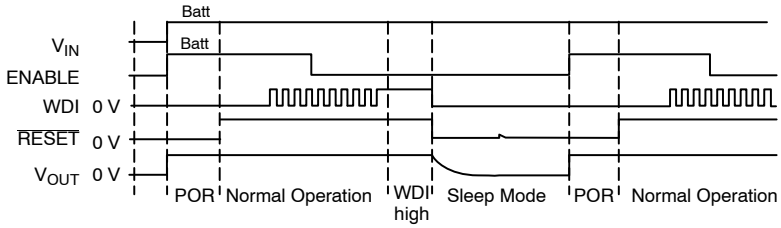
V_{OUT} When Watchdog is Held Low and ENABLE = HIGH



V_{OUT} When Watchdog is too Slow and ENABLE = HIGH



WDI Held High After a Normal Period of Operation; ENABLE = LOW



WDI Held Low or is too Slow after a Normal Period of Operation; ENABLE = LOW

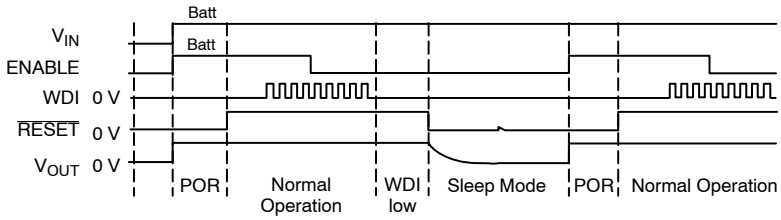


Figure 9. Timing Diagrams for Watchdog and ENABLE Functions

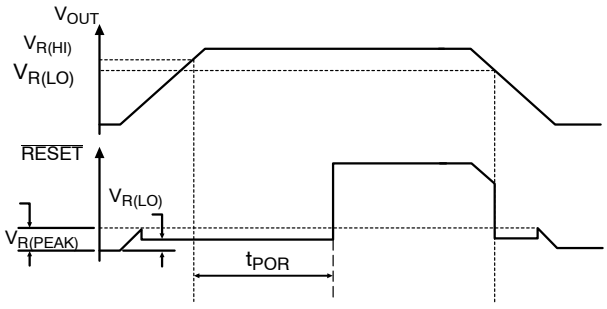


Figure 10. Power $\overline{RESET}$ and Power Down

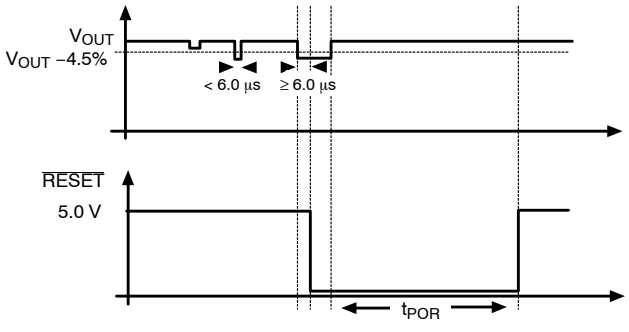


Figure 11. Undervoltage Triggered $\overline{RESET}$

APPLICATION NOTES

NCV8141 DESIGN EXAMPLE

The NCV8141 with its unique integration of linear regulator and control features: $\overline{\text{RESET}}$, ENABLE and WATCHDOG, provides a single IC solution for a microprocessor power supply. The reset delay, reset duration and watchdog frequency limit are all determined by a single capacitor. For a particular microprocessor the overriding requirement is usually the reset delay (also known as power on reset). The capacitor is chosen to meet this requirement and the reset duration and watchdog frequency follow.

The reset delay is given by:

$$t_{POR(typ)} = (4.75 \times 10^5) C_{DELAY}$$

Assume that the reset delay must be 200 ms minimum.

From the NCV8141 data sheet the reset delay has a $\pm 37\%$ tolerance due to the regulator.

Assume the capacitor tolerance is $\pm 10\%$.

$$t_{POR(min)} = (4.75 \times 10^5 \times 0.63) \times C_{DELAY} \times 0.9$$

$$C_{DELAY(min)} = \frac{t_{POR(min)}}{2.69 \times 10^5}$$

$$C_{DELAY(min)} = 0.743\ \mu F$$

Closest standard value is 0.82 μF.

Minimum and maximum delays using 0.82 μF are 220 ms and 586 ms.

The duration of the reset pulse is given by:

$$T_{WDI(\overline{RESET})(typ)} = (1.0 \times 10^4) \times C_{DELAY}$$

This has a tolerance of ±50% due to the IC, and ±10% due to the capacitor.

The duration of the reset pulse ranges from 3.69 ms to 13.5 ms.

The watchdog signal can be expressed as a frequency or time. From a programmers point of view, time is more useful since they must ensure that a watchdog signal is issued consistently several times per second.

The watchdog time is given by:

$$t_{WDI} = (1.3 \times 10^5) C_{DELAY}$$

There is a tolerance of ±20% due to the NCV8141.

With a capacitor tolerance of ±10%:

$$t_{WDI} = (1.3 \times 10^5) \times 1.2 \times 1.1 \times C_{Delay}$$

$$t_{WDI} = 141\ \text{ms (max)}$$

$$t_{WDI} = (1.3 \times 10^5) \times 0.8 \times 0.9 \times C_{DELAY}$$

$$t_{WDI} = 76\ \text{ms (min)}$$

The software must be written so that a watchdog signal arrives at least every 76 ms.

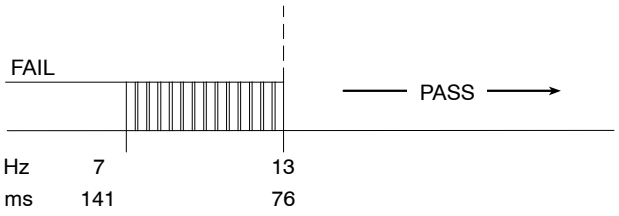


Figure 12. WDI Signal for C_{Delay} = 0.82 μF using NCV8141

ENERGY CONSERVATION AND SMART FEATURES

Energy conservation is another benefit of using a regulator with integrated microprocessor control features. Using the NCV8141 as indicated in Figure 13, the microprocessor can control its own power down sequence. The momentary contact switch quickly charges C1 through R1.

When the voltage across C1 reaches 3.95 V (the enable threshold), the output switches on and V_{OUT} rises to 5.0 V. After a delay period determined by C_{Delay}, a frequency programmable reset pulse train is generated at the reset output. The pulse train continues until the correct watchdog signal appears at the WDI lead. C1 is now left to discharge through the input impedance of the enable lead (approximately 150 kΩ) and the enable signal disappears. The output voltage remains at 5.0 V as long as the NCV8141 continues to receive the correct watchdog signal.

The microprocessor can power itself down by terminating its watchdog signal. When the microprocessor finishes its housekeeping or power down software routine, it stops sending a watchdog signal. In response, the regulator generates a reset signal and goes into a sleep mode where V_{OUT} drops to 0 V, shutting down the microprocessor.

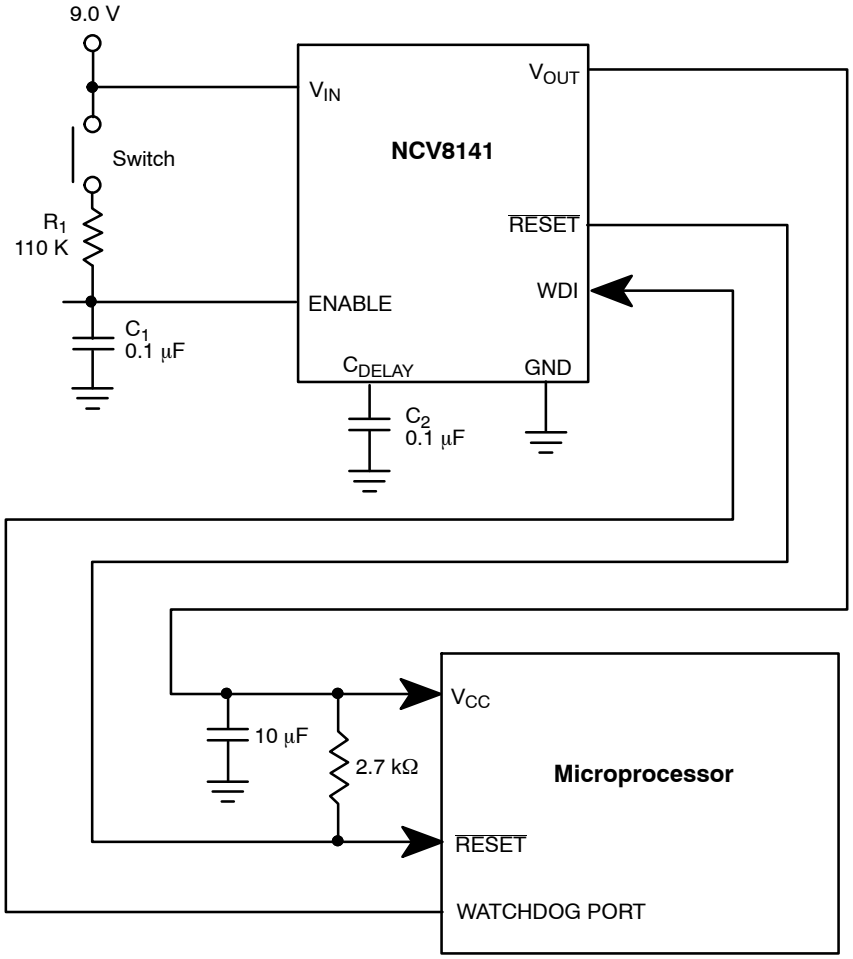
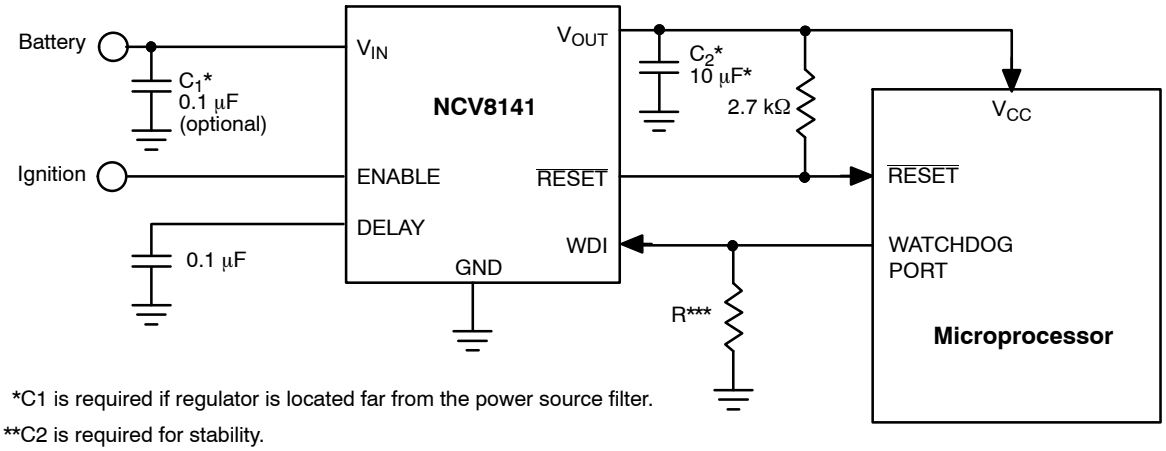


Figure 13. Application Diagram for NCV8141. The NCV8141 Provides a 5.0 V Tightly Regulated Supply and Control Function to the Microprocessor. In this Application, the Microprocessor Controls its own Power Down Sequence (see text).



*C1 is required if regulator is located far from the power source filter.

**C2 is required for stability.

***R ≤ 80 kΩ.

Figure 14. Application Diagram

STABILITY CONSIDERATIONS

The output or compensation capacitor C_2 in Figure 14 helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. An aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor C_2 shown in Figure 14 should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for C_2 for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in Step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat Steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat Steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Increase the temperature to the highest specified operating temperature. Vary the load current as instructed in Step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of ± 20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in Step 3 above.

CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 15) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}]I_{OUT(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,
$V_{OUT(min)}$ is the minimum output voltage,
$I_{OUT(max)}$ is the maximum output current for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

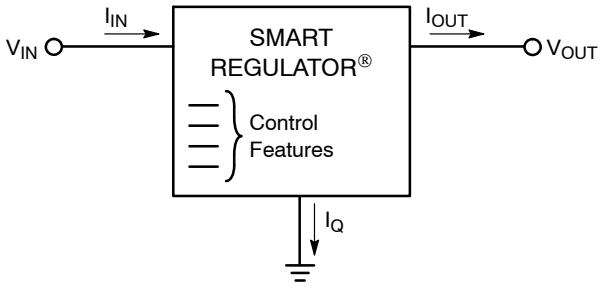


Figure 15. Single Output Regulator With Key Performance Parameters Labeled

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in Equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

HEATSINKS

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,

$R_{\theta CS}$ = the case−to−heatsink thermal resistance, and

$R_{\theta SA}$ = the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heatsink data sheets of heatsink manufacturers.

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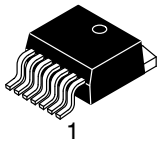
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

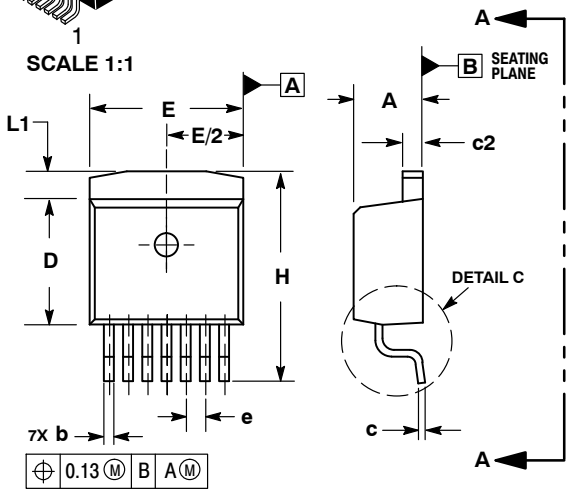
ON Semiconductor®

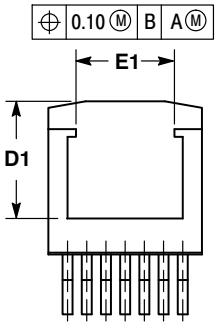
D²PAK–7 (SHORT LEAD)
CASE 936AB–01
ISSUE B

DATE 08 SEP 2009

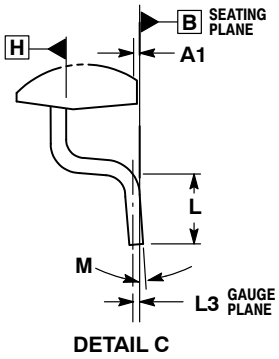


SCALE 1:1





VIEW A–A

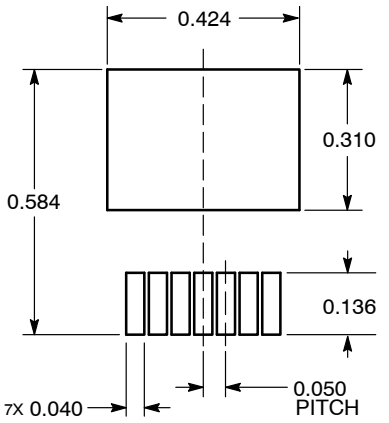


DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.005 MAXIMUM PER SIDE. THESE DIMENSIONS TO BE MEASURED AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1. DIMENSIONS D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THE THERMAL PAD.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.170	0.180	4.32	4.57
A1	0.000	0.010	0.00	0.25
b	0.026	0.036	0.66	0.91
c	0.017	0.026	0.43	0.66
c2	0.045	0.055	1.14	1.40
D	0.325	0.368	8.25	9.53
D1	0.270	---	6.86	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.050 BSC		1.27 BSC	
H	0.539	0.579	13.69	14.71
L	0.058	0.078	1.47	1.98
L1	---	0.066	---	1.68
L3	0.010 BSC		0.25 BSC	
M	0 °	8 °	0 °	8 °

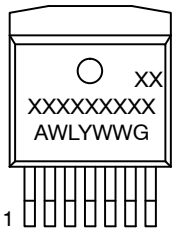
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

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