PIC24HJXXXGPX06/X08/X10 Rev. A2/A3/A4 Silicon Errata

The PIC24H (Rev. A2/A3/A4) devices you received were found to conform to the specifications and functionality described in the following documents:

- DS70175 – "*PIC24H Family Data Sheet*"
- DS70157 – "*dsPIC30F/33F Programmer's Reference Manual*"
- DS70046 – *"dsPIC30F Family Reference Manual"*

The exceptions to the specifications in the documents listed above are described in this section. The specific devices for which these exceptions are described are listed below:

- PIC24HJ64GP206
- PIC24HJ64GP210
- PIC24HJ64GP506
- PIC24HJ64GP510
- PIC24HJ128GP206
- PIC24HJ128GP210
- PIC24HJ128GP306
- PIC24HJ128GP310
- PIC24HJ128GP506
- PIC24HJ128GP510
- PIC24HJ256GP206
- PIC24HJ256GP210
- PIC24HJ256GP610

PIC24H Rev. A2/A3/A4 silicon is identified by performing a "Reset and Connect" operation to the device using MPLAB® ICD 2 with MPLAB IDE v7.40 or later. The output window will show a successful connection to the device specified in *Configure>Select Device*. The resulting DEVREV register values for Rev. A2/A3/A4 silicon are 0x3002, 0x3004, and 0x3040, respectively.

The errata described in this document will be addressed in future revisions of silicon.

Silicon Errata Summary

The following list summarizes the errata described in further detail through the remainder of this document:

1. Doze Mode

   When Doze mode is enabled, any writes to a peripheral SFR can cause other updates to that register to cease to function for the duration of the current CPU clock cycle.

2. 12-bit Analog-to-Digital Converter (ADC) Module

   For this revision of silicon, the 12-bit ADC module INL, DNL and signal acquisition time parameters are not within the published data sheet specifications.

3. 10-bit ADC Module

   For this revision of silicon, the 10-bit ADC module DNL, conversion speed and signal acquisition time parameters are not within the published data sheet specifications.

4. DMA Module: Interaction with `EXCH` Instruction

   The `EXCH` instruction does not execute correctly when one of the operands contains a value equal to the address of the DMAC SFRs.

5. `DISI` Instruction

   The `DISI` instruction will not disable interrupts if a `DISI` instruction is executed in the same instruction cycle that the `DISI` counter decrements to zero.

6. Output Compare Module in PWM Mode

   The output compare module will miss one compare event when the duty cycle register value is updated from 0x0000 to 0x0001.

7. SPI Module in Frame Master Mode

   The SPI module will fail to generate frame synchronization pulses in Frame Master mode if FRMDLY = 1.

8. SPI Module in Slave Select Mode

   The SPI module Slave Select functionality will not work correctly.

9. SPI Module

   The SMP bit does not have any effect when the SPI module is configured for a 1:1 prescale factor in Master mode.

10. ECAN™ Module

    ECAN transmissions may be incorrect if multiple transmit buffers are simultaneously queued for transmission.

11. ECAN Module

    Under specific conditions, the first five bits of a transmitted identifier may not match the value in the transmit buffer ID register.

12. ECAN Module Loopback Mode

    The ECAN module (ECAN1 or ECAN2) does not function correctly in Loopback mode.

13. I^2C™ Module

    The Bus Collision Status bit does not get set when a bus collision occurs during a Restart or Stop event.

14. INT0, ADC and Sleep/Idle Mode

    ADC event triggers from the INT0 pin will not wake-up the device from Sleep or Idle mode if the SMPI bits are non-zero.

15. Doze Mode and Traps

    The address error trap, stack error trap, math error trap and DMA error trap will not wake-up a device from Doze mode.

16. JTAG Programming

    JTAG programming does not work.

17. UART

    With the parity option enabled, a parity error may occur if the Baud Rate Generator (BRG) contains an odd value.

18. UART

    The Receive Buffer Overrun Error Status bit may get set before the UART FIFO has overflowed.

19. UART

    UART receptions may be corrupted if the BRG is set up for 4x mode.

20. UART

    The UTXISEL0 bit is always read back as zero.

21. UART

    The auto-baud feature may not calculate the correct baud rate when the BRG is set up for 4x mode.

22. UART

    With the auto-baud feature selected, the sync break character (0x55) may be loaded into the FIFO as data.

23. I^2C Module

    A write collision does not prevent the transmit register from being written.

24. I^2C Module

    The ACKSTAT bit only reflects the received ACK/NACK status for Master transmissions, but not for Slave transmissions.

25. I^2C Module

    The D_A Status bit does not get set on a slave write to the transmit register.

26. Traps and Idle Mode

    If a clock failure occurs when the device is in Idle mode, the oscillator failure trap does not vector to the Trap Service Routine (TSR).

27. $\overline{\text{MCLR}}$ Wake-up from Sleep Mode

    An $\overline{\text{MCLR}}$ wake-up from Sleep mode does not wait for the on-chip voltage regulator to power-up.

28. ECAN Module

    The C1RXOVF2 and C2RXOVF2 registers always read back as 0x0000.

29. FRC Oscillator

    Internal FRC accuracy parameters are not within the published data sheet specifications.

30. SPI Module

    SPI1 functionality for pin 34 (U1RX/SDI1/RF2) is erroneously enabled by the SPI2 module.

31. UART

    The auto-baud feature measures baud rate inaccurately for certain baud rate and clock speed combinations.

32. Device ID Register

    The content of the Device ID register changes from the factory programmed value.

33. DMA Module

    DMA data transfers that are active in Single-Shot mode while the device is in Sleep or Idle mode may result in more data transfers than expected.

34. Doze Mode and Traps

    A DMA error trap may not be generated when the device is in Doze mode.

35. Output Compare Module

    In Dual Compare Match mode, the OCx output is not reset when the OCxR and OCxRS registers are loaded with values having a difference of 1.

36. UART

    When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.

37. UART

    When an auto-baud is detected, the receive interrupt may occur twice.

38. DMA

    NULL Data Peripheral Write mode for the DMA channel does not function.

39. DMA

    DMA request Fault condition does not generate a DMA error trap.

40. DMA

    DMA channel writes an additional NULL value to the peripheral register.

41. REPEAT Instruction

    Any instruction executed inside a REPEAT loop that produces a Read-After-Write stall condition, results in the instruction being executed fewer times than was intended.

42. FRC Oscillator

    For certain values of the TUN<5:0> bits (OSCTUN<5:0>), the resultant frequencies are incorrect.

43. UART Module

    The 16x baud clock signal on the BCLK pin is present only when the module is transmitting.

44. SPI Module

    The SPIxCON1 DISSCK bit does not influence port functionality.

45. I^2C Module

    The BCL bit in I2CSTAT can be cleared only with 16-bit operation and can be corrupted with 1-bit or 8-bit operations on I2CSTAT.

46. I^2C Module: 10-bit addressing mode

    When the I^2C module is configured for 10-bit addressing using the same address bits (A10 and A9) as other I^2C devices, the A10 and A9 bits may not work as expected.

47. I^2C Module: 10-bit Addressing Mode

    When the I^2C module is configured as a 10-bit slave with an address of 0x102, the I2CxRCV register content for the lower address byte is 0x01 rather than 0x02.

48. I^2C Module

    With the I^2C module enabled, the PORT bits and external Interrupt Input functions (if any) associated with SCL and SDA pins will not reflect the actual digital logic levels on the pins.

49. I^2C Module: 10-bit Addressing Mode

    The 10-bit slave does not set the RBF flag or load the I2CxRCV register on address match if the Least Significant bits of the address are the same as the 7-bit reserved addresses.

50. Internal Voltage Regulator

    When the VREGS (RCON<8>) bit is set to a logic '0', higher sleep current may be observed.

51. ECAN Module

    The ECAN module does not generate a CAN event interrupt when coming out of Disable mode on bus wake-up activity even if the WAKIE bit in the CiINTE register is set.

52. PSV Operations

    An address error trap occurs in certain addressing modes when accessing the first four bytes of any PSV page.

53. UART (UxE Interrupt)

    The UART error interrupt may not occur, or may occur at an incorrect time, if multiple errors occur during a short period of time.

54. UART Module

    When the UART module is operating in 8-bit mode (PDSEL = 0x) and using the IrDA® encoder/decoder (IREN = 1), the module incorrectly transmits a data payload of 80h as 00h.

The following sections describe the errata and work around to these errata, where they may apply.

1. Module: Doze Mode

Enabling Doze mode slows down the CPU but allows peripherals to run at full speed. When the CPU clock is slowed down by enabling Doze mode (CLKDIV<11> = 1), any writes to a peripheral SFR can cause other updates to that register to cease to function for the duration of the current CPU clock cycle. This is only an issue if the CPU attempts to write to the same register as a peripheral while in Doze mode.

For instance, if the ADC module is active and Doze mode is enabled, the main program should avoid writing to ADCCONx registers because these registers are being used by the ADC module. If the CPU does make writes before the ADC module does, then any attempts by the ADC module to write to these registers will fail.

Work around

In Doze mode, avoid writing code that will modify SFRs which may be written to by enabled peripherals.

2. Module: 12-bit ADC

When the ADC module is configured for 12-bit operation, the specifications in the data sheets are not met.

Work around

Implement the ADC module as an 11-bit ADC with a maximum conversion rate of 300 ksps.

1. The specifications in Table 1 reflect 11-bit ADC operation. RIN source impedance is recommended as 200 ohms and sample time is recommended as 3 TAD to ensure compatibility on future enhanced ADC modules. Missing codes are possible every 2^7 codes.
2. When used as a 10-bit ADC, the INL is <±2 Least Significant Bytes (LSBs), and DNL is <±1 LSB with no missing codes. Maximum conversion rate is 300 ksps.

TABLE 1: ADC PERFORMANCE (11-BIT OPERATION)

Param No.	Symbol	Min	Typical	Max	Units	Conditions
AD17	RIN	—	—	200	Ohm	12-bit
ADC Accuracy – Measurements taken with External VREF+/VREF-						
AD20a	Nr	—	12 bits	—	Bits	—
AD21a	INL	-2	—	2	LSB	—
AD22a	DNL	-1.5	—	1	LSB	—
AD23a	GERR	1	5	10	LSB	—
AD24a	EOFF	1	3	6	LSB	—
ADC Accuracy – Measurements taken with Internal VREF+/VREF-						
AD21aa	INL	-2	—	2	LSB	—
AD22aa	DNL	-1.5	—	1	LSB	—
AD23aa	GERR	5	10	20	LSB	—
AD24aa	EOFF	3	6	15	LSB	—
Dynamic Performance						
AD33a	FNYQ	—	—	150	KHz	—
AD34a	ENOB	9.5	9.6	10.4	Bits	—
ADC Conversion Rate						
AD56a	FCNV	—	—	300	ksps	—
AD57a	TSAMP	—	3 TAD	—	—	—

3. Module: 10-bit ADC

When the ADC module is configured for 10-bit operation, the specifications in the data sheet are not met for operation above 500 ksps.

For 500 ksps, the module meets specifications except for Gain and Offset parameters AD23bb and AD24bb.

For 600 ksps operation, the module specifications are shown in Table 2.

Work around

None. Future versions of the silicon will support the ADC performance stated in the data sheet.

TABLE 2: 600 KSPS OPERATION

Param No.	Symbol	Min	Typical	Max	Units	Conditions
AD17	RIN	—	—	200	Ohm	10-bit
ADC Accuracy – Measurements taken with External VREF+/VREF-						
AD20b	Nr	—	10 bits	—	Bits	—
AD21b	INL	-2	—	2	LSB	—
AD22b	DNL	-1.5	—	2	LSB	—
AD23b	GERR	1	3	6	LSB	—
AD24b	EOFF	1	2	5	LSB	—
ADC Accuracy – Measurements taken with Internal VREF+/VREF-						
AD21bb	INL	-2	—	2	LSB	—
AD22bb	DNL	-1.5	—	2	LSB	—
AD23bb	GERR	1	6	12	LSB	—
AD24bb	EOFF	2	5	10	LSB	—
Dynamic Performance						
AD33b	FNYQ	—	—	300	KHz	—
AD34b	ENOB	8.5	9.7	9.8	Bits	—
ADC Conversion Rate						
AD56b	FCNV	—	—	600	ksps	—
AD57b	TSAMP	—	3 TAD	—	—	—

4. Module: DMA Module: Interaction with EXCH Instruction

The EXCH instruction does not execute correctly when either of the two operands is numerically equal to the address of any of the DMAC SFRs for this revision of silicon.

Work around

If writing source code in assembly, the recommended fix is to replace:

```
EXCH Wsource, Wdestination
```

with:

```
PUSH Wdestination
MOV Wsource, Wdestination
POP Wsource
```

If using the MPLAB C30 C compiler, specify the compiler option, `-merrata=exch` (*Project>Build Options>Projects>MPLAB C30>Use Alternate Settings*)

5. Module: DISI Instruction

When a user executes a DISI #7, for example, this will disable interrupts for 7 + 1 cycles (7 + the DISI instruction itself). In this case, the DISI instruction uses a counter which counts down from 7 to 0. The counter is loaded with 7 at the end of the DISI instruction.

If the user code executes another DISI on the instruction cycle where the DISI counter has become zero, the new DISI count is loaded, but the DISI state machine does not properly re-engage and continue to disable interrupts. At this point, all interrupts are enabled. The next time the user code executes a DISI instruction, the feature will act normally and block interrupts.

In summary, it is only when a DISI execution is coincident with the current DISI count = 0, that the issue occurs. Executing a DISI instruction before the DISI counter reaches zero will not produce this error. In this case, the DISI counter is loaded with the new value, and interrupts remain disabled until the counter becomes zero.

Work around

When executing multiple DISI instructions within the source code, make sure that subsequent DISI instructions have at least one instruction cycle between the time that the DISI counter decrements to zero and the next DISI instruction. Alternatively, make sure that subsequent DISI instructions are called before the DISI counter decrements to zero.

6. Module: Output Compare Module in PWM Mode

The Output Compare module will miss a compare event when the current duty cycle register (OCxRS) value is 0x0000 (0% duty cycle), and the OCxRS register is updated with a value of 0x0001. The compare event is only missed the first time a value of 0x0001 is written to OCxRS, and the PWM output remains low for one PWM period. Subsequent PWM high and low times occur as expected.

Work around

None. If the current OCxRS register value is 0x0000, avoid writing a value of 0x0001 to OCxRS. Instead, write a value of 0x0002; however, in this case the duty cycle will be slightly different from the desired value.

7. Module: SPI Module in Frame Master Mode

The SPI module will fail to generate frame synchronization pulses when configured in the Frame Master mode if the start of data is selected to coincide with the start of the frame synchronization pulse (FRMEN = 1, SPIFSD = 0, FRMDLY = 1). However, the module functions correctly in Frame Slave mode, and also in Frame Maser mode if FRMDLY = 0.

Work around

If DMA is not being used, manually drive the $\overline{SSx}$ pin (x = 1 or 2) high using the associated PORT register, and then drive it low after the required 1 bit-time pulse-width. This operation needs to be performed when the transmit buffer is written.

If DMA is being used, and if no other peripheral modules are using DMA transfers, use a Timer interrupt to periodically generate the frame synchronization pulse (using the method described above) after every 8- or 16-bit periods (depending on the data word size, configured using the MODE 16-bit).

If FRMDLY = 0, no work around is needed.

8. Module: SPI in Slave Select Mode

The SPI module Slave Select functionality (enabled by setting SSEN = 1) will not function correctly. Whether the $\overline{SSx}$ pin (x = 1 or 2) is high or low, the SPI data transfer will be completed and an interrupt will be generated.

Work around

If DMA is *not* being used, poll the SSx pin state using the Change Notification (CN) pin associated to the SSx pin as follows:

1. Disable the SPIx module by clearing the SPIEN bit in the SPIxSTAT register.
2. Clear the SSEN bit in the SPIxCON1 register to allow the I/O port to control the SSx pin.
3. Ensure that the CNx pin is configured as a digital input by setting the associated bit in the TRISx register.
4. Enable interrupts for the selected CNx pin by setting the appropriate bits in the CNEN1 and CNEN2 registers.
5. Turn on the weak pull-up device for the selected CNx pins by setting the appropriate bits in the CNPU1 and CNPU2 registers.
6. Clear the CNIF interrupt flag in the IFSx register.
7. Select the desired interrupt priority for CNx interrupts using the CNIP<2:0> control bits in the IPCx register.
8. Enable CNx interrupts using the CNIE control bit in the IECx register.
9. In the CNx Interrupt Service Routine, read the PORTx register associated to the SSx pin:
   a) If the PORTx bit is '0', then enable the SPIx module by setting the SPIEN bit and perform the required data read/write.
   b) If the PORTx bit is '1', then disable the SPIx module by setting the SPIEN bit, clear the SPI interrupt flag (SPIxIF), perform a dummy read of the SPIxBUF register and return from the Interrupt Service Routine (ISR).

If DMA is being used, no work around exists.

9. Module: SPI

The SMP bit (SPIxCON1<9>, where x = 1 or 2) does not have any effect when the SPI module is configured for a 1:1 prescale factor in Master mode. In this mode, whether the SMP bit is set or cleared, the data is always sampled at the end of data output time.

Work around

If sampling at the middle of data output time is required, then configure the SPI module to use a clock prescale factor other than 1:1 using the PPRE<1:0> and SPRE<2:0> bits in the SPIxCON1 register.

10. Module: ECAN

If multiple ECAN transmit buffers are enabled (multiple TXREQ or TXEN bits are set to '1' simultaneously), then the message transmissions from the enabled buffers may interfere with one another. As a result, incorrect ID and data transmissions will occur intermittently.

Work around

Enable only Buffer 0 for transmission at any given time. In the user application, this can be ensured by checking that all other TXREQn and TXENn bits are clear, before setting the TXREQn bit or TXENn to Buffer 0.

11. Module: ECAN

Under specific conditions, the first five bits of a transmitted identifier may not match the value in the transmit buffer SID. If the ECAN module detects a Start-of-Frame (SOF) in the third bit of interframe space and if a message to be transmitted is pending, the first five bits of the transmitted identifier may be corrupted.

Work around

None.

12. Module: ECAN Loopback Mode

The ECAN module (ECAN1 or ECAN2) does not function correctly in Loopback mode.

Work around

Do not use Loopback mode.

13. Module: I^2C

The Bus Collision Status bit (BCL) does not get set when a bus collision occurs during a Restart or Stop event. However, the BCL bit gets set when a bus collision occurs during a Start event.

Work around

None.

14. Module: INT0, ADC and Sleep/Idle Mode

ADC event triggers from the INT0 pin will not wake-up the device from Sleep or Idle mode if the SMPI bits are non-zero. This means that if the ADC is configured to generate an interrupt after a certain number of INT0 triggered conversions, the ADC conversions will not be triggered and the device will remain in Sleep. The ADC will perform conversions and wake-up the device only if it is configured to generate an interrupt after each INT0 triggered conversion (SMPI<3:0> = 0000).

Work around

None. If ADC event trigger from the INT0 pin is required, initialize SMPI<3:0> to '0000' (interrupt on every conversion).

15. Module: Doze Mode and Traps

The address error trap, stack error trap, math error trap and DMA error trap will not wake-up a device from Doze mode.

Work around

None.

16. Module: JTAG Programming

JTAG programming does not work.

Work around

None.

17. Module: UART

With the parity option enabled, a parity error, indicated by the PERR bit (UxSTA<3>) being set, may occur if the Baud Rate Generator contains an odd value. This affects both even and odd parity options.

Work around

Load the Baud Rate Generator register, UxBRG, with an even value, or disable the peripheral's parity option by loading either 0b00 or 0b11 into the Parity and Data Selection bits, PDSEL<1:0> (UxMODE<2:1>).

18. Module: UART

The Receive Buffer Overrun Error Status bit, OERR (UxSTA<1>), may get set before the UART FIFO has overflowed. After the fourth byte is received by the UART, the FIFO is full. The OERR bit should set after the fifth byte has been received in the UART shift register. Instead, the OERR bit may set after the fourth received byte with the UART Shift register empty.

Work around

After four bytes have been received by the UART, the UART Receiver Interrupt Flag bit, U1RXIF (IFS0<11>) or U2RXIF (IFS1<14>), will be set, indicating the UART FIFO is full. The OERR bit may also be set. After reading the UART receive buffer, UxRXREG, four times to clear the FIFO, clear both the OERR and UxRXIF bits in software.

19. Module: UART

UART receptions may be corrupted if the Baud Rate Generator is set up for 4x mode (BRGH = 1).

Work around

Use the 16x baud rate option (BRGH = 0) and adjust the baud rate accordingly.

20. Module: UART

The UTXISEL0 bit (UxSTA<13>) is always read as zero regardless of the value written to it. The bit can be written to either a '0' or '1', but will always be read as zero. This will affect read-modify-write operations such as bitwise or shift operations. Using a read-modify-write instruction on the UxSTA register (e.g., BSET, BLCR) will always write the UTXISEL0 bit to zero.

Work around

If a UTXISEL0 value of '1' is needed, avoid using read-modify-write instructions on the UxSTA register. Copy the UxSTA register to a temporary variable and set UxSTA<13> prior to performing read-modify-write operations. Copy the new value back to the UxSTA register.

21. Module: UART

The auto-baud feature may not calculate the correct baud rate when the High Baud Rate Enable bit, BRGH, is set. With the BRGH bit set, the baud rate calculation used is the same as BRG = 0.

Work around

If the auto-baud feature is needed, use the Low Baud Rate mode by clearing the BRGH bit.

22. Module: UART

With the auto-baud feature selected, the sync break character (0x55) may be loaded into the FIFO as data.

Work around

To prevent the sync break character from being loaded into the FIFO, load the UxBRG register with either 0x0000 or 0xFFFF prior to enabling the auto-baud feature (ABAUD = 1).

23. Module: I^2C

Writing to I2CxTRN during a Start bit transmission generates a write collision, indicated by the IWCOL (I2CxSTAT<7>) bit being set. In this state, additional writes to the I2CxTRN register should be blocked. However, in this condition, the I2CxTRN register can be written, although transmissions will not occur until the IWCOL bit is cleared in software.

Work around

After each write to the I2CxTRN register, read the IWCOL bit to ensure a collision has not occurred. If the IWCOL bit is set, it must be cleared in software and I2CxTRN register must be rewritten.

24. Module: I^2C

The ACKSTAT bit (I2CxSTAT<15>) only reflects the received ACK/NACK status for Master transmissions, but not for Slave transmissions. As a result, a Slave cannot use this bit to determine if it received an ACK or a NACK from a Master. In future silicon revisions, the ACKSTAT bit will reflect received ACK/NACK status for both Master and Slave transmissions.

Work around

The SDA pin should be connected to any other available I/O pin on the device. After transmitting a byte, the Slave should poll the SDA line (subject to a time-out period dependent on the application) to determine if an ACK (‘0’) or NACK (‘1’) was received.

25. Module: I^2C

The D_A Status bit (I2CxSTAT<5>) gets set on a slave data reception in the I2CxRCV register, but does not get set on a slave write to the I2CxTRN register. In future silicon revisions, the D_A bit will get set on a slave write to the I2CxTRN register.

Work around

Use the D_A Status bit only for determining slave reception status and not slave transmission status.

26. Module: Traps and Idle Mode

If a clock failure occurs when the device is in Idle mode, the oscillator failure trap does not vector to the Trap Service Routine. Instead, the device will simply wake-up from Idle mode and continue code execution if the Fail-Safe Clock Monitor (FSCM) is enabled.

Work around

Whenever the device wakes up from Idle (assuming the FSCM is enabled) the user software should check the state of the OSCFAIL bit (INTCON1<1>) to determine whether a clock failure occurred, and then perform the appropriate clock switch operation. Regardless, the Trap Service Routine must be included in the user application.

27. Module: $\overline{\text{MCLR}}$ Wake-up from Sleep Mode

If a $\overline{\text{MCLR}}$ reset pulse causes the device to wake-up from Sleep mode, the device wakes up without waiting for the on-chip voltage regulator to power-up. This will subsequently result in a Brown-out Reset (BOR).

Work around

None.

28. Module: ECAN

The C1RXOVF2 and C2RXOVF2 registers are non-functional. They are always read back as 0x0000, even when a receive overflow has occurred.

Work around

None.

29. Module: FRC Oscillator

The device does not meet the internal FRC accuracy specifications in the data sheet (Table 23-18 of the "*PIC24H Family Data Sheet*" (DS70175)). The actual accuracy specifications are shown in Table 3.

Work around

None.

TABLE 3: INTERNAL FRC ACCURACY

AC Characteristics		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Parameter No.	**Characteristic**	**Min**	**Typical**	**Max**	**Units**	**Conditions**	
Internal FRC Accuracy @ FRC Frequency = 7.37 MHz(1,2)							
F20	—	-3	—	+3	%	-40°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V

Note 1: Frequency calibrated at 25°C and 3.3V. TUN bits can be used to compensate for temperature drift.

2: Devices set to initial frequency of 7.37 MHz (±2%) at 25°C.

30. Module: SPI

SPI1 functionality for pin 34 (U1RX/SDI1/RF2) is enabled by the SPI2 module. As a result, two side effects occur:

1. RF2 functionality is disabled if the SPI2 module is enabled.
2. This pin will not function as SDI1 if the SPI1 module is enabled.

This issue affects 64-pin devices only:

- PIC24HJ64GP206
- PIC24HJ128GP206
- PIC24HJ256GP206
- PIC24HJ128GP306
- PIC24HJ64GP506
- PIC24HJ128GP506

Work around

Two conditions apply:

1. If the SPI2 module is used, pin 34 cannot be used as an I/O (RF2). It is recommended to use another I/O pin.
2. If the SPI1 module is used, the SPI2 module must also be enabled to gain SDI1 functionality on pin 34. As an alternative, I/O (RF2) can be configured as an input, which will allow pin 34 to function as SDI1.

31. Module: UART

The auto-baud feature may miscalculate for certain baud rate and clock speed combinations, resulting in a BRG value that is greater than or less than the expected value by 1. This may result in reception or transmission failures.

Work around

Test the auto-baud rate at various clock speed and baud rate combinations that would be used in an application. If an inaccurate BRG value is generated, manually correct the baud rate in user software.

32. Module: Device ID Register

On a few devices, the content of the Device ID register can change from the factory programmed default value immediately after RTSP or ICSP™ Flash programming.

As a result, development tools will not recognize these devices and will generate an error message indicating that the device ID and the device part number do not match. Additionally, some peripherals will be reconfigured and will not function as described in the device data sheet.

Refer to **Section 5. "Flash Programming"** (DS70191), of the "*dsPIC33F Family Reference Manual*" for an explanation of RTSP and ICSP Flash programming.

Work around

All RTSP and ICSP Flash programming routines must be modified as follows:

1. No word programming is allowed. Any word programming must be replaced with row programming.
2. During row programming, load write latches as described in **5.4.2.3 "Loading Write Latches"** of **Section 5. "Flash Programming"** (DS70191).
3. After latches are loaded, reload any latch location (in a given row) that has 5 LSB set to 0x18, with the original data. For example, reload one of the following latch locations with the desired data:

   0xXXXX18, 0xXXXX38, 0xXXXX58, 0xXXXX78, 0xXXXX98, 0xXXXXB8, 0xXXXXD8, 0xXXXXF8
4. Start row programming by setting NVMOP<3:0> = '0001' (memory row program operation) in the NVMCON register.
5. After row programming is complete, verify the contents of Flash memory.
6. If Flash verification errors are found, repeat steps 2 through 5. If Flash verification errors are found after a second iteration, report this problem to Microchip.

Steps 1 through 5 in the work around are implemented in MPLAB IDE version 8.00 or higher for the MPLAB ICD 2, MPLAB REAL ICE™ in-circuit emulator and PM3 tools.

33. Module: DMA

When a DMA channel is enabled in Single-Shot mode while the device is in Idle mode, and the corresponding peripheral is active and configured to operate during Idle mode, the DMA channel may not become disabled immediately upon transferring the required amount of data.

As a result, the number of bytes or words of data transferred may exceed the DMA transfer count specified in the DMAxCNT register.

For example, if DMA transfers are active for both SPI byte transmissions and receptions, and only the receive DMA channel interrupt is enabled for waking up the device from Idle mode, an extra byte will be transmitted by the time the device wakes up from Idle mode.

Work around

None.

34. Module: Doze Mode and Traps

A DMA error trap may not be generated when the device is in Doze mode.

Work around

None.

35. Module: Output Compare

When the Output Compare module is operated in the Dual Compare Match mode, a timer compare match with the value in the OCxR register sets the OCx output producing a rising edge on the OCx pin. Then, when a timer compare match with the value in the OCxRS register occurs, the OCx output is reset producing a falling edge on the OCx pin.

The above statement applies to all conditions except when the difference between OCxR and OCxRS is 1. In this case, the Output Compare module may miss the reset compare event, and cause the OCx pin to remain continuously high. This condition will remain until the difference between values in the OCxR and OCxRS registers is made greater than 1.

Work around

Ensure in software that the difference between values in OCxR and OCxRS registers is maintained greater than 1.

36. Module: UART

When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.

This issue does not affect the other UART configurations.

Work around

Use the 16x baud rate option (BRGH = 0) and adjust the baud rate accordingly.

37. Module: UART

When an auto-baud is detected, the receive interrupt may occur twice. The first interrupt occurs at the beginning of the Start bit and the second after reception of the Sync field character.

Work around

If an extra interrupt is detected, ignore the additional interrupt.

38. Module: DMA

When the DMA channel is configured for NULL Data Peripheral Write mode (DMAxCON<11> = 1), it does not execute a null (all zeros) write to the peripheral address.

Work around

Use two DMA channels to receive data from the peripheral module. One channel must be configured to transfer data from the peripheral to DMA RAM, while another channel must be configured to transfer dummy data from the DMA RAM to the peripheral. Both channels must be setup for the same DMA request.

39. Module: DMA

A low priority DMA channel request can be pre-empted by a higher priority DMA channel request. For example, if DMA Channel 0 has a higher priority than DMA Channel 1. A request to DMA channel 1 will be pending while DMA Channel 0 is processing its request. If DMA Channel 1 receives another request while it is in a pending request state, the DMA module does not generate a DMA error trap event.

Work around

None. Using higher priority DMA channels for servicing sources of frequent requests significantly reduces the possibility of the condition described above occurring, but does not completely eliminate it.

40. Module: DMA

When the DMA channel is configured for One Shot mode with NULL write enabled, the channel will write an extra NULL to the peripheral register after completing the last transfer. In the case of the SPI module and the SPIxBUF register, this would cause the SPI module to perform an extra receive operation.

Work around

None. In the case of using DMA NULL write with the SPI module, perform a dummy read of the SPIxBUF register after the DMA transfer is completed to clear the SPIRBF flag and prevent an un-expected overflow condition on the next SPI receive operation.

41. Module: REPEAT Instruction

Any instruction executed inside a REPEAT loop, which produces a Read-After-Write stall condition, results in the instruction being executed fewer times than was intended.

An example of such code is:

```
repeat #0xf
inc [w1],[++w1]
```

Work around

Avoid repeating an instruction that creates a stall using a REPEAT instruction. Instead, use a software loop using conditional branches.

42. Module: FRC Oscillator

For certain values of the TUN<5:0> bits (OSCTUN<5:0>), the resultant frequencies do not match the expected values.

As shown in Table 4, the actual frequencies obtained for different values of the TUN<5:0> bits are listed in terms of percentage change relative to the center frequency of 7.3728 MHz. The frequency errors listed in the table are approximate and may vary slightly from device to device.

It is recommended that the user application include some means of measuring the exact oscillator frequency in order to verify the frequencies listed below.

Work around

Configure your peripherals and other system parameters based on the actual frequencies listed in Table 4.

TABLE 4:

TUN<5:0>	Expected Change from 7.3728 MHz	Actual Change from 7.3728 MHz
000000	—	—
000001	+0.375%	+0.375%
000010	+0.75%	+0.75%
000011	+1.125%	+1.125%
000100	+1.5%	+1.5%
000101	+1.875%	+1.875%
000110	+2.25%	+2.25%
000111	+2.625%	+2.625%
001000	+3%	+3%
001001	+3.375%	+3.375%
001010	+3.75%	+3.75%
001011	+4.125%	+4.125%
001100	+4.5%	+4.5%
001101	+4.875%	+4.875%
001110	+5.25%	+5.25%
001111	+5.625%	+5.625%
010000	+6%	+8.325%
010001	+6.375%	+8.7%
010010	+6.75%	+9.075%
010011	+7.125%	+9.45%
010100	+7.5%	+9.825%
010101	+7.875%	+10.2%
010110	+8.25%	+10.575%
010111	+8.625%	+10.95%
011000	+9%	+11.325%
011001	+9.375%	+11.7%
011010	+9.75%	+12.075%
011011	+10.125%	+12.45%
011100	+10.5%	+12.825%
011101	+10.875%	+13.2%
011110	+11.25%	+13.575%
011111	+11.625%	+13.95%

TABLE 4: (CONTINUED)

TUN<5:0>	Expected Change from 7.3728 MHz	Actual Change from 7.3728 MHz
100000	-12%	-12%
100001	-11.625%	-11.625%
100010	-11.25%	-11.25%
100011	-10.875%	-10.875%
100100	-10.5%	-10.5%
100101	-10.125%	-10.125%
100110	-9.75%	-9.75%
100111	-9.375%	-9.375%
101000	-9%	-9%
101001	-8.625%	-8.625%
101010	-8.25%	-8.25%
101011	-7.875%	-7.875%
101100	-7.5%	-7.5%
101101	-7.125%	-7.125%
101110	-6.75%	-6.75%
101111	-6.375%	-6.375%
110000	-6%	-3.675%
110001	-5.625%	-3.3%
110010	-5.25%	-2.925%
110011	-4.875%	-2.55%
110100	-4.5%	-2.175%
110101	-4.125%	-1.8%
110110	-3.75%	-1.425%
110111	-3.375%	-1.05%
111000	-3%	-0.675%
111001	-2.625%	-0.3%
111010	-2.25%	+0.075%
111011	-1.875%	+0.45%
111100	-1.5%	+0.825%
111101	-1.125%	+1.2%
111110	-0.75%	+1.575%
111111	-0.375%	+1.95%

43. Module: UART

When the UART is configured for IR interface operations (UxMODE<9:8> = 11), the 16x baud clock signal on the BCLK pin is present only when the module is transmitting. The pin is idle at all other times.

Work around

Configure one of the output compare modules to generate the required baud clock signal when the UART is receiving data or in an idle state.

44. Module: SPI

Setting the DISSCK bit in the SPIxCON1 register does not allow the user application to use the SCK pin as a general purpose I/O pin.

Work around

None.

45. Module: I^2C

The BCL bit in I2CSTAT can be cleared only with 16-bit operation and can be corrupted with 1-bit or 8-bit operations on I2CSTAT.

Work around

Use 16-bit operations to clear BCL.

46. Module: I^2C

If there are two I^2C devices on the bus, one of them is acting as the Master receiver and the other as the Slave transmitter. If both devices are configured for 10-bit addressing mode, and have the same value in the A10 and A9 bits of their addresses, then when the Slave select address is sent from the Master, both the Master and Slave acknowledge it. When the Master sends out the read operation, both the Master and the Slave enter into Read mode and both of them transmit the data. The resultant data will be the ANDing of the two transmissions.

Work around

In all I^2C devices, the addresses as well as bits A10 and A9 should be different.

47. Module: I^2C

When the I^2C module is configured as a 10-bit slave with and address of 0x102, the I2CxRCV register content for the lower address byte is 0x01 rather than 0x02; however, the module acknowledges both address bytes.

Work around

None.

48. Module: I^2C

With the I^2C module enabled, the PORT bits and external interrupt input functions (if any) associated with the SCL and SDA pins do not reflect the actual digital logic levels on the pins.

Work around

If the SDA and/or SCL pins need to be polled, these pins should be connected to other port pins in order to be read correctly. This issue *does not* affect the operation of the I^2C module.

49. Module: I^2C

In 10-bit Addressing mode, some address matches don't set the RBF flag or load the receive register I2CxRCV, if the lower address byte matches the reserved addresses. In particular, these include all addresses with the form XX0000XXXX and XX1111XXXX, with the following exceptions:

- 001111000X
- 011111001X
- 101111010X
- 111111011X

Work around

Ensure that the lower address byte in 10-bit Addressing mode does not match any 7-bit reserved addresses.

50. Module: Internal Voltage Regulator

When the VREGS (RCON<8>) bit is set to a logic '0', higher sleep current may be observed.

Work around

Ensure VREGS (RCON<8>) bit is set to a logic '1' for device Sleep mode operation.

51. Module: ECAN

The ECAN module does not generate a CAN event interrupt when coming out of Disable mode on bus wake-up activity even if the WAKIE bit in the CiINTE register is set. The WAKIF bit in the CiINTF register will reflect the correct status. The CAN event interrupt occurs only if the device was in Sleep mode when the bus wake-up activity occurred.

Work around

When placing the ECAN module in Disable mode, place the device in Sleep mode to be able to generate the CAN event interrupt on bus wake-up activity. If it is not possible to place the device in Sleep mode, poll the WAKIF bit in the CiINTF register to track bus wake-up activity.

52. Module: PSV Operations

An address error trap occurs in certain addressing modes when accessing the first four bytes of an PSV page. This only occurs when using the following addressing modes:

- MOV.D
- Register Indirect Addressing (word or byte mode) with pre/post-decrement

Work around

Do not perform PSV accesses to any of the first four bytes using the above addressing modes. For applications using the C language, MPLAB C30 version 3.11 or higher, provides the following command-line switch that implements a work around for the erratum.

```
-merrata=psv_trap
```

Refer to the `readme.txt` file in the MPLAB C30 v3.11 tool suite for further details.

53. Module: UART (UxE Interrupt)

The UART error interrupt may not occur, or may occur at an incorrect time, if multiple errors occur during a short period of time.

Work around

Read the error flags in the UxSTA register whenever a byte is received to verify the error status. In most cases, these bits will be correct, even if the UART error interrupt fails to occur.

54. Module: UART (IrDA)

When the UART is operating in 8-bit mode (PDSEL = 0x) and using the IrDA encoder/decoder (IREN = 1), the module incorrectly transmits a data payload of 80h as 00h.

Work around

None.

APPENDIX A: REVISION HISTORY

Revision A (6/2006)

Initial release of the document.

Revision B (12/2006)

Added issues 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, and 17.

Revision C (3/2007)

Changed document title, updated issue 8, and added issues 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30 and 31.

Revision D (6/2007)

Added the following silicon issues: 32 (SPI), 33 (UART), 34 (Device ID Register), 35 (DMA), 36 (Doze Mode and Traps) and 37 (DCI).

Revision E (10/2007)

Removed issue 6 (Output Compare) and issue 37 (DCI). Updated silicon issue 27 (Traps and Idle Mode). Added silicon issues 36 (ECAN), 37 (Output Compare), 38-39 (UART), 40-42 (DMA), 43 (REPEAT Instruction), and 44 (FRC Oscillator).

Revision F (4/2008)

Updated silicon issues 4 (DMA Module: Interaction with EXCH Instruction) 10 (ECAN). Removed silicon issue 23 (ECAN). Added silicon issues 44 (UART), 45 (SPI) and 46-47 (I^2C).

Revision G (9/2008)

Added reference to silicon revision A4. Updated issue 8 (SPI in Slave Select Mode) and 24 (I^2C). Removed issue 35 (ECAN). Added silicon issues 47-49 (I^2C), 50 (Internal Voltage Regulator), 51 (ECAN), 52 (PSV Operations), 53 (UART (UxE Interrupt)) and 54 (UART (IrDA)).

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