



PIC16F193X/LF193X Memory Programming Specification

This document includes the programming specifications for the following devices:

- PIC16F1933 • PIC16F1934 • PIC16F1936
- PIC16F1937 • PIC16F1938 • PIC16F1939
- PIC16LF1933 • PIC16LF1934 • PIC16LF1936
- PIC16LF1937 • PIC16LF1938 • PIC16LF1939

1.0 OVERVIEW

The PIC16F193X and PIC16LF193X devices can be programmed using either the high-voltage In-Circuit Serial Programming™ (ICSP™) method or the low-voltage ICSP™ method.

1.1 Hardware Requirements

1.1.1 HIGH-VOLTAGE ICSP PROGRAMMING

In High-Voltage ICSP™ mode, the PIC16F193X and PIC16LF193X devices require two programmable power supplies: one for VDD and one for the MCLR/VPP/RE3 pin.

1.1.2 LOW-VOLTAGE ICSP PROGRAMMING

In Low-Voltage ICSP™ mode, the PIC16F193X and PIC16LF193X devices can be programmed using a single VDD source in the operating range. The MCLR/VPP/RE3 pin does not have to be brought to a different voltage, but can instead be left at the normal operating voltage.

1.1.2.1 Single-Supply ICSP Programming

The LVP bit in Configuration Word 2 enables single-supply (low-voltage) ICSP programming. The LVP bit defaults to a '1' (enabled) from the factory. The LVP bit may only be programmed to '0' by entering the High-Voltage ICSP mode, where MCLR/VPP/RE3 pin is raised to VIH. Once the LVP bit is programmed to a '0', only the High-Voltage ICSP mode is available and only the High-Voltage ICSP mode can be used to program the device.

Note 1: The High-Voltage ICSP mode is always available, regardless of the state of the LVP bit, by applying VIH to the MCLR/VPP/RE3 pin.

2: While in Low-Voltage ICSP mode, MCLR is always enabled, regardless of the MCLRE bit, and RE3 pin can no longer be used as a general purpose input.

1.2 Pin Utilization

Five pins are needed for ICSP™ programming. The pins are listed in Table 1-1.

TABLE 1-1: PIN DESCRIPTIONS DURING PROGRAMMING

Pin Name	During Programming		
	Function	Pin Type	Pin Description
RB6	ICSPCLK	I	Clock Input – Schmitt Trigger Input
RB7	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
RE3/MCLR/VPP	Program/Verify mode	P ⁽¹⁾	Program Mode Select/Programming Power Supply
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

Note 1: In the PIC16F193X/LF193X, the programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to MCLR input. Since the MCLR is used for a level source, MCLR does not draw any significant current.

PIC16F193X/LF193X

Table of Contents

1.0	Overview	1
1.1	Hardware Requirements	1
1.1.1	High-Voltage ICSP Programming	1
1.1.2	Low-Voltage ICSP Programming	1
1.2	Pin Utilization	1
2.0	Device Pinouts	3
3.0	Memory Map	8
3.1	User ID Location	9
3.2	Device ID	9
3.3	Configuration Words	10
3.4	Calibration Words	10
4.0	Program/Verify Mode	13
4.1	High Voltage Program/Verify Mode Entry and Exit	13
4.1.1	VPP – First Entry Mode	13
4.1.2	VDD – First Entry Mode	13
4.1.3	Program/Verify Mode Exit	13
4.2	Low-Voltage Programming (LVP) Mode	13
4.3	Program/Verify Commands	14
4.3.1	Load Configuration	15
4.3.2	Load Data For Program Memory	15
4.3.3	Load Data For Data Memory	16
4.3.4	Read Data From Program Memory	16
4.3.5	Read Data From Data Memory	17
4.3.6	Increment Address	17
4.3.7	Reset Address	18
4.3.8	Begin Internally Timed Programming	18
4.3.9	Begin Externally Timed Programming	19
4.3.10	End Externally Timed Programming	19
4.3.11	Bulk Erase Program Memory	20
4.3.12	Bulk Erase Data Memory	20
4.3.13	Row Erase Program Memory	21
5.0	Programming Algorithms	22
6.0	Code Protection	30
6.1	Program Memory	30
6.2	Data Memory	30
7.0	Hex File Usage	30
7.1	Configuration Word	30
7.2	Device ID and Revision	30
7.3	Data EEPROM	30
7.4	Checksum Computation	31
7.4.1	Code Protection Disabled	31
7.4.2	Code Protection Enabled	32
8.0	Electrical Specifications	33
8.1	AC Timing Diagrams	34

2.0 DEVICE PINOUTS

The pin diagrams for the PIC16F193X/PIC16LF193X family are shown in Figure 2-1 through Figure 2-5. The pins that are required for programming are listed in Table 1-1 and shown in bold lettering in the pin diagrams.

FIGURE 2-1: 28-PIN PDIP/SOIC/SSOP DIAGRAM FOR PIC16F1933/1936/1938 AND PIC16LF1933/1936/1938

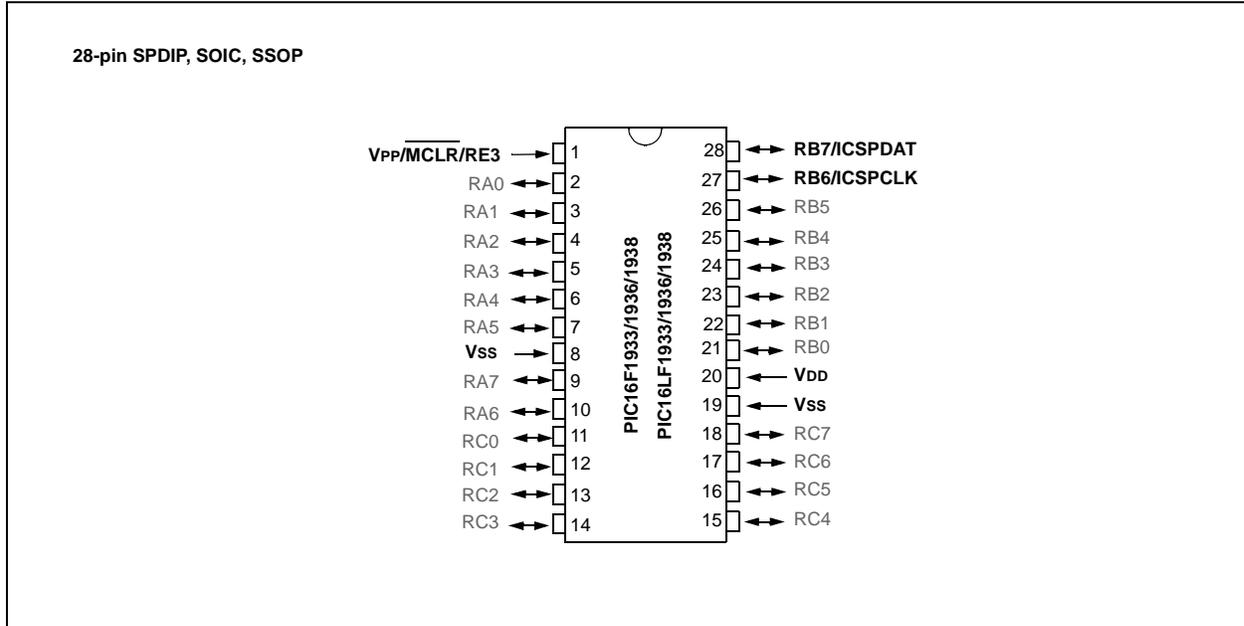
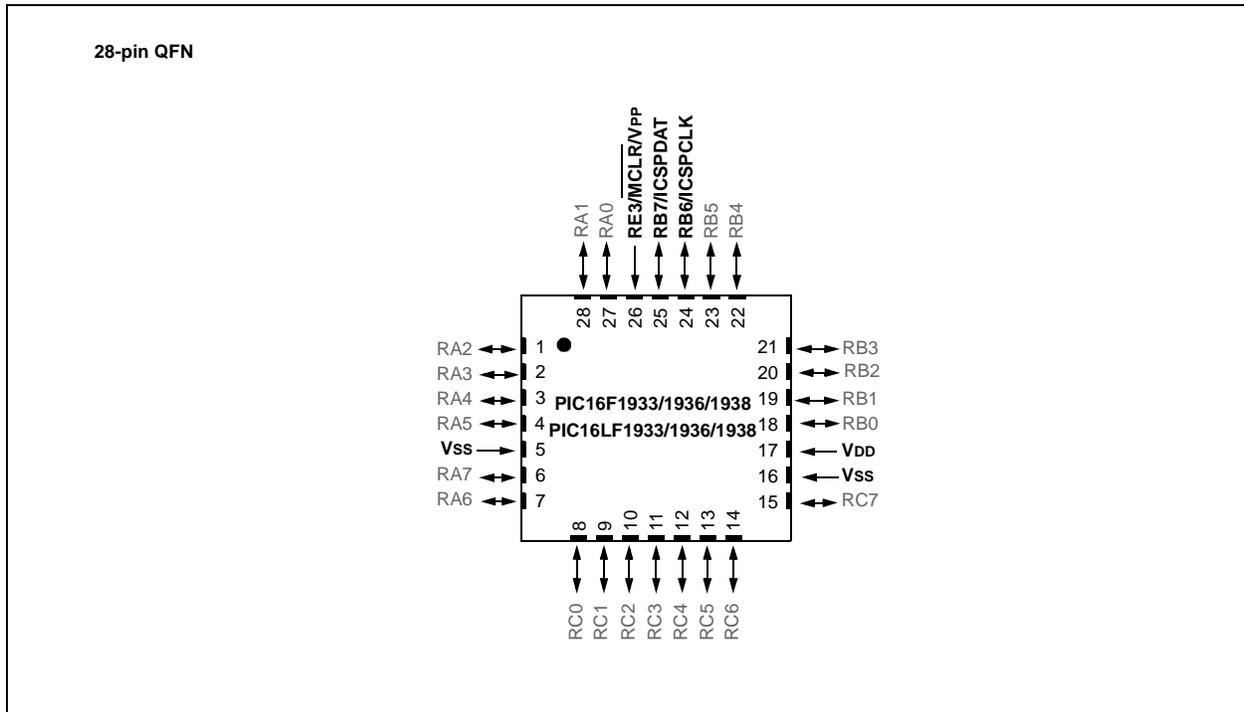


FIGURE 2-2: 28-PIN QFN PACKAGE DIAGRAM FOR PIC16F1933/1936/1938 AND PIC16LF1933/1936/1938



PIC16F193X/LF193X

FIGURE 2-3: 40-PIN PDIP PACKAGE DIAGRAM FOR PIC16F1934/1937/1939 AND PIC16LF1934/1937/1939

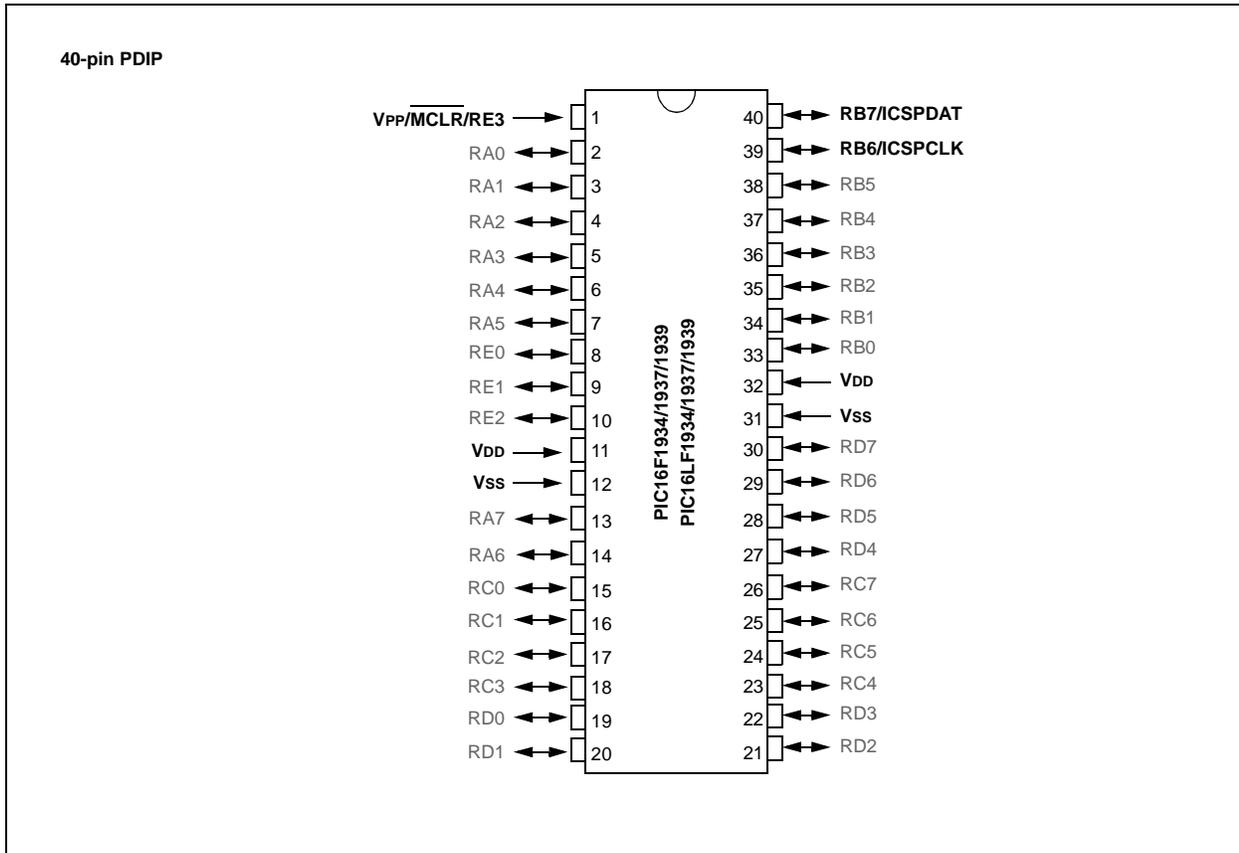
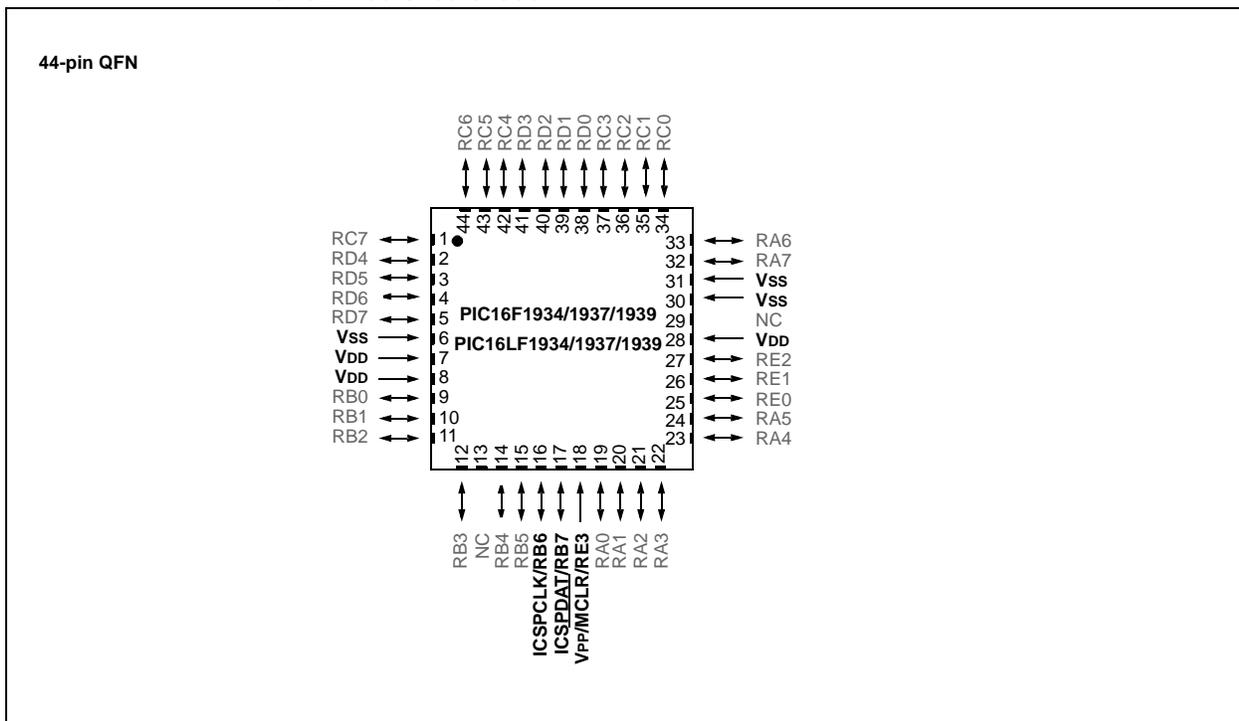
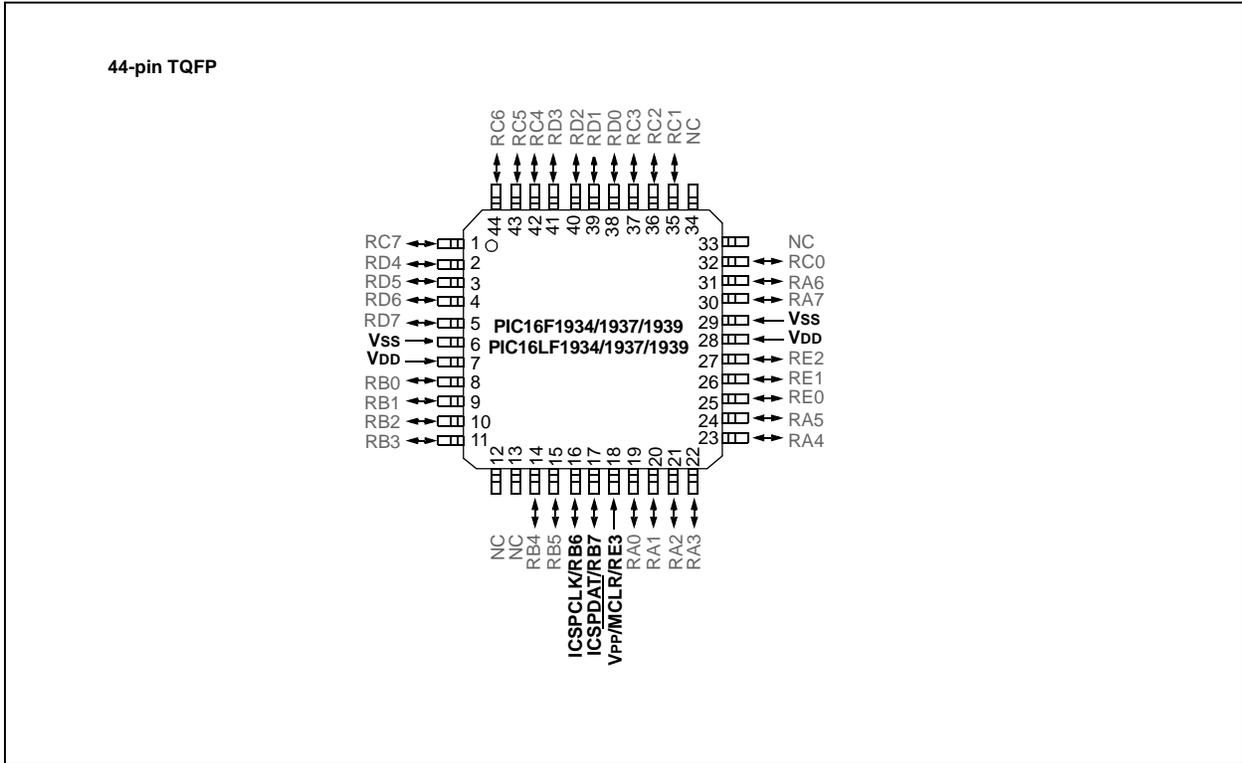


FIGURE 2-4: 44-PIN QFN PACKAGE DIAGRAM FOR PIC16F1934/1937/1939 AND PIC16LF1934/1937/1939



PIC16F193X/LF193X

FIGURE 2-5: 44-PIN TQFP PACKAGE DIAGRAM FOR PIC16F1934/1937/1939 AND PIC16LF1934/1937/1939

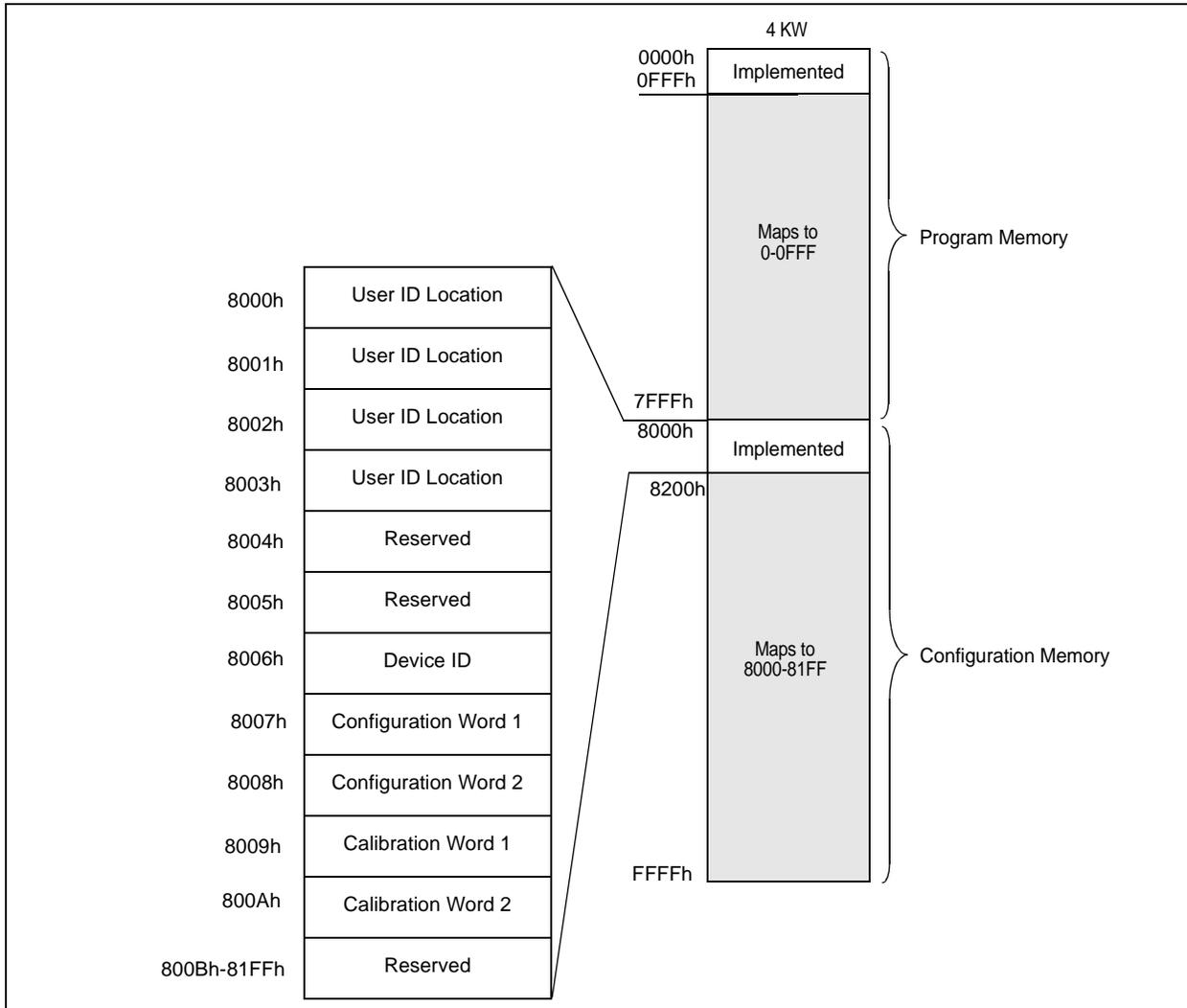


PIC16F193X/LF193X

3.0 MEMORY MAP

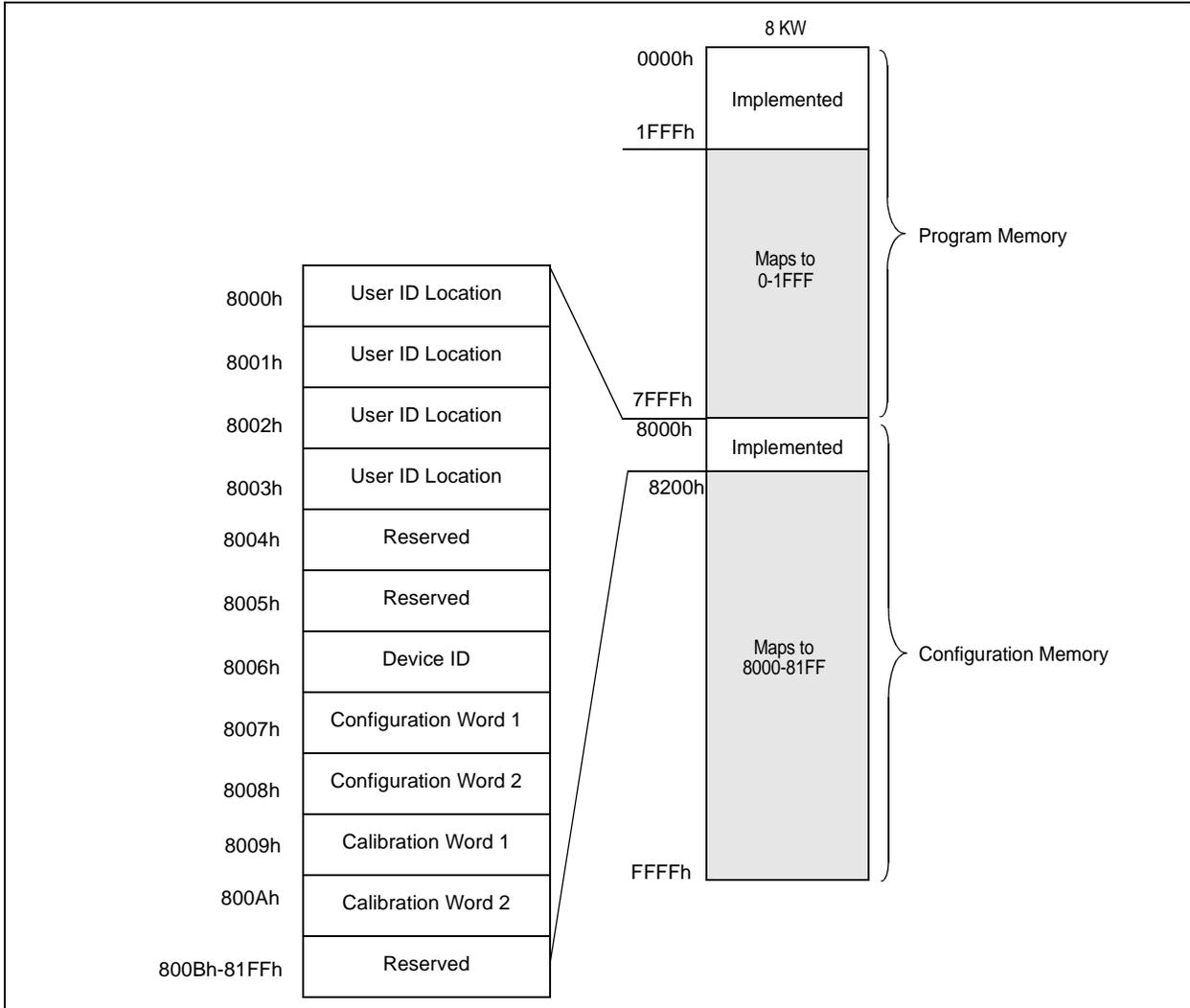
The memory for the PIC16F193X/LF193X devices is broken into two sections: program memory and configuration memory. Only the size of the program memory changes between devices, the configuration memory remains the same.

FIGURE 3-1: PIC16F1933/PIC16LF1933, PIC16F1934/PIC16LF1934 PROGRAM MEMORY MAPPING



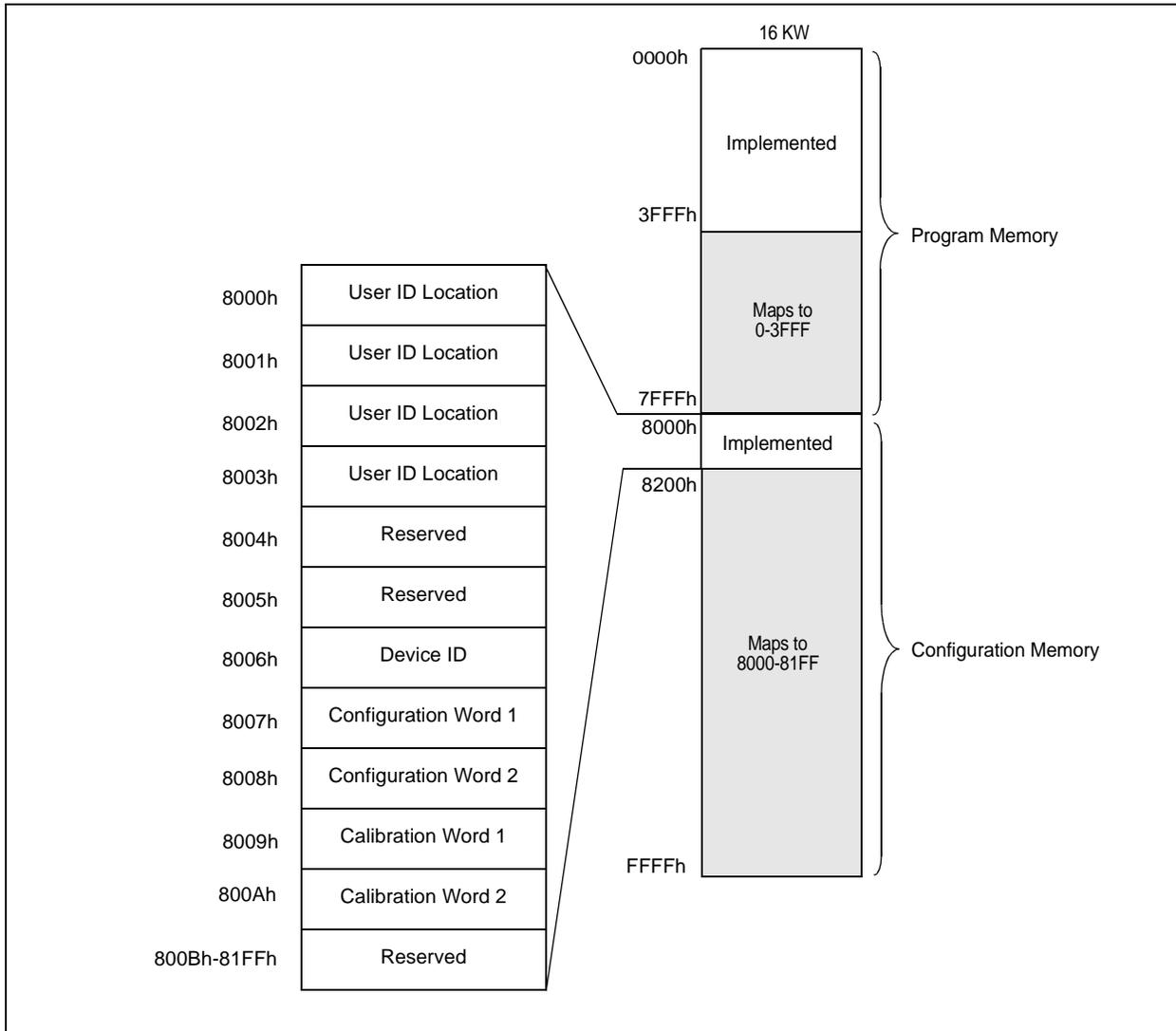
PIC16F193X/LF193X

FIGURE 3-2: PIC16F1936/PIC16LF1936, PIC16F1937/PIC16LF1937 PROGRAM MEMORY MAPPING



PIC16F193X/LF193X

FIGURE 3-3: PIC16F1938/PIC16LF1938, PIC16F1939/PIC16LF1939 PROGRAM MEMORY MAPPING



PIC16F193X/LF193X

3.1 User ID Location

A user may store identification information (user ID) in four designated locations. The user ID locations are mapped to 8000h-8003h. Each location is 14 bits in length. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

Note: MPLAB® IDE only displays the 7 Least Significant bits (LSb) of each user ID location, the upper bits are not read. It is recommended that only the 7 LSb's be used if MPLAB IDE is the primary tool used to read these addresses.

3.2 Device ID

The device ID word for the PIC16F193X/LF193X is located at 8006h. This location is read-only and can not be erased or modified.

REGISTER 3-1: DEVICEID: DEVICE ID REGISTER⁽¹⁾

R-q	R-q	R-q	R-q	R-q	R-q	R-q
DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	DEV2
bit 13						bit 7

R-q	R-q	R-q	R-q	R-q	R-q	R-q
DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 6						bit 0

Legend:	P = Programmable bit	U = Unimplemented bit, read as '0'
R = Readable bit	W = Writable bit	'0' = Bit is cleared
-n = Value at POR	'1' = Bit is set	x = Bit is unknown

bit 13-5 **DEV<8:0>**: Device ID bits
These bits are used to identify the part number.

bit 4-0 **REV<4:0>**: Revision ID bits
These bits are used to identify the revision.

Note 1: This location cannot be written.

TABLE 3-1: DEVICE ID VALUES

DEVICE	DEVICE ID VALUES	
	DEV	REV
PIC16F1933	10 0011 001	x xxxxx
PIC16F1934	10 0011 010	x xxxxx
PIC16F1936	10 0011 011	x xxxxx
PIC16F1937	10 0011 100	x xxxxx
PIC16F1938	10 0011 101	x xxxxx
PIC16F1939	10 0011 110	x xxxxx
PIC16LF1933	10 0100 001	x xxxxx
PIC16LF1934	10 0100 010	x xxxxx
PIC16LF1936	10 0100 011	x xxxxx
PIC16LF1937	10 0100 100	x xxxxx
PIC16LF1938	10 0100 101	x xxxxx
PIC16LF1939	10 0100 110	x xxxxx

PIC16F193X/LF193X

3.3 Configuration Words

The PIC16F193X/PIC16LF193X has two Configuration Words, Configuration Word 1 (8007h) and Configuration Word 2 (8008h). The individual bits within these Configuration Words are used to enable or disable device functions such as the Brown-out Reset, code protection and Power-up Timer.

3.4 Calibration Words

For the PIC16F193X/PIC16LF193X devices, the internal calibration values are factory calibrated and stored in Calibration Words 1 and 2 (8009h and 800Ah).

The Calibration Words do not participate in erase operations. The device can be erased without affecting the Calibration Words.

REGISTER 3-2: CONFIGURATION WORD 1

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
FCMEN	IESO	CLKOUTEN	BOREN1	BOREN0	CPD	CP
bit 13						bit 7

R/P-1						
MCLRE	PWRTE	WDTE1	WDTE0	FOSC2	FOSC1	FOSC0
bit 6						bit 0

Legend:	U = Unimplemented bit, read as '0'
R = Readable bit	'0' = Bit is cleared
-n = Value at POR	x = Bit is unknown
W = Writable bit	
'1' = Bit is set	

- bit 13 **FCMEN:** Fail-Safe Clock Monitor Enable bit
 1 = Fail-Safe Clock Monitor is enabled
 0 = Fail-Safe Clock Monitor is disabled
- bit 12 **IESO:** Internal External Switchover bit
 1 = Internal/External Switchover mode is enabled
 0 = Internal/External Switchover mode is disabled
- bit 11 **CLKOUTEN:** Clock Out Enable bit
 1 = CLKOUT function is disabled. I/O or oscillator function on RA6/CLKOUT
 0 = CLKOUT function is enabled on RA6/CLKOUT
- bit 10-9 **BOREN<1:0>:** Brown-out Reset Enable bits⁽¹⁾
 11 = BOR enabled
 10 = BOR enabled during operation and disabled in Sleep
 01 = BOR controlled by SBOREN bit of the PCON register
 00 = BOR disabled
- bit 8 **CPD:** Data Code Protection bit⁽²⁾
 1 = Data memory code protection is disabled
 0 = Data memory code protection is enabled
- bit 7 **CP:** Code Protection bit⁽³⁾
 1 = Program memory code protection is disabled
 0 = Program memory code protection is enabled
- bit 6 **MCLRE:** RE3/MCLR/VPP Pin Function Select bit
 If LVP bit = 1:
 This bit is ignored.
 If LVP bit = 0:
 1 = RE3/MCLR/VPP pin function is MCLR; Weak pull-up enabled.
 0 = RE3/MCLR/VPP pin function is digital input; MCLR internally disabled; Weak pull-up under control of WPUE3 bit.
- bit 5 **PWRTE:** Power-up Timer Enable bit⁽¹⁾
 1 = PWRT disabled
 0 = PWRT enabled
- bit 4-3 **WDTE<1:0>:** Watchdog Timer Enable bit
 11 = WDT enabled
 10 = WDT enabled while running and disabled in Sleep.
 01 = WDT controlled by the SWDTEN bit in the WDTCN register
 00 = WDT disabled
- bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
 111 = ECH: External Clock, High-Power mode: CLKIN on RA7/OSC1/CLKIN
 110 = ECM: External Clock, Medium-Power mode: CLKIN on RA7/OSC1/CLKIN
 101 = ECL: External Clock, Low-Power mode: CLKIN on RA7/OSC1/CLKIN
 100 = INTOSC oscillator: I/O function on RA7/OSC1/CLKIN
 011 = EXTRC oscillator: RC function on RA7/OSC1/CLKIN
 010 = HS oscillator: High-speed crystal/resonator on RA6/OSC2/CLKOUT pin and RA7/OSC1/CLKIN
 001 = XT oscillator: Crystal/resonator on RA6/OSC2/CLKOUT pin and RA7/OSC1/CLKIN
 000 = LP oscillator: Low-power crystal on RA6/OSC2/CLKOUT pin and RA7/OSC1/CLKIN

- Note 1:** Enabling Brown-out Reset does not automatically enable Power-up Timer.
Note 2: The entire data EEPROM will be erased when the code protection is turned off during an erase.
Note 3: The entire program memory will be erased when the code protection is turned off.

PIC16F193X/LF193X

REGISTER 3-3: CONFIGURATION WORD 2

R/P-1	R/P-1	U-1	R/P-1	R/P-1	R/P-1	U-1
LVP	DEBUG	—	BORV	STVREN	PLLEN	—
bit 13						bit 7

U-1	R/P-1	R/P-1	U-1	U-1	R/P-1	R/P-1
—	VCAPEN1	VCAPEN0	—	—	WRT1	WRT0
bit 6						bit 0

Legend:	U = Unimplemented bit, read as '0'
R = Readable bit	W = Writable bit
-n = Value at POR	'0' = Bit is cleared
	'1' = Bit is set
	x = Bit is unknown

- bit 13 **LVP:** Low-Voltage Programming Enable bit⁽¹⁾
 1 = Low-voltage programming enabled
 0 = HV on MCLR/VPP must be used for programming.
- bit 12 **DEBUG:** In-Circuit Debugger Mode bit
 1 = In-Circuit Debugger disabled, RB6/ICSPCLK and RB7/ICSPDAT are general purpose I/O pins
 0 = In-Circuit Debugger enabled, RB6/ICSPCLK and RB7/ICSPDAT are dedicated to the debugger
- bit 11 **Unimplemented:** Read as '1'
- bit 10 **BORV:** Brown-out Reset Voltage Selection bit
 1 = Brown-out Reset voltage set to 1.9V
 0 = Brown-out Reset voltage set to 2.7V
- bit 9 **STVREN:** Stack Overflow/Underflow Reset Enable bit
 1 = Stack overflow or underflow will cause a Reset
 0 = Stack overflow or underflow will not cause a Reset
- bit 8 **PLLEN:** PLL Enable bit
 1 = 4xPLL enabled
 0 = 4xPLL disabled
- bit 7-6 **Unimplemented:** Read as '1'
- bit 5-4 **VCAPEN<1:0>:** Voltage Regulator Capacitor Enable bits⁽²⁾
 00 = VCAP functionality is enabled on RA0.
 01 = VCAP functionality is enabled on RA5.
 10 = VCAP functionality is enabled on RA6.
 11 = No capacitor on VCAP pin.
- bit 3-2 **Unimplemented:** Read as '1'
- bit 1-0 **WRT<1:0>:** Flash memory self-write protection bits
4 kW FLASH memory (PIC16F1933/PIC16LF1933 and PIC16F1934/PIC16LF1934 only):
 11 = Write protection off
 10 = 000h to 1FFh write protected, 200h to FFFh may be modified by EECON control
 01 = 000h to 7FFh write protected, 800h to FFFh may be modified by EECON control
 00 = 000h to FFFh write protected, no addresses may be modified by EECON control
8 kW FLASH memory (PIC16F1936/PIC16LF1936 and PIC16F1937/PIC16LF1937 only):
 11 = Write protection off
 10 = 000h to 1FFh write protected, 200h to 1FFFh may be modified by EECON control
 01 = 000h to FFFh write protected, 1000h to 1FFFh may be modified by EECON control
 00 = 000h to 1FFFh write protected, no addresses may be modified by EECON control
16 kW FLASH memory (PIC16F1938/PIC16LF1938 and PIC16F1939/PIC16LF1939 only):
 11 = Write protection off
 10 = 000h to 1FFh write protected, 200h to 3FFFh may be modified by EECON control
 01 = 000h to 1FFFh write protected, 2000h to 3FFFh may be modified by EECON control
 00 = 000h to 3FFFh write protected, no addresses may be modified by EECON control

- Note 1:** The LVP bit cannot be programmed to '0' when Programming mode is entered via LVP.
Note 2: Reads as '11' on PIC16LF193X only.

4.0 PROGRAM/VERIFY MODE

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted LSb first. Data changes on the rising edge of the ICSPCLK and latched on the falling edge. In Program/Verify mode both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/O's are automatically configured as high-impedance inputs and the address is cleared.

4.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different methods of entering Program/Verify mode via high-voltage:

- VPP – First entry mode
- VDD – First entry mode

4.1.1 VPP – FIRST ENTRY MODE

To enter Program/Verify mode via the VPP-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
2. Raise the voltage on $\overline{\text{MCLR}}$ from 0V to V_{IH} .
3. Raise the voltage on VDD FROM 0V to the desired operating voltage.

The VPP-first entry prevents the device from executing code prior to entering Program/Verify mode. For example, when the Configuration Word has $\overline{\text{MCLR}}$ disabled ($\text{MCLRE} = 0$), the power-up time is disabled ($\text{PWRTE} = 0$), the internal oscillator is selected ($\text{FOSC} = 100$), and RB6 and RB7 are driven by the user application, the device will execute code. Since this may prevent entry, VPP-first entry mode is strongly recommended. See the timing diagram in Figure 8-3.

4.1.2 VDD – FIRST ENTRY MODE

To enter Program/Verify mode via the VDD-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on VDD from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{\text{MCLR}}$ from VDD or below to V_{IH} .

The VDD-first method is useful when programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in Figure 8-2.

4.1.3 PROGRAM/VERIFY MODE EXIT

To exit Program/Verify mode take $\overline{\text{MCLR}}$ to VDD or lower (V_{IL}). See Figures 8-4 and 8-5.

4.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows the PIC16F193X/LF193X devices to be programmed using VDD only, without high voltage. When the LVP bit of the Configuration Word 2 register is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify modes requires the following steps:

1. $\overline{\text{MCLR}}$ is brought to V_{IL} .
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

The key sequence is a specific 32-bit pattern, '0100 1101 0100 0011 0100 1000 0101 0000' (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Least Significant bit of the Least Significant nibble must be shifted in first.

Once the key sequence is complete, $\overline{\text{MCLR}}$ must be held at V_{IL} for as long as Program/Verify mode is to be maintained.

For low-voltage programming timing, see Figures 8-9 and 8-10.

Exiting Program/Verify mode is done by no longer driving $\overline{\text{MCLR}}$ to V_{IL} . See Figures 8-9 and 8-10.

PIC16F193X/LF193X

4.3 Program/Verify Commands

The PIC16F193X and PIC16LF193X implement 13 programming commands, each six bits in length. The commands are summarized in Table 4-1.

Commands that have data associated with them are specified to have a minimum delay of TDLY between the command and the data. After this delay 16 clocks are required to either clock in or clock out the 14-bit data word. The first clock is for the Start bit and the last clock is for the Stop bit.

TABLE 4-1: COMMAND MAPPING FOR PIC16F193X/LF193X

Command	Mapping						Hex	Data/Note
	Binary (MSb ... LSb)							
Load Configuration	x	0	0	0	0	0	00h	0, data (14), 0
Load Data For Program Memory	x	0	0	0	1	0	02h	0, data (14), 0
Load Data For Data Memory	x	0	0	0	1	1	03h	0, data (8), zero (6), 0
Read Data From Program Memory	x	0	0	1	0	0	04h	0, data (14), 0
Read Data From Data Memory	x	0	0	1	0	1	05h	0, data (8), zero (6), 0
Increment Address	x	0	0	1	1	0	06h	—
Reset Address	x	1	0	1	1	0	16h	—
Begin Internally Timed Programming	x	0	1	0	0	0	08h	—
Begin Externally Timed Programming	x	1	1	0	0	0	18h	—
End Externally Timed Programming	x	0	1	0	1	0	0Ah	—
Bulk Erase Program Memory	x	0	1	0	0	1	09h	Internally Timed
Bulk Erase Data Memory	x	0	1	0	1	1	0Bh	Internally Timed
Row Erase Program Memory	x	1	0	0	0	1	11h	Internally Timed

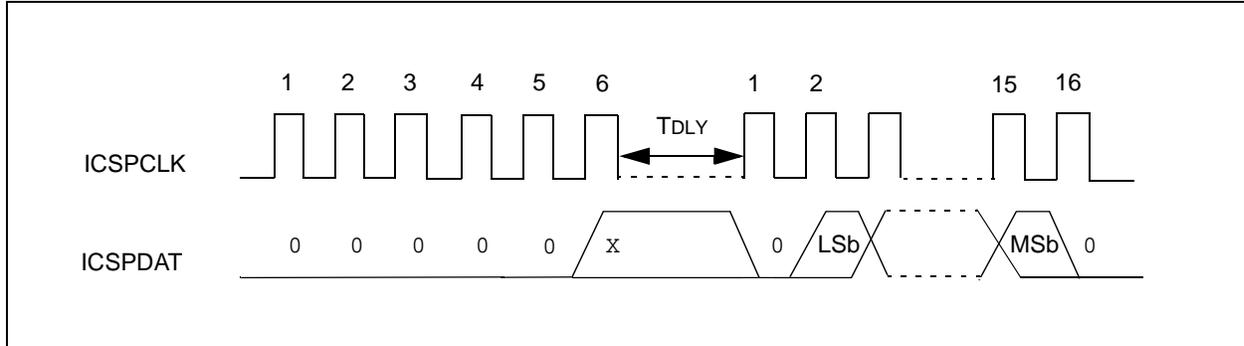
4.3.1 LOAD CONFIGURATION

The Load Configuration command is used to access the configuration memory (User ID Locations, Configuration Words, Calibration Words). The Load Configuration command sets the address to 8000h and loads the data latches with one word of data (see Figure 4-1).

After issuing the Load Configuration command, use the Increment Address command until the proper address to be programmed is reached. The address is then programmed by issuing either the Begin Internally Timed Programming or Begin Externally Timed Programming command.

The only way to get back to the program memory (address 0) is to exit Program/Verify mode or issue the Reset Address command after the configuration memory has been accessed by the Load Configuration command.

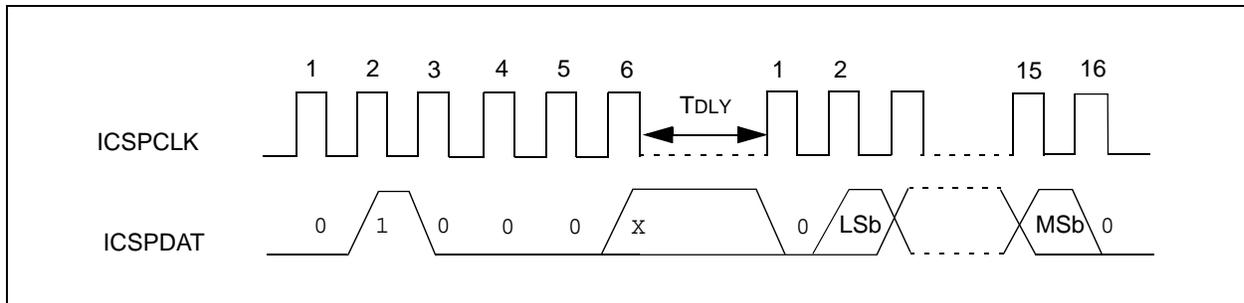
FIGURE 4-1: LOAD CONFIGURATION



4.3.2 LOAD DATA FOR PROGRAM MEMORY

The Load Data for Program Memory command is used to load one 14-bit word into the data latches. The word programs into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming command is issued (see Figure 4-2).

FIGURE 4-2: LOAD DATA FOR PROGRAM MEMORY

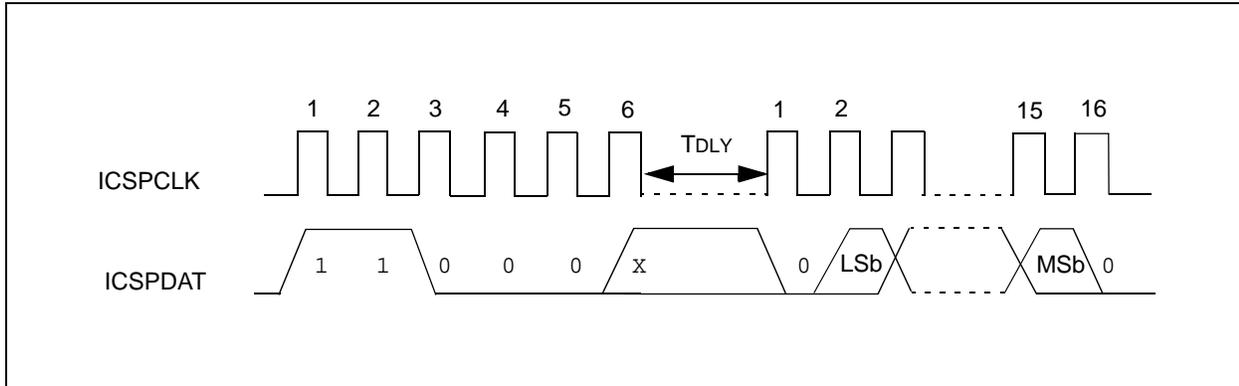


PIC16F193X/LF193X

4.3.3 LOAD DATA FOR DATA MEMORY

The Load Data for Data Memory command will load a 14-bit “data word” when 16 cycles are applied. However, the data memory is only 8 bits wide and thus, only the first 8 bits of data after the Start bit will be programmed into the data memory. It is still necessary to cycle the clock the full 16 cycles in order to allow the internal circuitry to reset properly (see Figure 4-3).

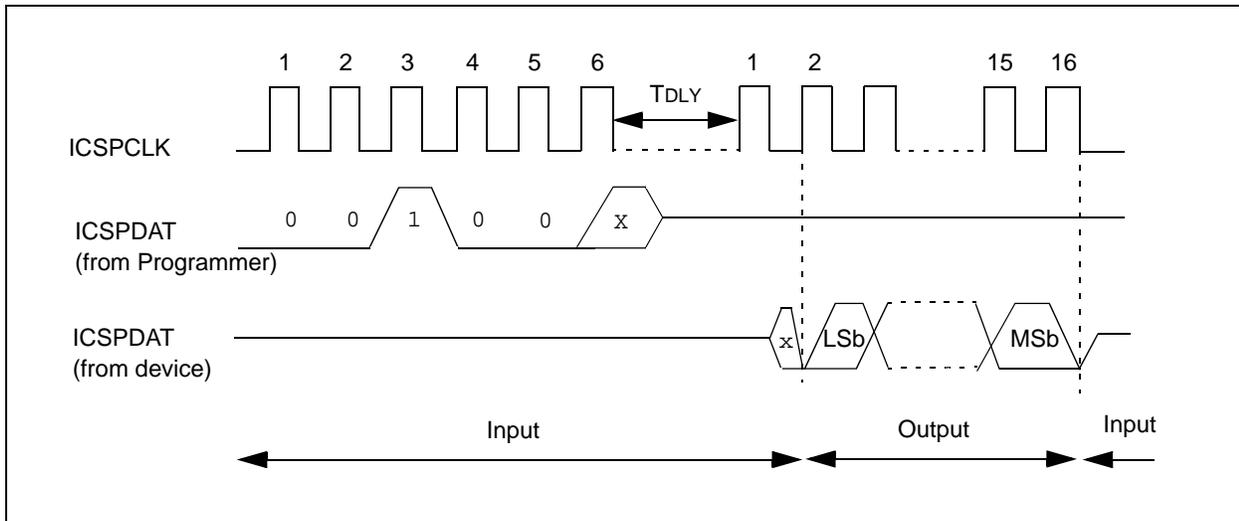
FIGURE 4-3: LOAD DATA FOR DATA MEMORY COMMAND



4.3.4 READ DATA FROM PROGRAM MEMORY

The Read Data from Program Memory command will transmit data bits out of the program memory map currently accessed, starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the first falling clock edge, and it will revert to Input mode (high-impedance) after the 16th falling edge of the clock. If the program memory is code-protected (\overline{CP}), the data will be read as zeros (see Figure 4-4).

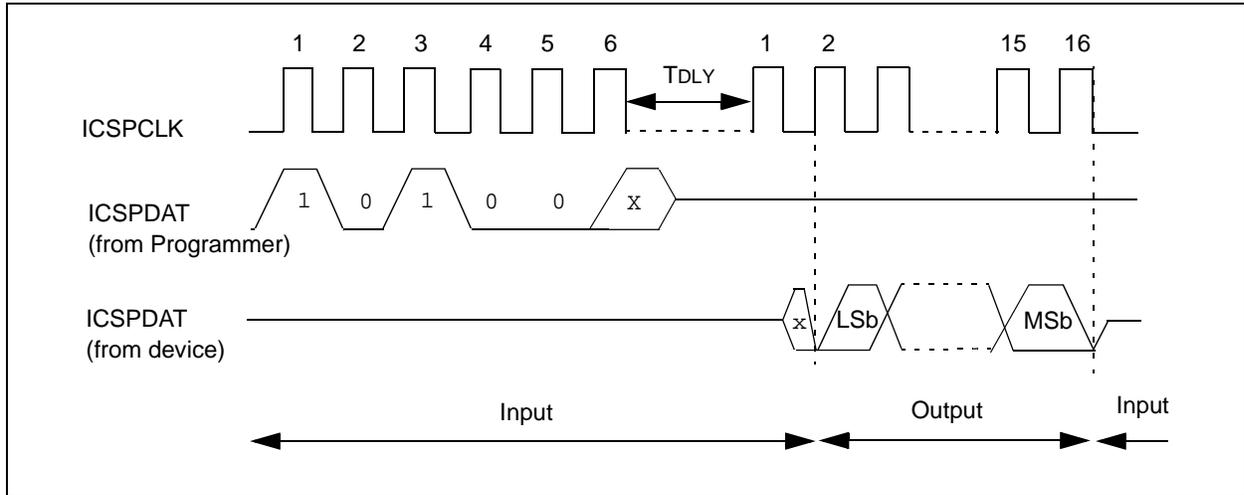
FIGURE 4-4: READ DATA FROM PROGRAM MEMORY



4.3.5 READ DATA FROM DATA MEMORY

The Read Data from Data Memory command will transmit data bits out of the data memory starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the second rising edge, and it will revert to Input mode (high-impedance) after the 16th rising edge. The data memory is 8 bits wide, and therefore, only the first 8 bits that are output are actual data. If the data memory is code-protected, the data is read as all zeros. A timing diagram of this command is shown in Figure 4-5.

FIGURE 4-5: READ DATA FROM DATA MEMORY COMMAND

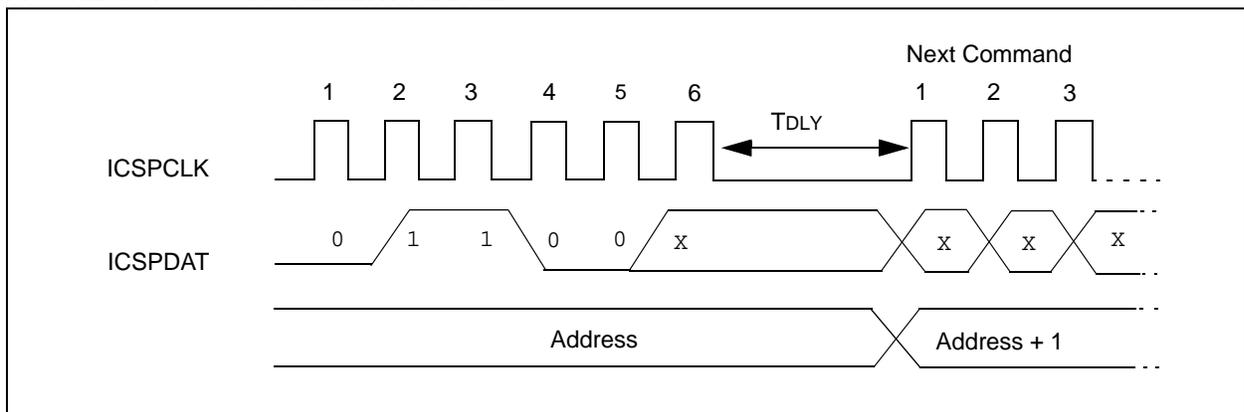


4.3.6 INCREMENT ADDRESS

The address is incremented when this command is received. It is not possible to decrement the address. To reset this counter, the user must use the Reset Address command or exit Program/Verify mode and re-enter it.

If the address is incremented from address 7FFFh, it will wrap around to location 0000h. If the address is incremented from FFFFh, it will wrap around to location 8000h.

FIGURE 4-6: INCREMENT ADDRESS

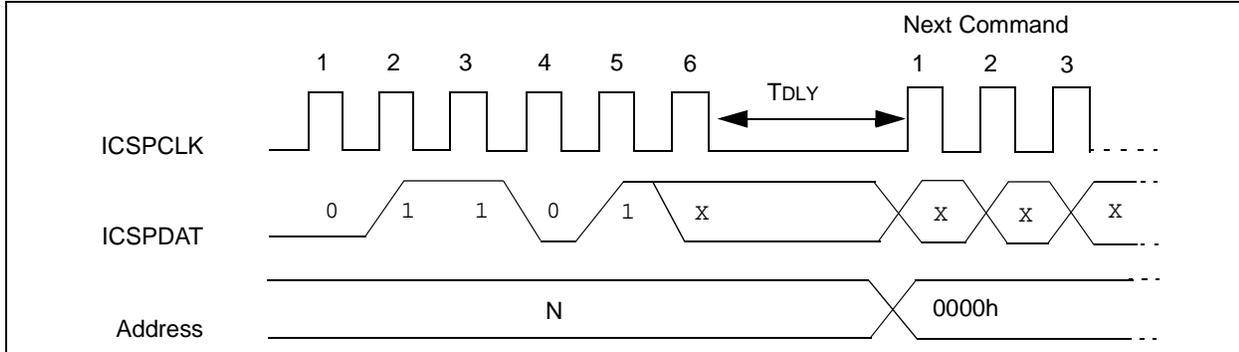


PIC16F193X/LF193X

4.3.7 RESET ADDRESS

The Reset Address command will reset the address to 0000h, regardless of the current value. The address is used in program memory or the configuration memory.

FIGURE 4-7: RESET ADDRESS



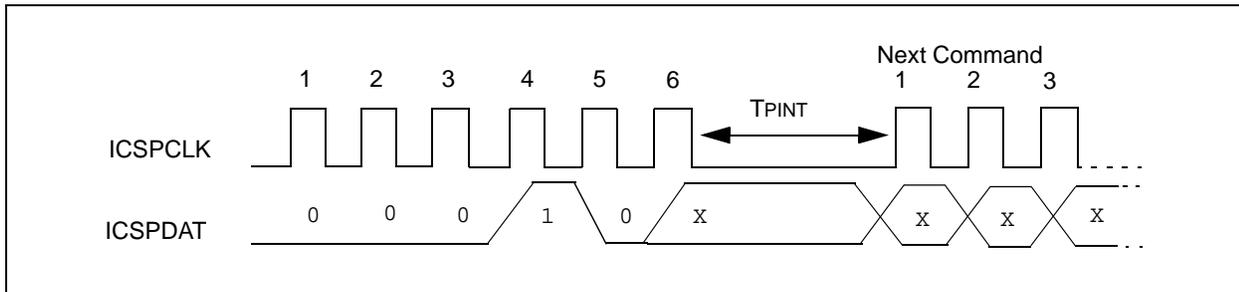
4.3.8 BEGIN INTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. An internal timing mechanism executes the write. The user must allow for the program cycle time, TPINT, for the programming to complete.

The End Externally Timed Programming command is not needed when the Begin Internally Timed Programming is used to start the programming.

The program memory address that is being programmed is not erased prior to being programmed. However, the EEPROM memory address that is being programmed is erased prior to being programmed with internally timed programming.

FIGURE 4-8: BEGIN INTERNALLY TIMED PROGRAMMING

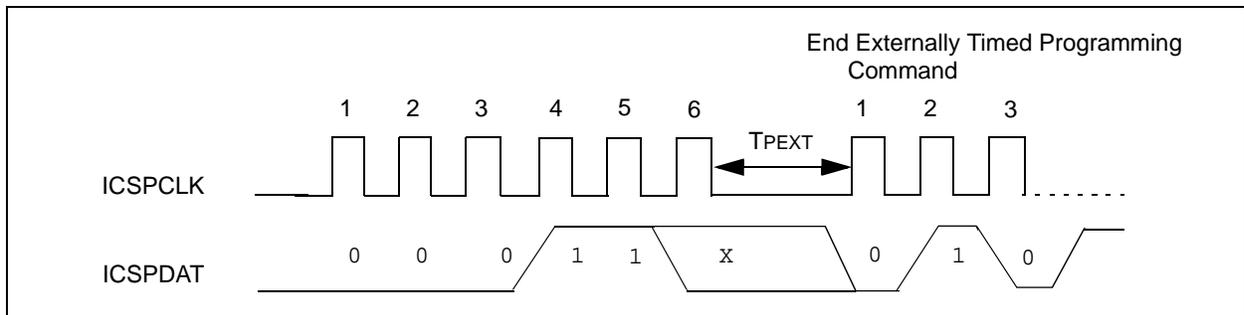


4.3.9 BEGIN EXTERNALLY TIMED PROGRAMMING

A Load Configuration, Load Data for Program Memory or Load Data for Data Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. To complete the programming the End Externally Timed Programming command must be sent in the specified time window defined by TPEXT. No internal erase is performed for the data EEPROM, therefore, the device should be erased prior to executing this command.

The Begin Externally Timed Programming command can not be used for programming the Configuration Words (see Figure 4-9).

FIGURE 4-9: BEGIN EXTERNALLY TIMED PROGRAMMING

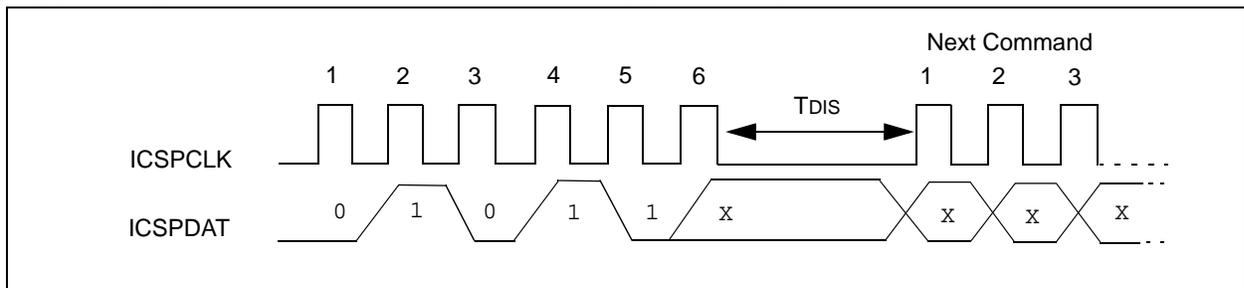


4.3.10 END EXTERNALLY TIMED PROGRAMMING

This command is required after a Begin Externally Timed Programming command is given. This command must be sent within the time window specified by TPEXT after the Begin Externally Timed Programming command is sent.

After sending the End Externally Timed Programming command, an additional delay (TDIS) is required before sending the next command. This delay is longer than the delay ordinarily required between other commands (see Figure 4-10).

FIGURE 4-10: END EXTERNALLY TIMED PROGRAMMING



PIC16F193X/LF193X

4.3.11 BULK ERASE PROGRAM MEMORY

The Bulk Erase Program Memory command performs two different functions dependent on the current state of the address.

Address 0000h-7FFFh:

- Program Memory is erased
- Configuration words are erased
- If $\overline{CPD} = 0$, Data Memory is erased

Address 8000h-8008h:

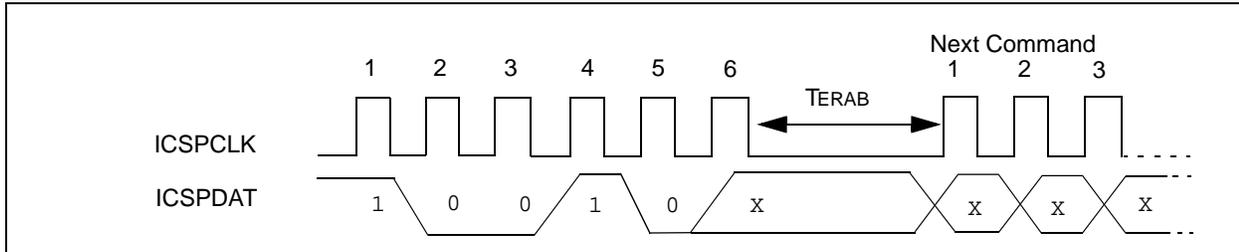
- Program Memory is erased
- Configuration Words are erased
- User ID Locations are erased
- If $\overline{CPD} = 0$, Data Memory is erased

A Bulk Erase Program Memory command should not be issued when the address is greater than 8008h.

After receiving the Bulk Erase Program Memory command the erase will not complete until the time interval, T_{ERAB} , has expired.

Note: The code protection Configuration bit (\overline{CP}) has no effect on the Bulk Erase Program Memory command.

FIGURE 4-11: BULK ERASE PROGRAM MEMORY



4.3.12 BULK ERASE DATA MEMORY

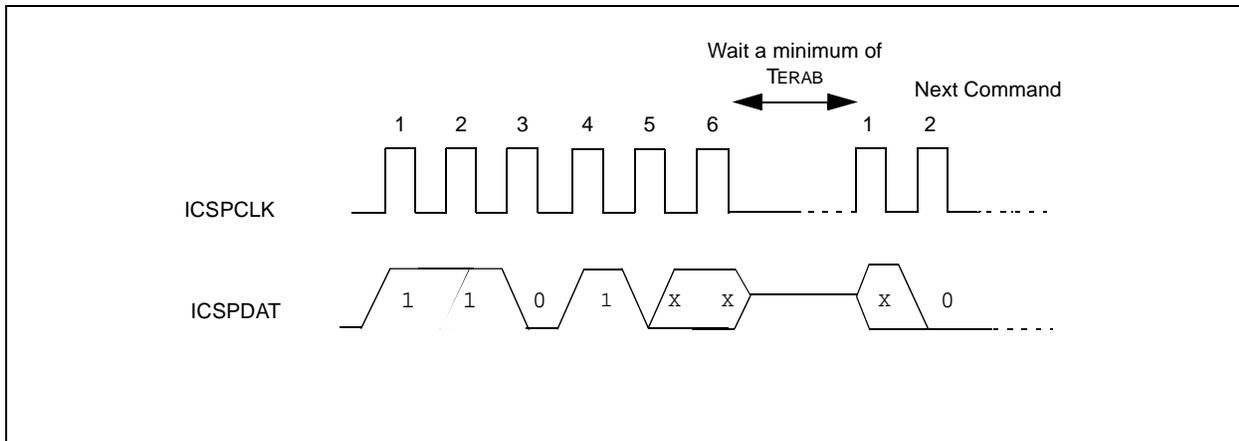
To perform an erase of the data memory, after a Bulk Erase Data Memory command, wait a minimum of T_{ERAB} to complete Bulk Erase.

To erase data memory when data code-protect is active ($\overline{CPD} = 0$), the Bulk Erase Program Memory command should be used.

After receiving the Bulk Erase Data Memory command, the erase will not complete until the time interval, T_{ERAB} , has expired.

Note: Data memory will not erase if code-protected ($\overline{CPD} = 0$).

FIGURE 4-12: BULK ERASE DATA MEMORY COMMAND

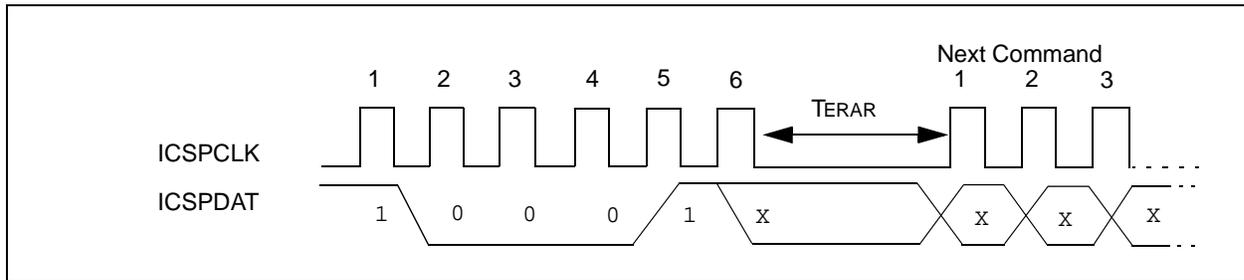


4.3.13 ROW ERASE PROGRAM MEMORY

The Row Erase Program Memory command will erase an individual row. A row of program memory consists of 32 consecutive 14-bit words. A row is addressed by the address PC<15:5>. If the program memory is code-protected the Row Erase Program Memory command will be ignored. When the address is 8000h-8008h the Row Erase Program Memory command will only erase the user ID locations regardless of the setting of the CP Configuration bit.

After receiving the Row Erase Program Memory command the erase will not complete until the time interval, TERAR, has expired.

FIGURE 4-13: ROW ERASE PROGRAM MEMORY



PIC16F193X/LF193X

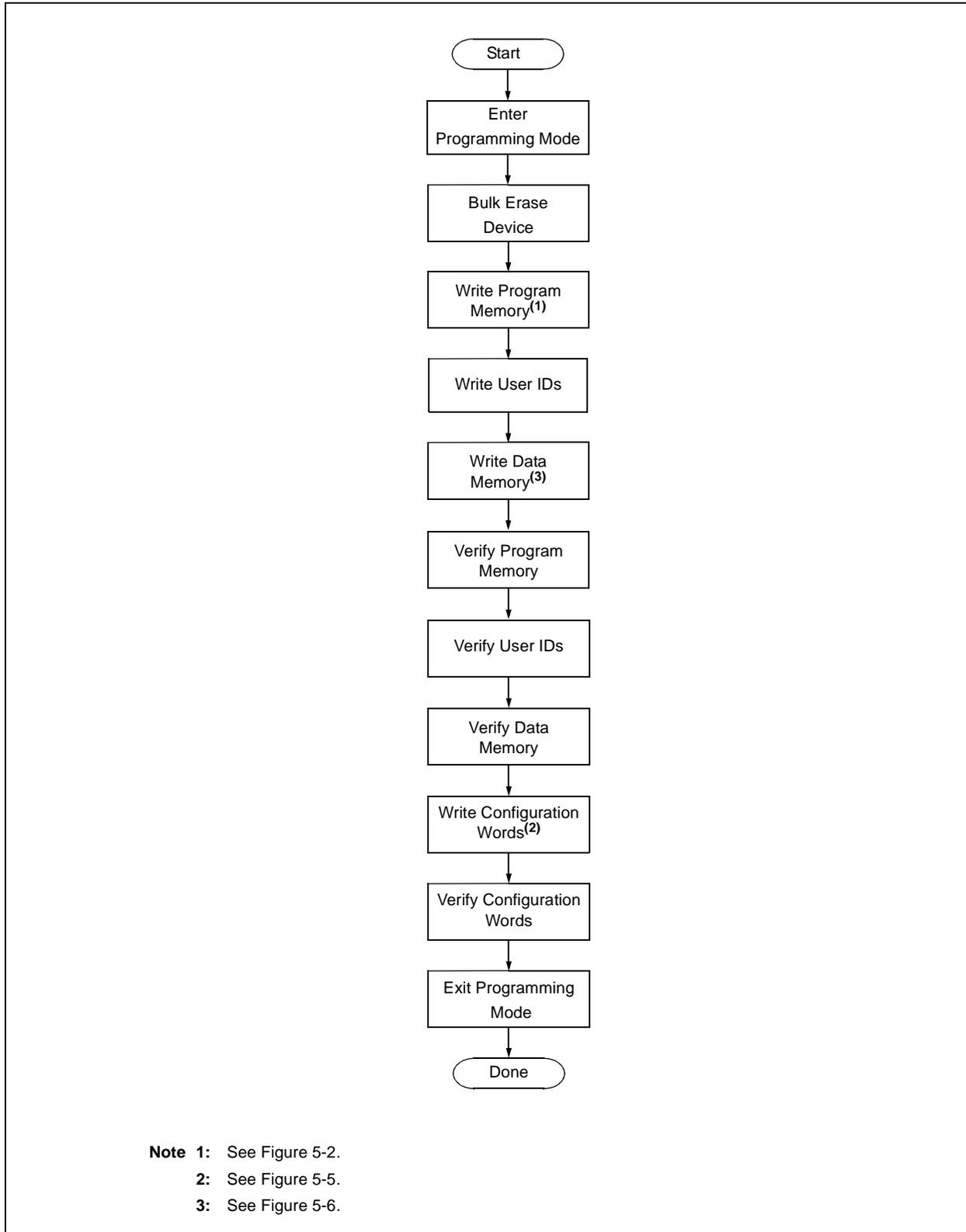
5.0 PROGRAMMING ALGORITHMS

The PIC16F193X/PIC16LF193X devices have the capability of storing eight 14-bit words in its data latches. The data latches are internal to the PIC16F193X/PIC16LF193X devices and are only used for programming. The data latches allow the user to program up to eight program words with a single Begin Externally Timed Programming or Begin Internally Timed Programming command. The Load Program Data or the Load Configuration command is used to load a single data latch. The data latch will hold the data until the Begin Externally Timed Programming or Begin Internally Timed Programming command is given.

The data latches are aligned with the 3 LSb of the address. The address at the time the Begin Externally Timed Programming or Begin Internally Timed Programming command is given will determine which location(s) in memory are written. Writes can not cross a physical eight-word boundary. For example, attempting to write from address 0002h-0009h will result in data being written to 0008h-000Fh.

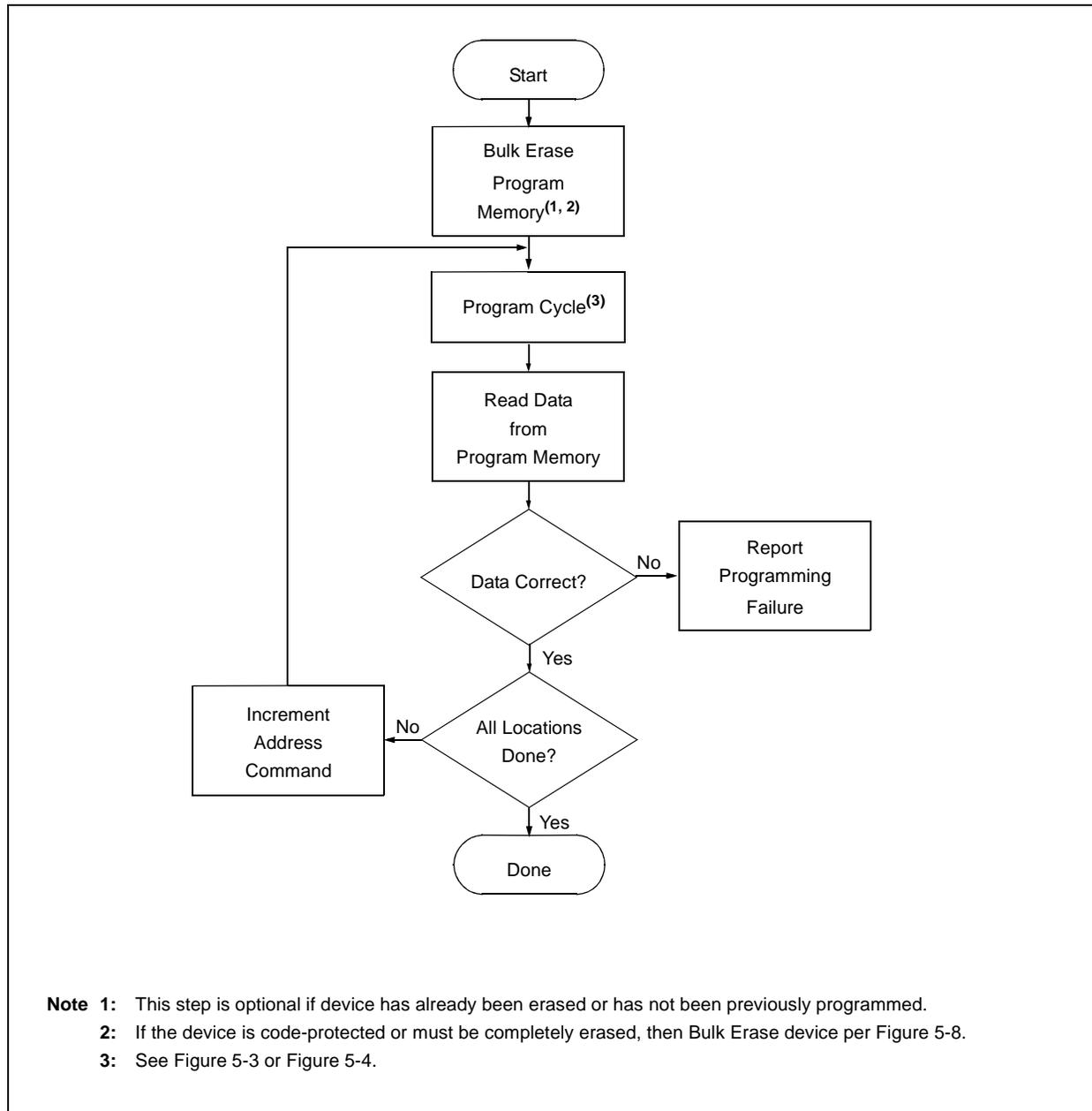
If more than 8 data latches are written without a Begin Externally Timed Programming or Begin Internally Timed Programming command the data in the data latches will be overwritten. The following figures show the recommended flowcharts for programming.

FIGURE 5-1: DEVICE PROGRAM/VERIFY FLOWCHART



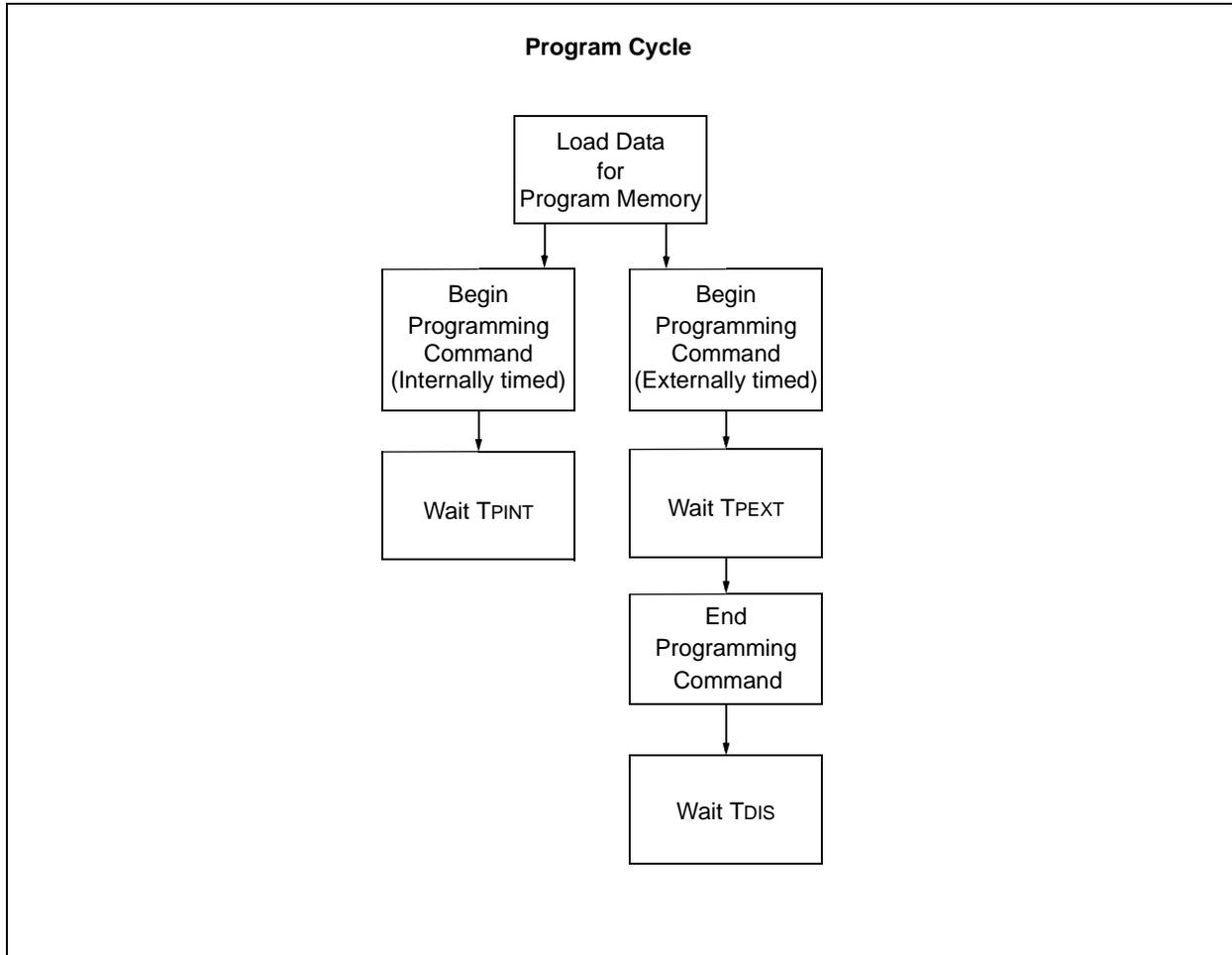
PIC16F193X/LF193X

FIGURE 5-2: PROGRAM MEMORY FLOWCHART



- Note 1:** This step is optional if device has already been erased or has not been previously programmed.
- Note 2:** If the device is code-protected or must be completely erased, then Bulk Erase device per Figure 5-8.
- Note 3:** See Figure 5-3 or Figure 5-4.

FIGURE 5-3: ONE-WORD PROGRAM CYCLE



PIC16F193X/LF193X

FIGURE 5-4: MULTIPLE-WORD PROGRAM CYCLE

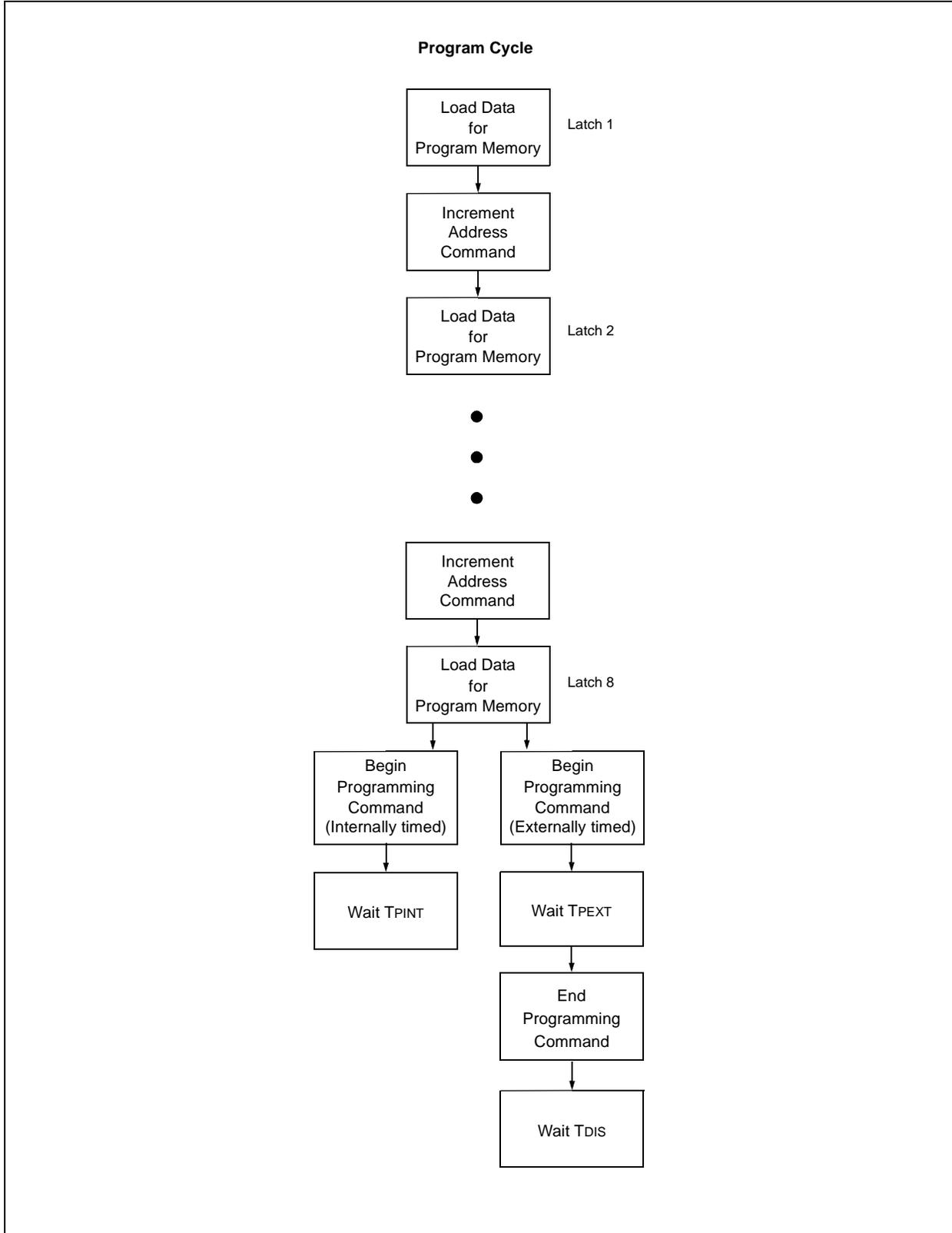
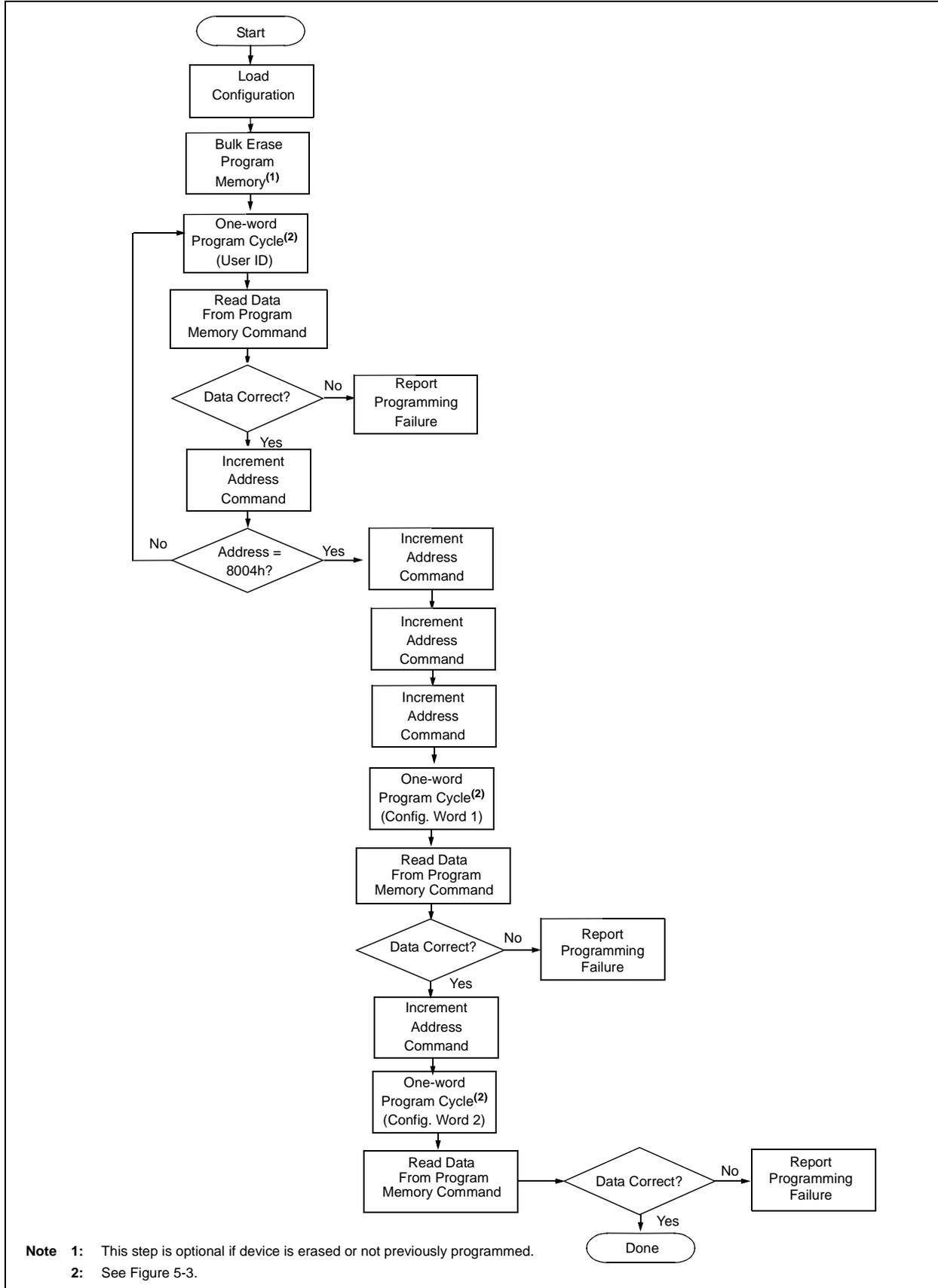


FIGURE 5-5: CONFIGURATION MEMORY PROGRAM FLOWCHART



PIC16F193X/LF193X

FIGURE 5-6: DATA MEMORY PROGRAM FLOWCHART

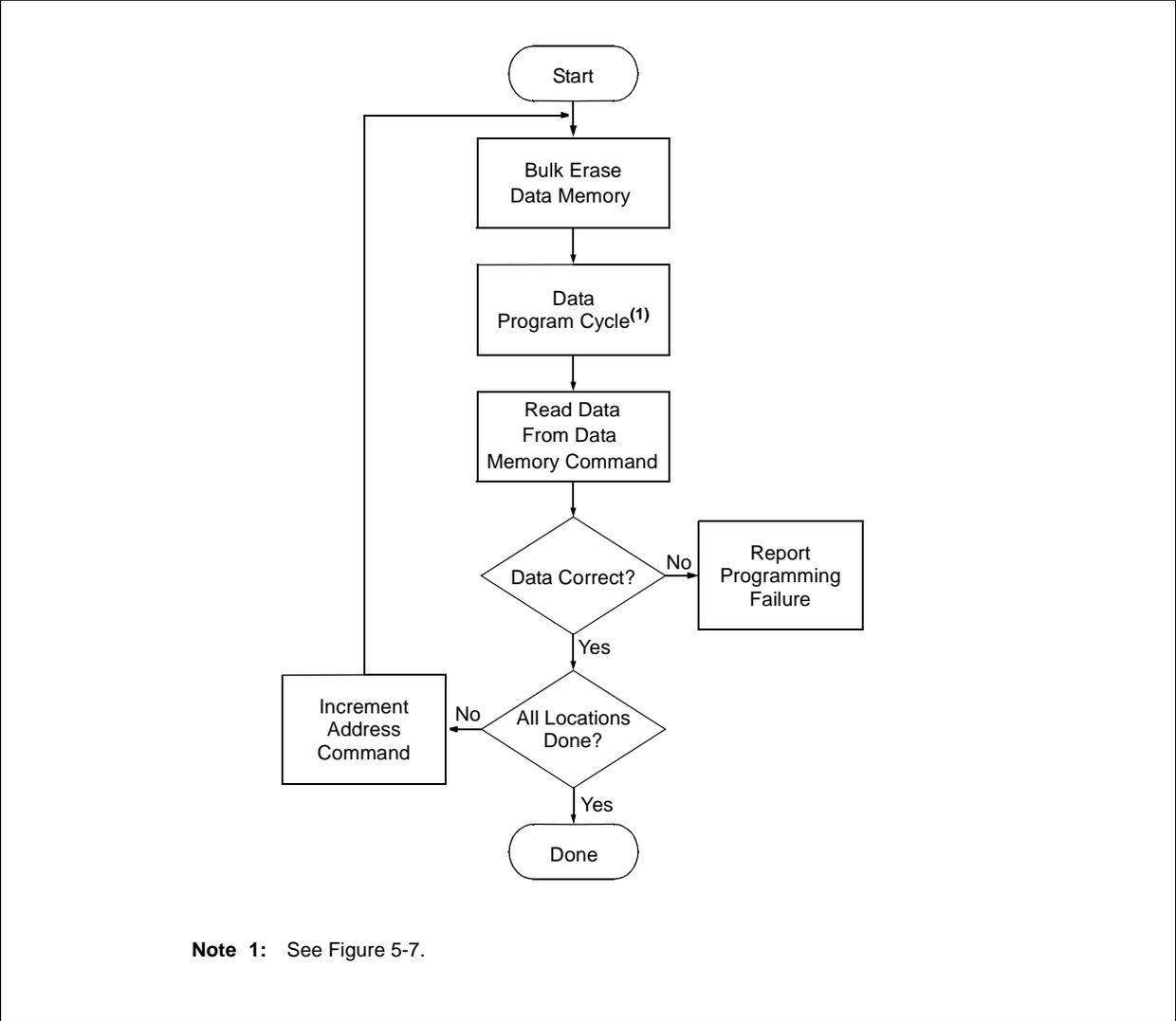


FIGURE 5-7: DATA MEMORY PROGRAM CYCLE

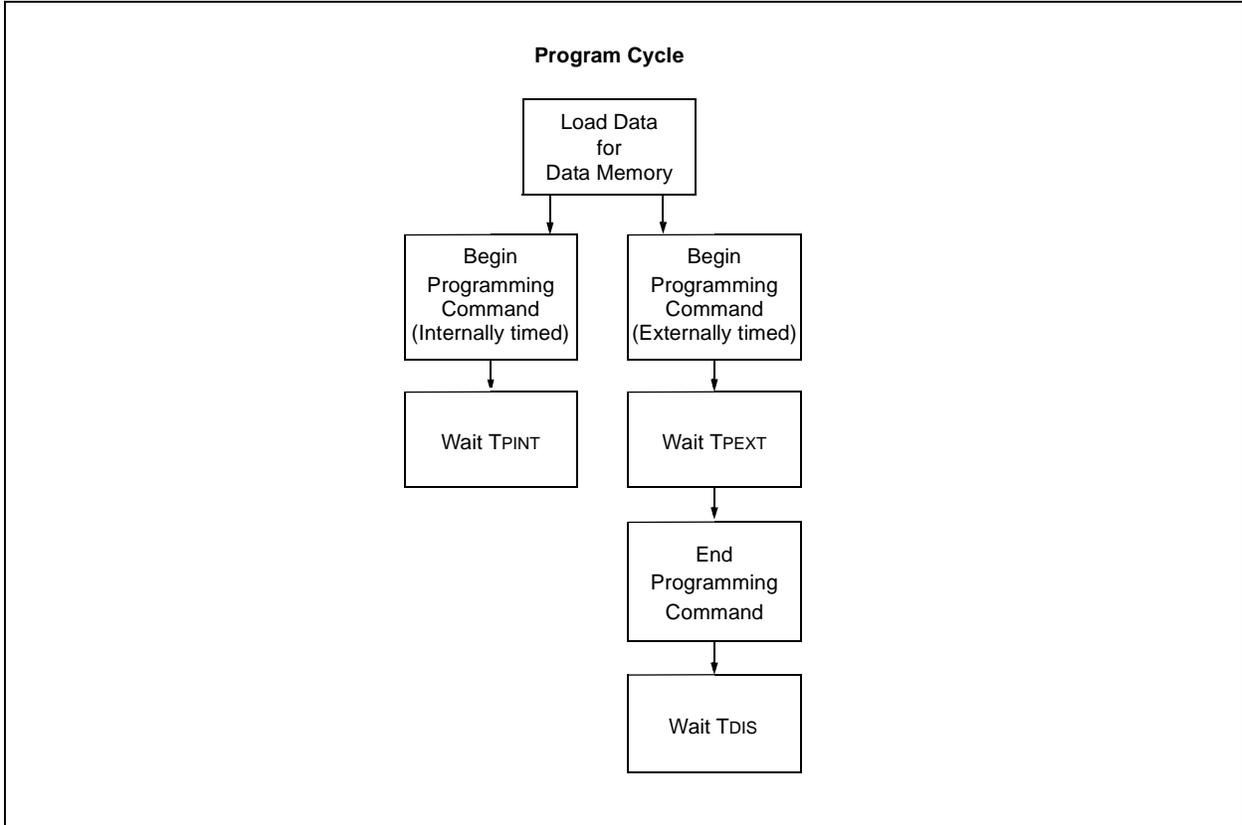
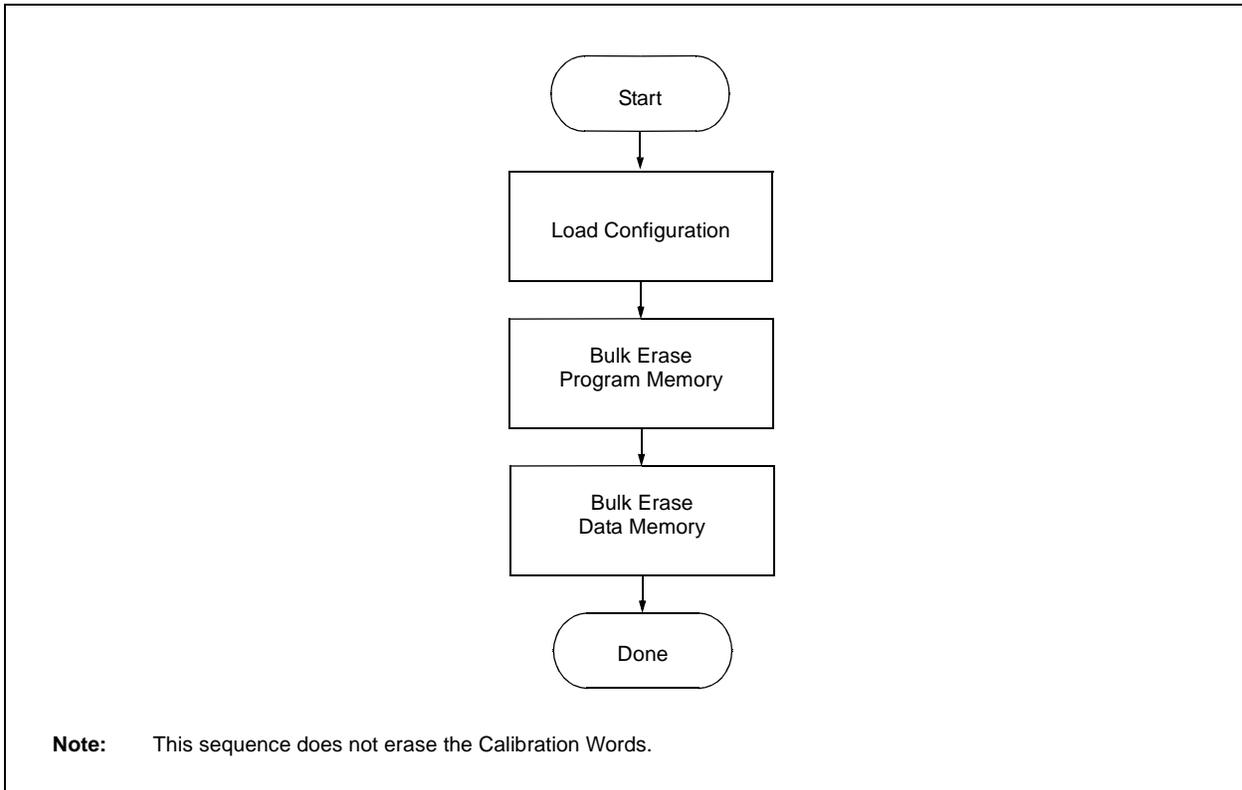


FIGURE 5-8: ERASE FLOWCHART



PIC16F193X/LF193X

6.0 CODE PROTECTION

Code protection is controlled using the \overline{CP} bit in Configuration Word 1. When code protection is enabled, all program memory locations (0000h-7FFFh) read as all '0'. Further programming is disabled for the program memory (0000h-7FFFh).

Data memory is protected with its own Code-Protect bit (\overline{CPD}). When data code-protection is enabled ($\overline{CPD} = 0$), all data memory locations read as '0'. Further programming is disabled for the data memory. Data memory can still be programmed and read during program execution.

The user ID locations and Configuration Words can be programmed and read out regardless of the code protection settings.

6.1 Program Memory

Code protection is enabled by programming the \overline{CP} bit in Configuration Word 1 register to '0'.

The only way to disable code protection is to use the Bulk Erase Program Memory command.

6.2 Data Memory

Data memory protection is enabled by programming the \overline{CPD} bit in Configuration Word 1 register to '0'.

The only way to disable code protection is to use the Bulk Erase Program Memory command.

Note: To ensure system security, if \overline{CPD} bit = 0, the Bulk Erase Program Memory command will also erase data memory.

7.0 HEX FILE USAGE

In the hex file there are two bytes per program word stored in the Intel[®] INHX32 hex format. Data is stored LSB first, MSB second. Because there are two bytes per word, the addresses in the hex file are 2x the address in program memory. (Example: The Configuration Word 1 is stored at 8007h on the PIC16F193X/PIC16LF193X. In the hex file this will be referenced as 1000Eh-1000Fh).

7.1 Configuration Word

To allow portability of code, it is strongly recommended that the programmer is able to read the Configuration Words and user ID locations from the hex file. If the Configuration Words information was not present in the hex file, a simple warning message may be issued. Similarly, while saving a hex file, Configuration Words and user ID information should be included.

7.2 Device ID and Revision

If a device ID is present in the hex file at 1000Ch-1000Dh (8006h on the part), the programmer should verify the device ID (excluding the revision) against the value read from the part. On a mismatch condition the programmer should generate a warning message.

7.3 Data EEPROM

The programmer should be able to read data memory information from a hex file and write data memory contents to a hex file.

The physical address range of the 256 data memory is 0000h-00FFh. However, these addresses are logically mapped to address 1E000h-1E1FFh in the hex file. This provides a way of differentiating between the data and program memory locations in this range. The format for data memory storage is one data byte per address location, LSb aligned.

7.4 Checksum Computation

The checksum is calculated by two different methods dependent on the setting of the \overline{CP} Configuration bit.

TABLE 7-1: CONFIGURATION WORD MASK VALUES

Device	Config. Word 1 Mask	Config. Word 2 Mask
PIC16F1933	3FFFh	3733h
PIC16LF1933	3FFFh	3703h
PIC16F1934	3FFFh	3733h
PIC16LF1934	3FFFh	3703h
PIC16F1936	3FFFh	3733h
PIC16LF1936	3FFFh	3703h
PIC16F1937	3FFFh	3733h
PIC16LF1937	3FFFh	3703h
PIC16F1938	3FFFh	3733h
PIC16LF1938	3FFFh	3703h
PIC16F1939	3FFFh	3733h
PIC16LF1939	3FFFh	3703h

7.4.1 PROGRAM CODE PROTECTION DISABLED

With the program code protection disabled, the checksum is computed by reading the contents of the PIC16F193X/PIC16LF193X program memory locations and adding up the program memory data starting at address 0000h, up to the maximum user addressable location (e.g., 1FFFh for the PIC16F1936). Any Carry bit exceeding 16 bits are ignored. Additionally, the relevant bits of the Configuration Words are added to the checksum. All unimplemented Configuration bits are masked to '0'.

Note: Data memory does not effect the checksum.

EXAMPLE 7-1: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION DISABLED (PIC16F1936)

PIC16F1936	Sum of Memory addresses 0000h-1FFFh	2534h
	Configuration Word 1	2D83h
	Configuration Word 1 mask	3FFFh
	Configuration Word 2	3AEFh
	Configuration Word 2 mask	3733h
	Checksum = 2534h + (2D83h and 3FFFh) + (3AEFh and 3733h)	
	= 2534h + 2D83h + 3223h	
	= 84DAh	

EXAMPLE 7-2: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION DISABLED (PIC16LF1936)

PIC16LF1936	Sum of Memory addresses 0000h-1FFFh	2534h
	Configuration Word 1	2D83h
	Configuration Word 1 mask	3FFFh
	Configuration Word 2	3AFFh
	Configuration Word 2 mask ⁽¹⁾	3703h
	Checksum = 2534h + (2D83h and 3FFFh) + (3AFFh and 3703h)	
	= 2534h + 2D83h + 3203h	
	= 84BAh	
Note 1: In PIC16LF193X devices, the VCAPEN<1:0> bits are not implemented in Configuration Word 2 and the Configuration Word 2 mask is 3703h.		

PIC16F193X/LF193X

7.4.2 PROGRAM CODE PROTECTION ENABLED

With the program code protection enabled the checksum is computed in the following manner. The Configuration Words are summed (all unimplemented Configuration bits are masked to '0') with the Least Significant nibble of the user ID's.

Note: Data memory does not effect the checksum.

EXAMPLE 7-3: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED (PIC16F1936)

PIC16F1936	Configuration Word 1	2C03h
	Configuration Word 1 mask	3FFFh
	Configuration Word 2	3AECh
	Configuration Word 2 mask	3733h
	User ID (8000h)	0123h
	User ID (8001h)	4567h
	User ID (8002h)	89ABh
	User ID (8003h)	CDEFh
	Checksum	= (2C03h and 3FFFh) + (3AECh and 3733h) + (0123h and 000Fh) + (4567h and 000Fh) + (89ABh and 000Fh) +(CDEFh and 000Fh)
		= 2C03h +3220h + 0003h + 0007h + 000Bh + 000Fh
		= 5E47h

EXAMPLE 7-4: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED (PIC16LF1936)

PIC16LF1936	Configuration Word 1	2C03h
	Configuration Word 1 mask	3FFFh
	Configuration Word 2	3AFCh
	Configuration Word 2 mask ⁽¹⁾	3703h
	User ID (8000h)	0123h
	User ID (8001h)	4567h
	User ID (8002h)	89ABh
	User ID (8003h)	CDEFh
	Checksum	= (2C03h and 3FFFh) + (3AFCh and 3703h) + (0123h and 000Fh) + (4567h and 000Fh) + (89ABh and 000Fh) +(CDEFh and 000Fh)
		= 2C03h +3200h + 0003h + 0007h + 000Bh + 000Fh
		= 5E27h

Note 1: In PIC16LF193X devices, the VCAPEN<1:0> bits are not implemented in Configuration Word 2 and the Configuration Word 2 mask is 3703h.

PIC16F193X/LF193X

8.0 ELECTRICAL SPECIFICATIONS

Refer to device specific data sheet for absolute maximum ratings.

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$					
Sym.	Characteristics	Min.	Typ.	Max.	Units	Conditions/Comments	
Supply Voltages and currents							
VDD	VDD						
	Read/Write and Row Erase operations	PIC16F193X	2.1	—	5.5	V	
		PIC16LF193X	2.1	—	3.6	V	
	Bulk Erase operations	PIC16F193X	2.7	—	5.5	V	
PIC16LF193X		2.7	—	3.6	V		
IDDI	Current on VDD, Idle	—	—	1.0	mA		
IDDP	Current on VDD, Programming	—	—	3.0	mA		
VPP							
IPP	Current on MCLR/VPP	—	—	600	μA		
VIHH	High voltage on MCLR/VPP for Program/Verify mode entry	8.0	—	9.0	V		
TVHHR	MCLR rise time (V_{IL} to V_{IHH}) for Program/Verify mode entry	—	—	1.0	μs		
I/O pins							
VIH	(ICSPCLK, ICSPDAT, MCLR/VPP) input high level	0.8 VDD	—	—	V		
VIL	(ICSPCLK, ICSPDAT, MCLR/VPP) input low level	—	—	0.2 VDD	V		
VOH	ICSPDAT output high level	VDD-0.7 VDD-0.7 VDD-0.7	—	—	V	IOH = 3.5 mA, VDD = 5V IOH = 3 mA, VDD = 3.3V IOH = 2 mA, VDD = 1.8V	
VOL	ICSPDAT output low level	—	—	VSS+0.6 VSS+0.6 VSS+0.6	V	IOH = 8 mA, VDD = 5V IOH = 6 mA, VDD = 3.3V IOH = 3 mA, VDD = 1.8V	
Programming mode entry and exit							
TENTS	Programming mode entry setup time: ICSPCLK, ICSPDAT setup time before VDD or MCLR \uparrow	100	—	—	ns		
TENTH	Programming mode entry hold time: ICSPCLK, ICSPDAT hold time after VDD or MCLR \uparrow	250	—	—	μs		
Serial Program/Verify							
TCKL	Clock Low Pulse Width	100	—	—	ns		
TCKH	Clock High Pulse Width	100	—	—	ns		
Tds	Data in setup time before clock \downarrow	100	—	—	ns		
TdH	Data in hold time after clock \downarrow	100	—	—	ns		
Tco	Clock \uparrow to data out valid (during a Read Data command)	0	—	80	ns		
TLZD	Clock \downarrow to data low-impedance (during a Read Data command)	0	—	80	ns		
THZD	Clock \downarrow to data high-impedance (during a Read Data command)	0	—	80	ns		
TDLY	Data input not driven to next clock input (delay required between command/data or command/command)	1.0	—	—	μs		
TERAB	Bulk Erase cycle time	—	—	5	ms		
TERAR	Row Erase cycle time	—	—	2.5	ms		
TPINT	Internally timed programming operation time	—	—	2.5	ms	Program memory Configuration words	
		—	—	5	ms		
TPEXT	Externally timed programming pulse	1.0	—	2.1	ms		
TDIS	Time delay from program to compare (HV discharge time)	100	—	—	μs		
TEXIT	Time delay when exiting Program/Verify mode	1	—	—	μs		

PIC16F193X/LF193X

8.1 AC Timing Diagrams

FIGURE 8-2: PROGRAMMING MODE ENTRY – V_{DD} FIRST

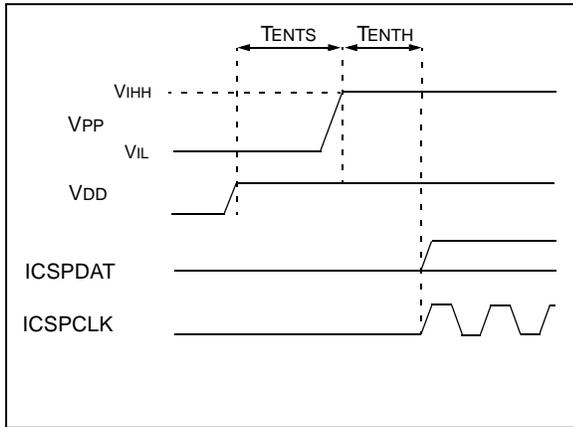


FIGURE 8-3: PROGRAMMING MODE ENTRY – V_{PP} FIRST

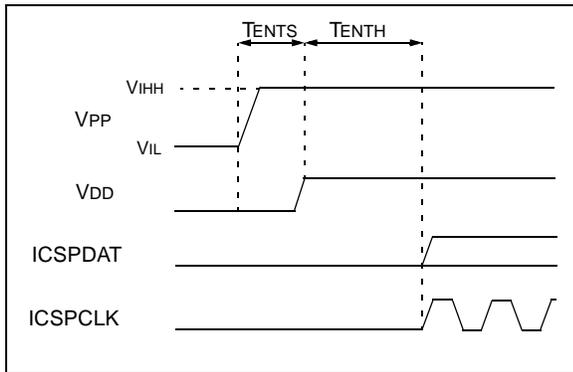


FIGURE 8-4: PROGRAMMING MODE EXIT – V_{PP} LAST

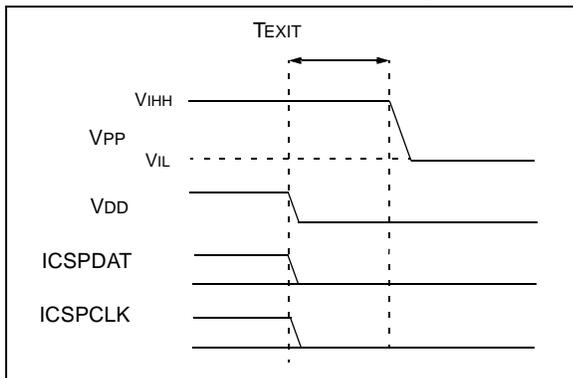


FIGURE 8-5: PROGRAMMING MODE EXIT – V_{DD} LAST

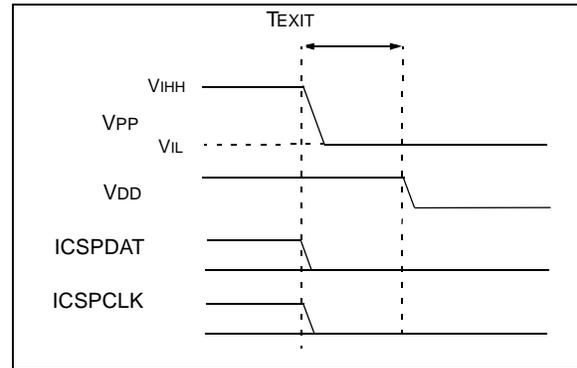


FIGURE 8-6: CLOCK AND DATA TIMING

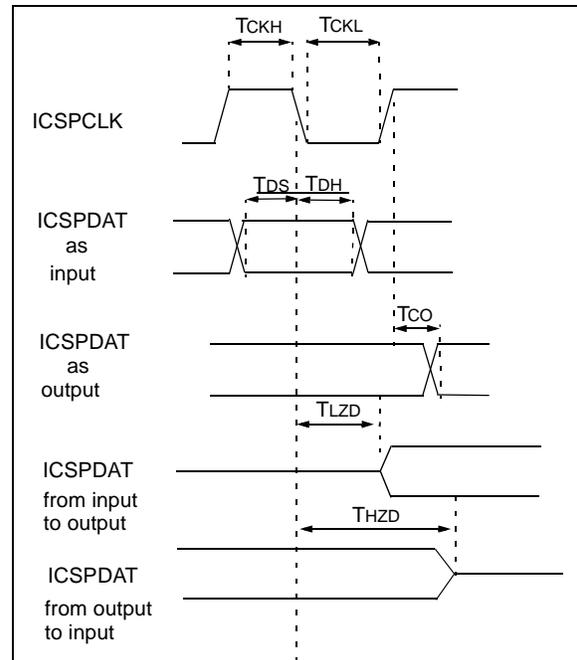


FIGURE 8-7: WRITE COMMAND-PAYLOAD TIMING

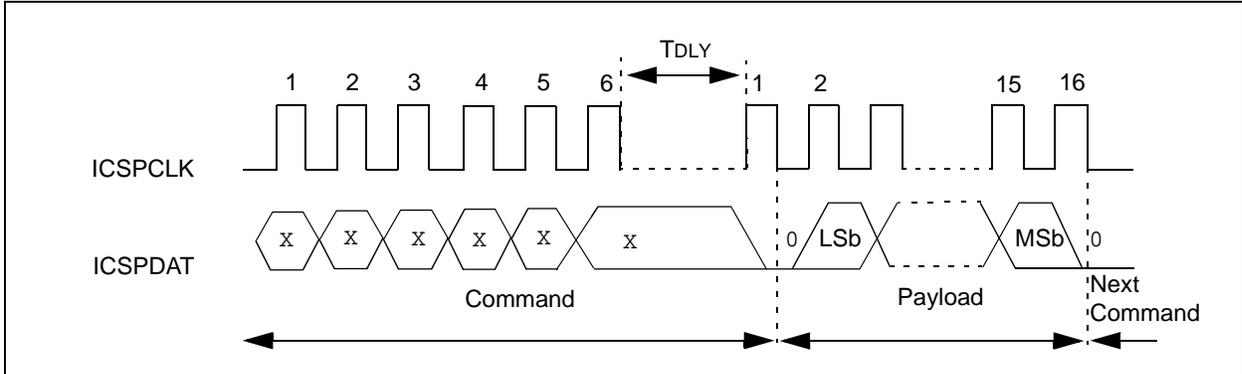
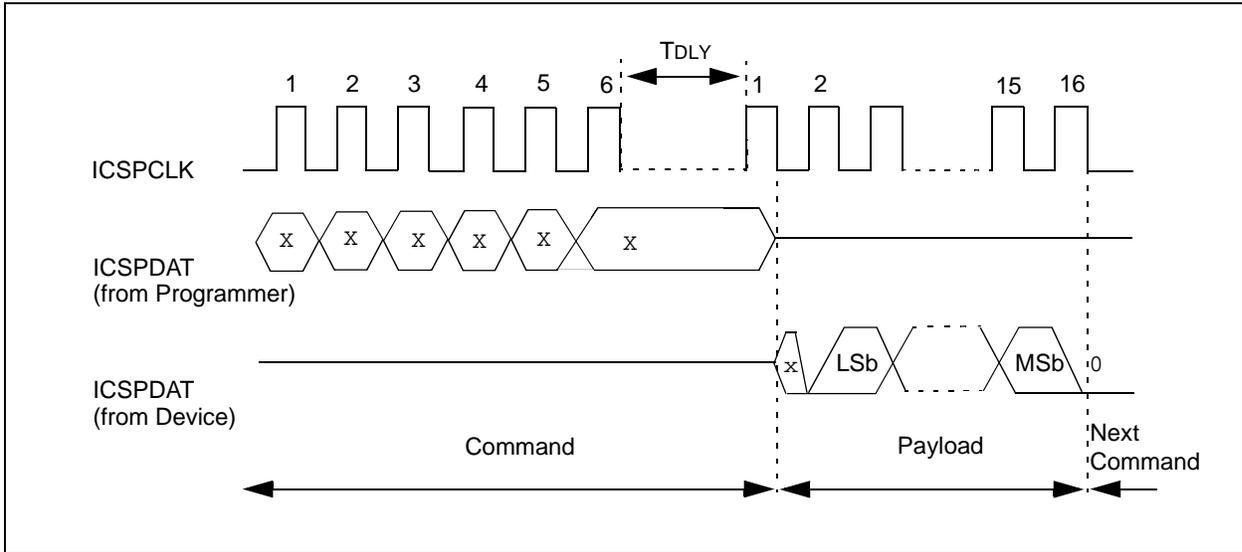


FIGURE 8-8: READ COMMAND-PAYLOAD TIMING



PIC16F193X/LF193X

FIGURE 8-9: LVP ENTRY (POWERING UP)

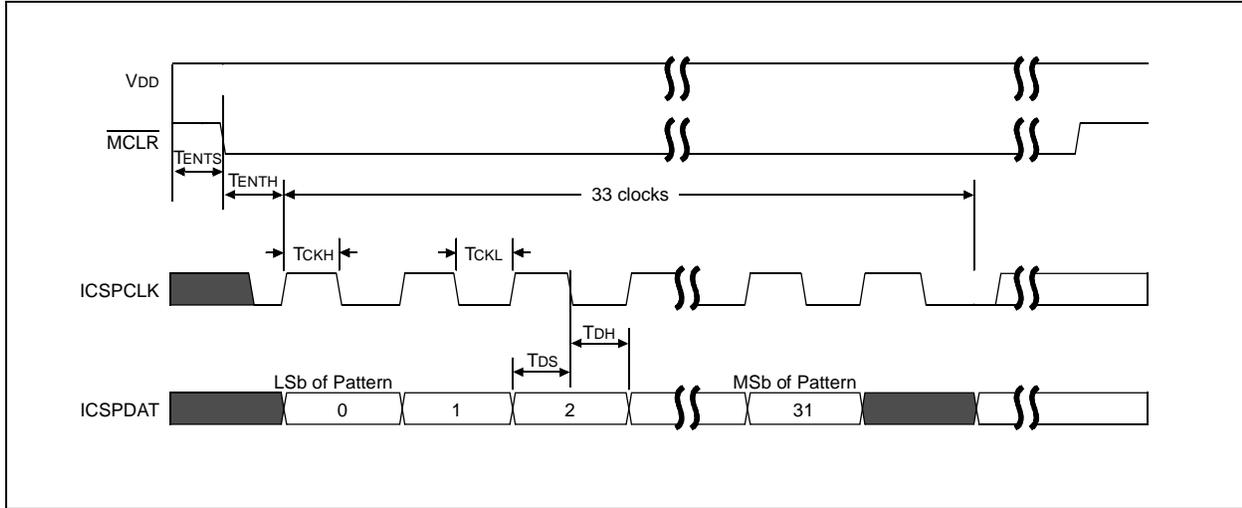
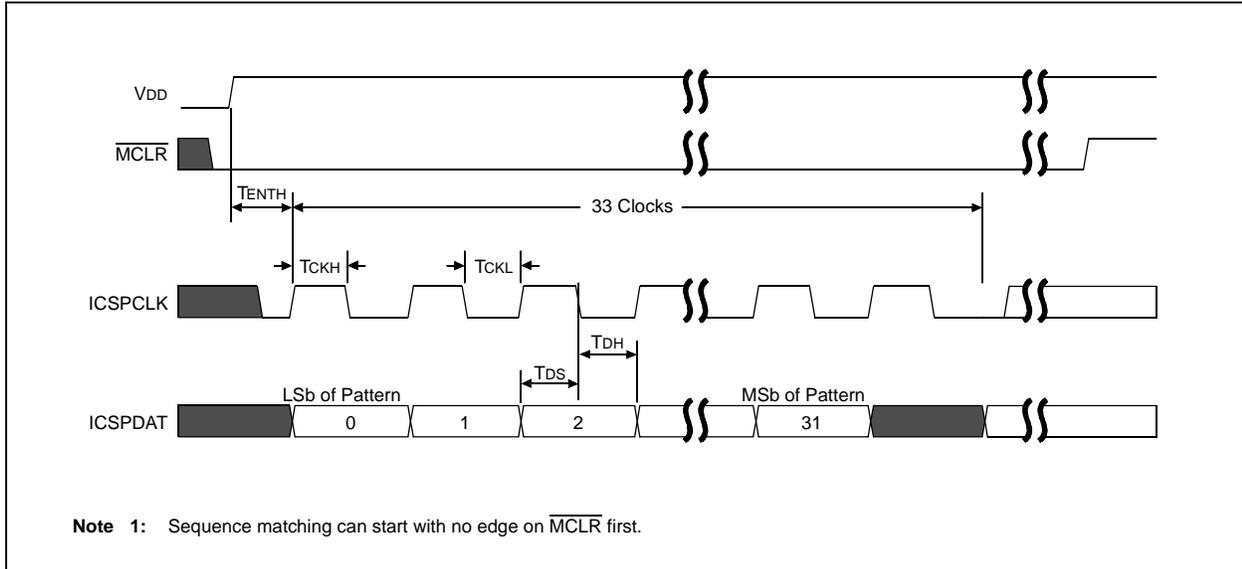


FIGURE 8-10: LVP ENTRY (POWERED)



APPENDIX A: REVISION HISTORY

Revision A (11/2008)

Original release of this document.

PIC16F193X/LF193X

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

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