A Microchip Technology Company

FlashFlex MCU
SST89C58RC

Data Sheet

SST89C58RC is a member of the FlashFlex family of 8-bit microcontrollers designed and manufactured with patented and proprietary SuperFlash CMOS semiconductor process technology. The split-gate cell design and thick-oxide tunneling injector offer significant cost and reliability benefits for customers. It uses the 8051 instruction set and is pin-for-pin compatible with standard 8051 microcontroller devices.

Features

- **8-bit 8051-Compatible Microcontroller (MCU) with Embedded SuperFlash Memory**
  - Fully Software Compatible
  - Development Toolset Compatible
  - Pin-for-Pin Package Compatible
- **SST89C58RC Operation**
  - 0 to 40 MHz at 2.7-5.5V
- **34 KByte Single Block SuperFlash EEPROM with two partitions**
  - 32 KByte primary partition + 2 KByte secondary partition
  - Flash Block is divided into four application pages (8 KByte) and one loader page (2 KByte)
  - Individual Page Security Lock
  - Address up to 64KB for External Data Memory
  - In-System Programming (ISP)
  - In-Application Programming (IAP)
  - Small-Sector Architecture: 128-Byte Sector Size
- **Total 1KByte On-chip RAM**
- **Supports External Address Range up to 64 KByte of Program and Data Memory**
- **Dual Enhanced SMBus**
  - Up to 400 Kbit per second
- **Full-Duplex, Enhanced UART**
  - Framing error detection
  - Automatic address recognition
- **Brown-out Reset (BOR)**
- **Nine Interrupt Sources at 4 Priority Levels**
- **Three 16-bit Timers/Counters**
- **Programmable Watchdog Timer (WDT)**
- **Second DPTR register**
- **Four 8-bit I/O Ports (32 I/O pins)**
- **I/O pins can tolerate V_{DD} +0.5V (Pulled up and driven to 5.5V)**
- **Standard 12 Clocks per cycle, the device has an option to double the speed to 6 clocks per cycle**
  - Speeds up to 40 MHz with 12 clock cycles per machine cycle
  - Speeds up to 20 MHz with 6 clock cycles per machine cycle - equivalent to 40 MHz
- **Enhanced Hook Emulation**
- **Low Power Modes**
  - Power-down Mode with External Interrupt Wake-up
  - Idle Mode
- **Temperature Ranges:**
  - Industrial (-40°C to +85°C)
  - Commercial (0°C to +70°C)
- **Packages Available**
  - 44-lead PLCC
  - 44-lead TQFP
  - 40-contact WQFN
- **All non-Pb (lead-free) devices are RoHS compliant**

Product Description

The SST89C58RC is a member of the FlashFlex family of 8-bit micro controllers designed and manufactured with SST patented and proprietary SuperFlash CMOS semiconductor process technology. The split-gate cell design and thick-oxide tunneling injector offer significant cost and reliability benefits for customers. It uses the 8051 instruction set and is pin-for-pin compatible with standard 8051 micro controller devices.

With two enhanced SMBus interfaces, the SST89C58RC supports speeds up to 400 Kbps. It comes with 34 KByte of on-chip flash EEPROM program memory which is divided into two independent program memory partitions. The primary partition occupies 32 KByte of internal program memory space and the secondary partition occupies 2 KByte of internal program memory space.

The flash memory can be programmed via a standard 87C5x OTP EPROM programmer fitted with a special adapter and firmware for SST devices. The SST89C58RC is designed to be programmed in-system on the printed circuit board for maximum flexibility. It is pre-programmed with an example of the bootstrap loader in memory, demonstrating initial user program code loading or subsequent user code updating via an ISP operation. The sample bootstrap loader is for the user's reference only, and SST does not guarantee its functionality. Chip-Erase operations will erase the pre-programmed sample code.

In addition to 34 KByte of SuperFlash EEPROM on-chip program memory and 1024 x8 bits of on-chip RAM, the device can address up to 64 KByte of external program memory and up to 64 KByte of external RAM.

The highly-reliable, patented SST SuperFlash technology and memory cell architecture offer a number of important advantages for designing and manufacturing flash EEPROMs. These advantages translate into significant cost and reliability benefits for customers.

Functional Blocks

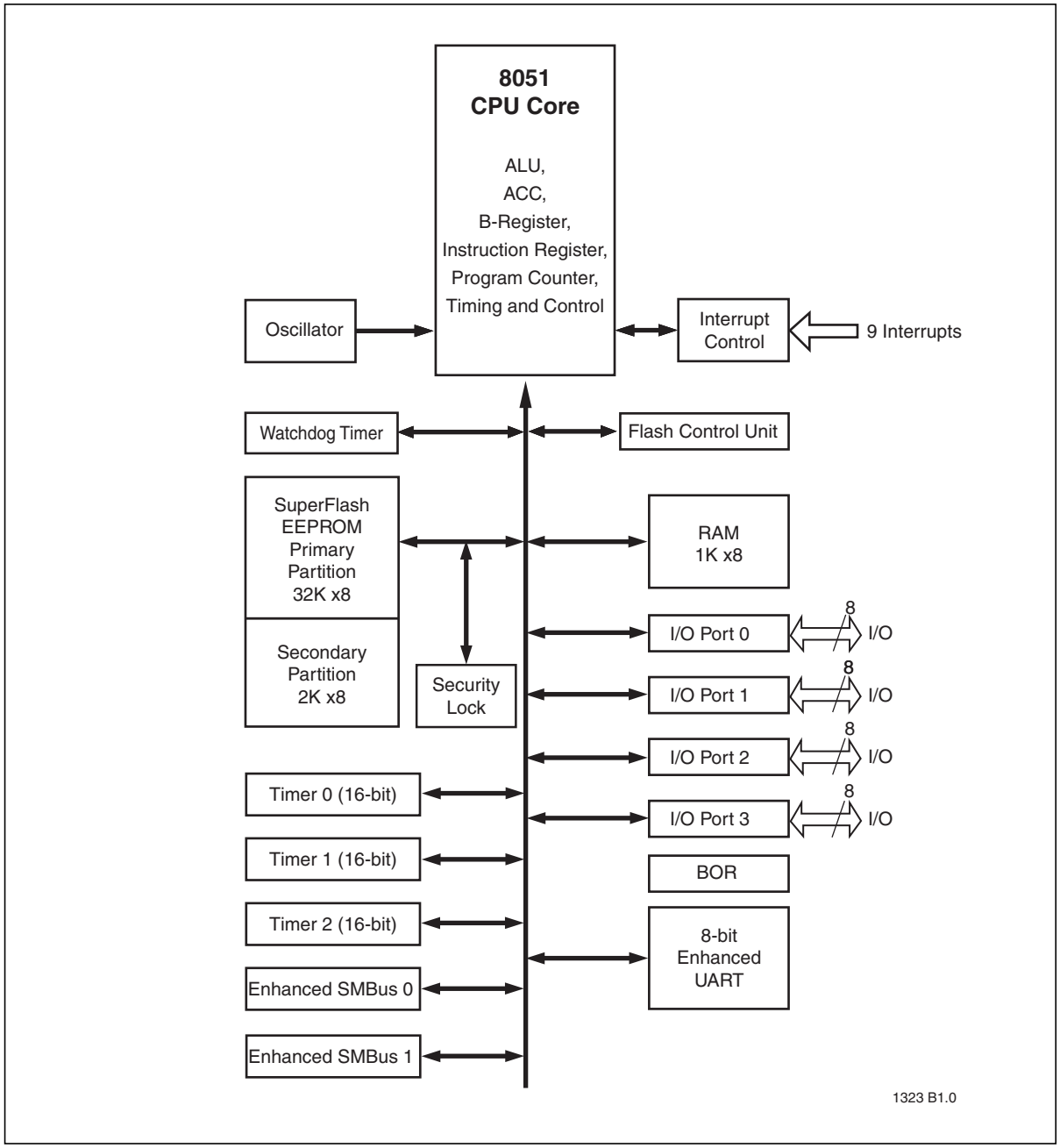

Figure 1: Functional Block Diagram

Pin Assignments

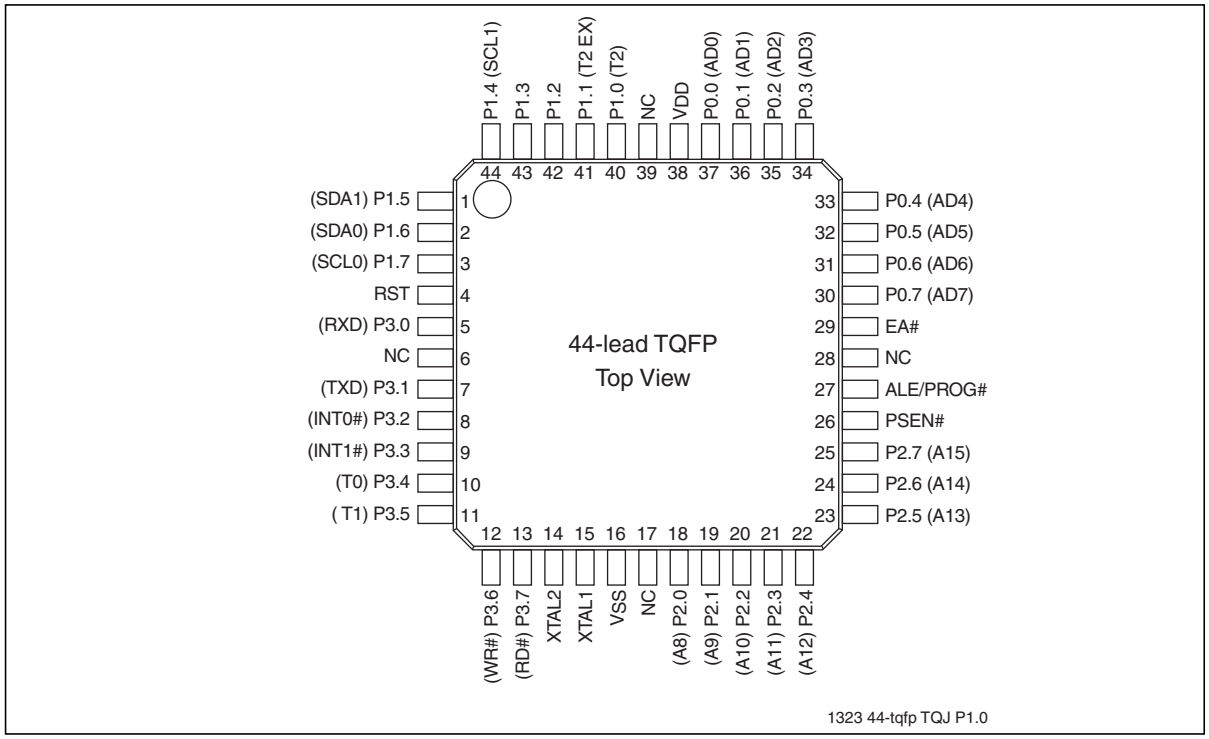

Figure 2: Pin Assignments for 44-Lead TQFP

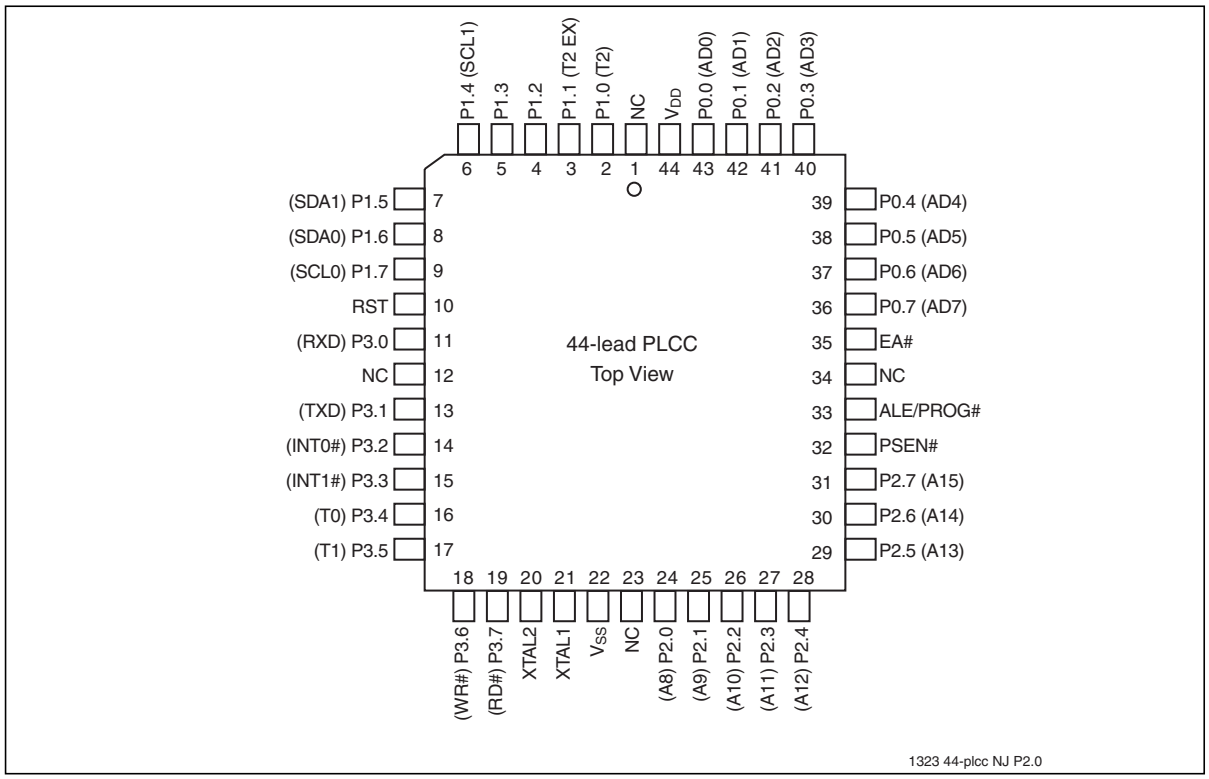

Figure 3: Pin Assignments for 44-Lead PLCC

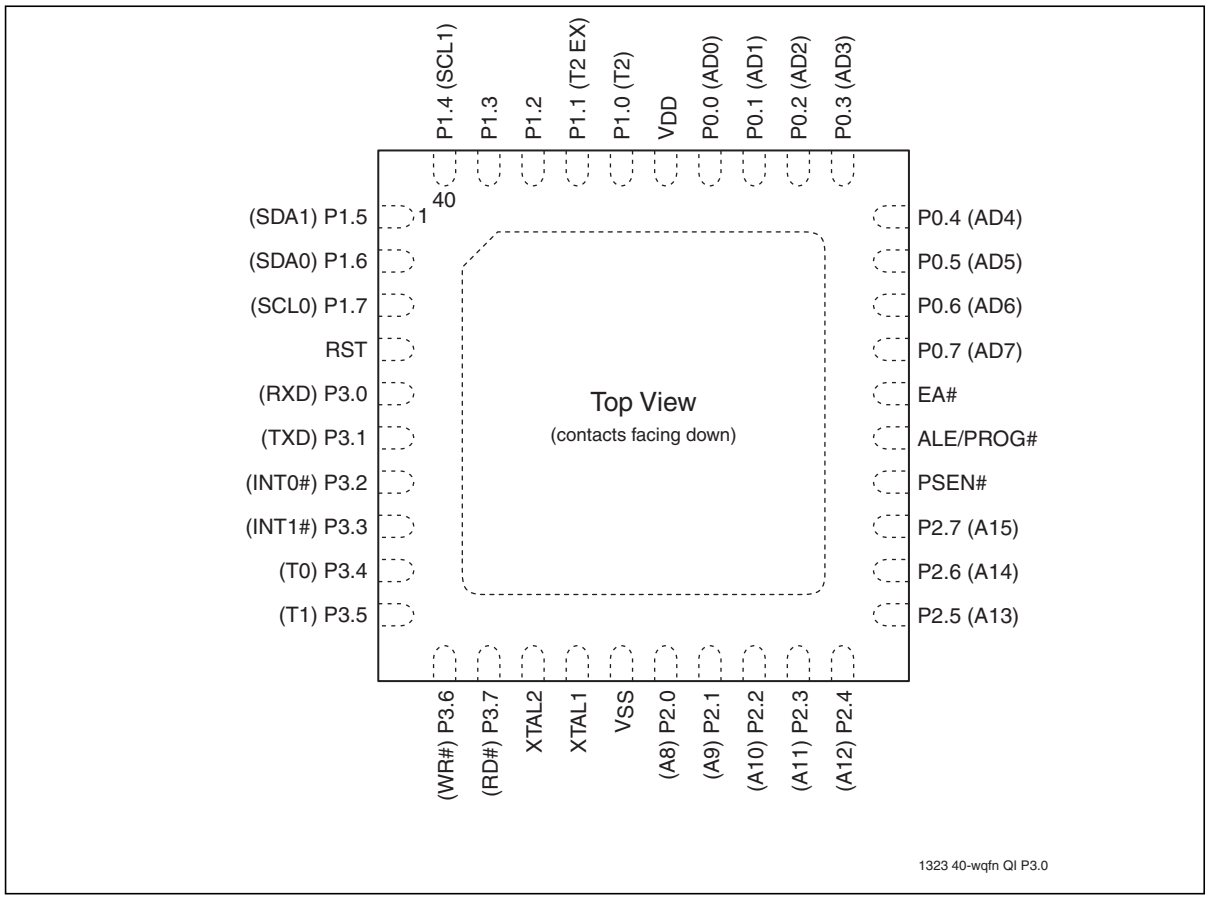

Figure 4: Pin Assignments for 40-Contact WQFN

Pin Descriptions

Table 1: Pin Descriptions (1 of 2)

Symbol	Type[1]	Name and Functions
P0[7:0]	I/O	**Port 0:** Port 0 is an 8-bit open drain bi-directional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have '1's written to them float, and in this state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external code and data memory. In this application, it uses strong internal pull-ups when transitioning to '1's. External pull-ups are required as a general purpose I/O port.
P1[7:0]	I/O with internal pull-up	**Port 1:** Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins are pulled high by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups.
P1[0]	I/O	**T2:** External count input to Timer/Counter 2 or Clock-out from Timer/Counter 2
P1[1]	I	**T2EX:** Timer/Counter 2 capture/reload trigger and direction control
P1[2]	I/O	GPIO
P1[3]	I/O	GPIO
P1[4]	I/O	**SCL1:** SMBus1 serial clock input / output
P1[5]	I/O	**SDA1:** SMBus1 serial data input / output
P1[6]	I/O	**SDA0:** SMBus0 serial data input / output
P1[7]	I/O	**SCL0:** SMBus1 serial clock input / output
P2[7:0]	I/O with internal pull-up	**Port 2:** Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. Port 2 pins are pulled high by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 sends the high-order address byte during accesses to external Data Memory that use 16-bit address (MOVX@DPTR). In this application, it uses strong internal pull-ups when transitioning to V_{OH}.
P3[7:0]	I/O with internal pull-up	**Port 3:** Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins are pulled high by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups.
P3[0]	I	**RXD:** Universal Asynchronous Receiver/Transmitter (UART) - Receive input
P3[1]	O	**TXD:** UART - Transmit output
P3[2]	I	**INT0#:** External Interrupt 0 Input
P3[3]	I	**INT1#:** External Interrupt 1 Input
P3[4]	I	**T0:** External count input to Timer/Counter 0
P3[5]	I	**T1:** External count input to Timer/Counter 1
P3[6]	O	**WR#:** External Data Memory Write strobe
P3[7]	O	**RD#:** External Data Memory Read strobe
PSEN#	I/O	**Program Store Enable:** PSEN# is the Read strobe to external program. When the device is executing from internal program memory, PSEN# is inactive (V_{OH}).
RST	I	**Reset:** While the oscillator is running, a "high" logic state on this pin for two machine cycles will reset the device.

Table 1: Pin Descriptions (Continued) (2 of 2)

Symbol	Type[1]	Name and Functions
EA#	I	**External Access Enable:** EA# must be connected to V_{SS} in order to enable the device to fetch code from the external program memory. EA# must be strapped to V_{DD} for internal program execution. However, Disable-Extern-Boot (See Section , "Security Lock") will disable EA#, and program execution is only possible from internal program memory.
ALE/ PROG#	I/O	**Address Latch Enable:** ALE is the output signal for latching the low byte of the address during an access to external memory. This pin is also the programming pulse input (PROG#) for flash programming. Normally the ALE[2] is emitted at a constant rate of 1/6 the crystal frequency[3]. One ALE pulse is skipped during each access to external data memory. However, if AO is set to '1', ALE is disabled.
NC	I/O	**No Connect**
XTAL1	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	O	**Crystal 2:** Output from the inverting oscillator amplifier.
V_{DD}	I	**Power Supply**
V_{SS}	I	**Ground**

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1. I = Input; O = Output
2. ALE loading issue: When ALE pin experiences higher loading (>30pf) during the reset, the MCU may accidentally enter into modes other than normal working mode. The solution is to add a pull-up resistor of 3-50 KΩ to V_{DD}, e.g. for ALE pin.
3. For 6 clock mode, ALE is emitted at 1/3 of crystal frequency.

I/O Descriptions

The device supports 2.7–5.5V supply, and the I/O pins can tolerate V_{DD} +0.5V. However, applying any voltage beyond power supply in quai-bidirectional mode is not recommended because doing so causes current to flow from the pin to VDD which consumes extra power.

Memory Organization

The SST89C58RC has separate address spaces for program and data memory.

Program Flash Memory

There are two internal flash memory partitions in the device. The primary flash memory partition (Partition 0) has 32 KByte. The secondary flash memory partition (Partition 1) has 2 KByte.

The 32 KByte primary flash partition is organized as 256 sectors, each sector consists of 128 Bytes. The primary partition is divided into four logical pages as shown in Figure 5.

The 2K x8 secondary flash partition is organized as 16 sectors, each sector consists also of 128 Bytes.

For both partitions, the 7 least significant program address bits select the byte within the sector. The remainder of the program address bits select the sector within the partition.

ENBOOT bit in AUXR1 (A2H) determines whether the second partition (Loader Page) is enabled or disabled. If ENBOOT is clear (default), the secondary partition (partition 1) is disabled. ENBOOT is automatically set when either of the following occur: the “Boot-From-Zero” bit is non-zero during reset or when P1.0 and P1.1 are pulled low while EA# is simultaneously held high on the falling edge of the reset.

If user-code boots from the default boot vector (0xF800) or from the User Boot Vector. The ENBOOT is set by hardware automatically to enable secondary partition (partition 1).

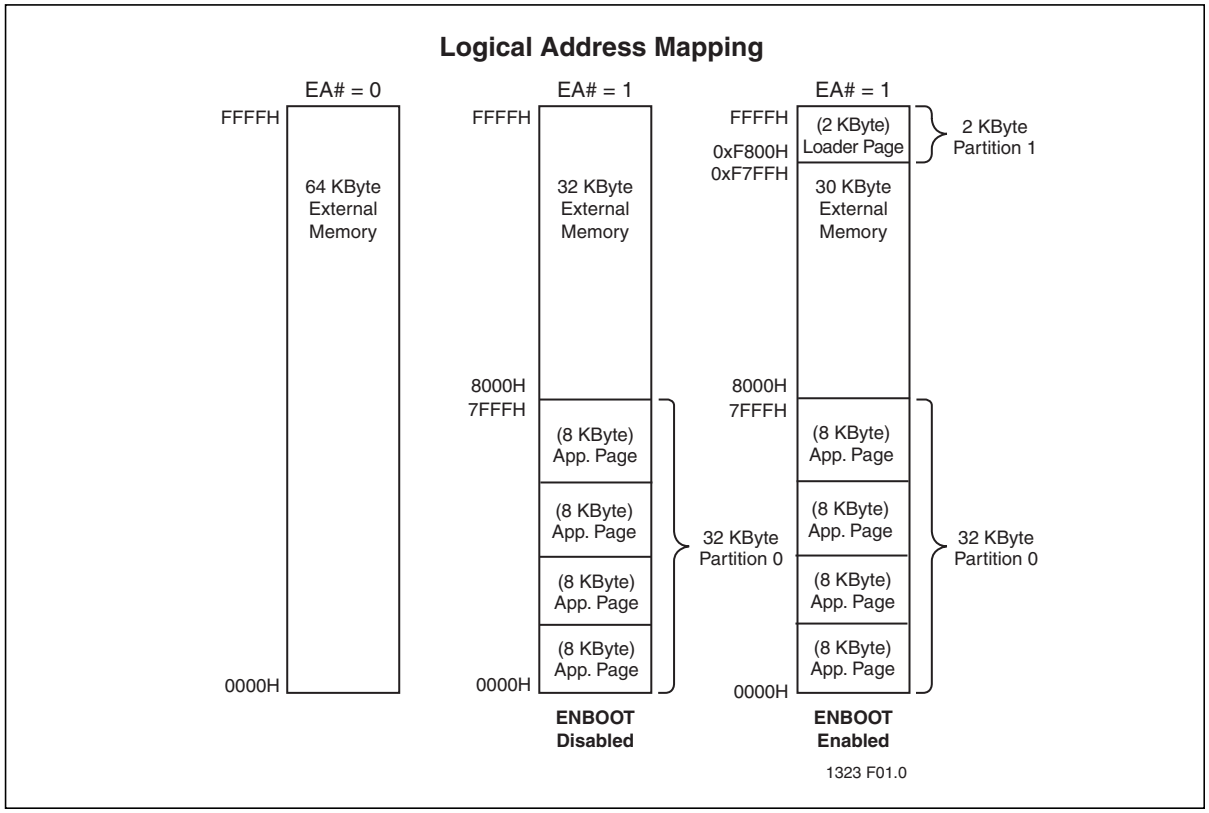

Figure 5: Program Memory Organization

Data RAM Memory

The data RAM has 1KByte of internal memory. The first 256 Bytes are available by default. The second 256 Bytes are enabled by clearing the EXTRAM bit in the AUXR register. The RAM can be addressed up to 64 KByte for external data memory.

Expanded Data RAM Addressing

The SST89C58RC has the capability of 1 KByte of RAM. See Figure 6.

The device has four sections of internal data memory:

1. The lower 128 Bytes of RAM (00H to 7FH) are directly and indirectly addressable.
2. The higher 128 Bytes of RAM (80H to FFH) are indirectly addressable.
3. The special function registers (80H to FFH) are directly addressable only.
4. The expanded RAM of 768 Bytes (00H to 2FFH) is indirectly addressable by the move external instruction (MOVX) and clearing the EXTRAM bit. (See “Auxiliary Register (AUXR)” in Section , “Special Function Registers”)

Since the upper 128 bytes occupy the same addresses as the SFRs, the RAM must be accessed indirectly. The RAM and SFRs space are physically separate even though they have the same addresses.

When instructions access addresses in the upper 128 bytes (above 7FH), the MCU determines whether to access the SFRs or RAM by the type of instruction given. If it is indirect, then RAM is accessed. If it is direct, then an SFR is accessed. See the examples below.

Indirect Access:

MOV@R0, #data; R0 contains 90H

Register R0 points to 90H which is located in the upper address range. Data in “#data” is written to RAM location 90H rather than port 1.

Direct Access:

MOV90H, #data; write data to P1

Data in “#data” is written to port 1. Instructions that write directly to the address write to the SFRs.

To access the expanded RAM, the EXTRAM bit must be cleared and MOVX instructions must be used. The extra 768 Bytes of memory is physically located on the chip and logically occupies the first 768 bytes of external memory (addresses 000H to 2FFH).

When EXTRAM = 0, the expanded RAM is indirectly addressed using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. Accessing the expanded RAM does not affect ports P0, P3.6 (WR#), P3.7 (RD#), or P2. With EXTRAM = 0, the expanded RAM can be accessed as in the following example.

Expanded RAM Access (Indirect Addressing only):

MOVX@DPTR, A; DPTR contains 0A0H

DPTR points to 0A0H and data in “A” is written to address 0A0H of the expanded RAM rather than external memory. Access to external memory higher than 2FFH using the MOVX instruction will access external memory (0300H to FFFFH) and will perform in the same way as the standard 8051, with P0 and P2 as data/address bus, and P3.6 and P3.7 as write and read timing signals.

When EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 8051. Using MOVX @Ri provides an 8-bit address with multiplexed data on Port 0. Other output port pins can be used to output higher order address bits. This provides external paging capabilities. Using MOVX @DPTR generates a 16-bit address. This allows external addressing up the 64K. Port 2 provides the high-order eight address bits (DPH), and Port 0 multiplexes the low order eight address bits (DPL) with data. Both MOVX @Ri and MOVX @DPTR generates the necessary read and write signals (P3.6 - WR# and P3.7 - RD#) for external memory use. Table 2 shows external data memory RD#, WR# operation with EXTRAM bit.

The stack pointer (SP) can be located anywhere within the 256 bytes of internal RAM (lower 128 bytes and upper 128 bytes). The stack pointer may not be located in any part of the expanded RAM.

Table 2: External Data Memory RD#, WR# with EXTRAM bit

	MOVX @DPTR, A or MOVX A, @DPTR		**MOVX @Ri, A or MOVX A, @Ri**
AUXR	**ADDR < 0300H**	**ADDR >= 0300H**	**ADDR = Any**
EXTRAM = 0	RD# / WR# not asserted	RD# / WR# asserted	RD# / WR# not asserted[1]
EXTRAM = 1	RD# / WR# asserted	RD# / WR# asserted	RD# / WR# asserted

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1. Access limited to ERAM address within 0 to 0FFH. 100H to 02FFH is not accessible.

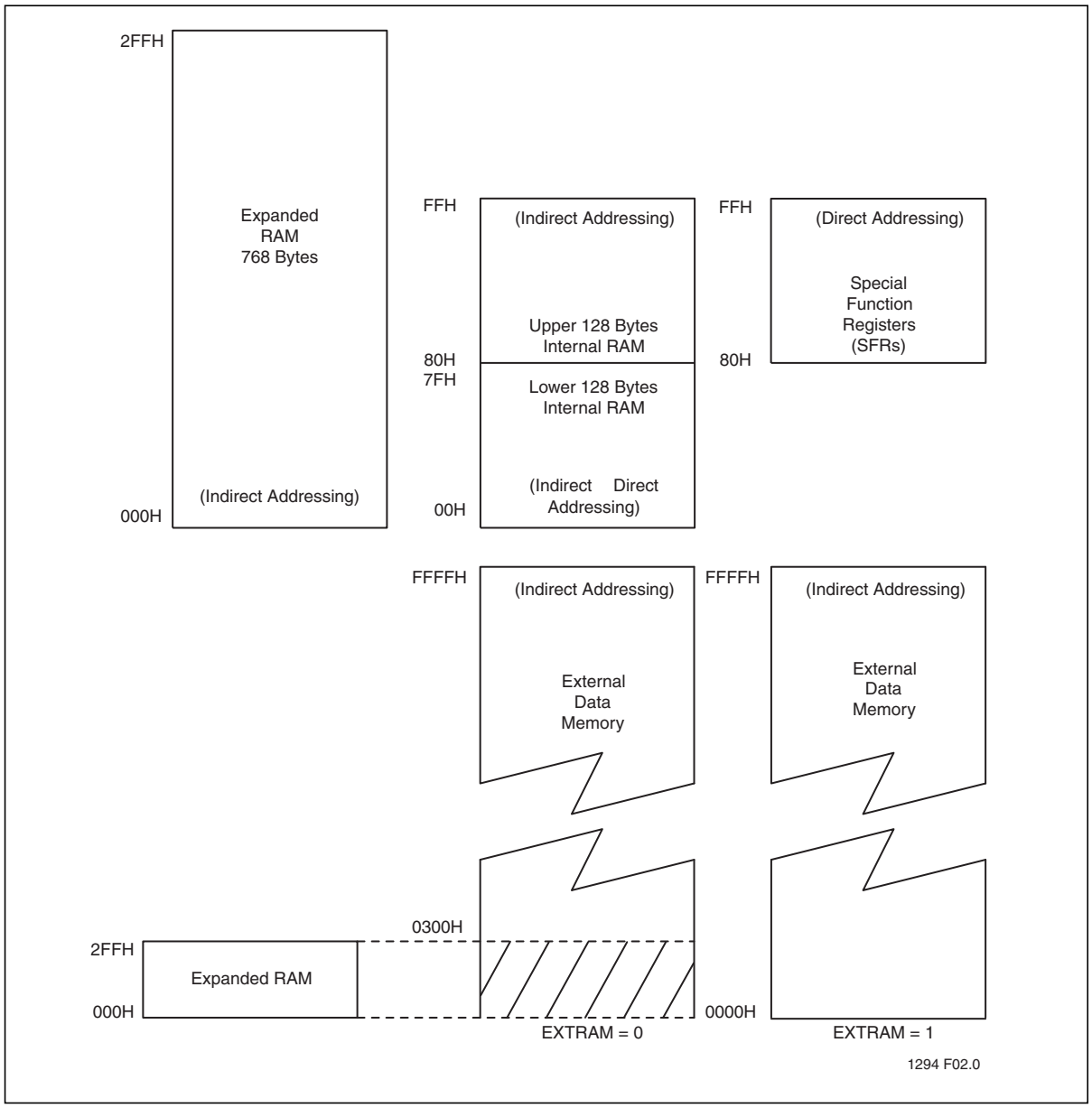

Figure 6: Internal and External Data Memory Structure

Dual Data Pointers

The SST89C58RC has two 16-bit data pointers. The DPTR Select (DPS) bit in AUXR1 determines which of the two data pointers is accessed. When DPS=0, DPTR0 is selected; when DPS=1, DPTR1 is selected. Quickly switching between the two data pointers can be accomplished by a single INC instruction on AUXR1. (See Figure 7)

Special Function Registers

Most of the unique features of the FlashFlex micro controller family are controlled by bits in special function registers (SFRs) located in the SFR memory map shown in Table 3. Individual descriptions of each SFR are provided and reset values indicated in Tables 4 to 8.

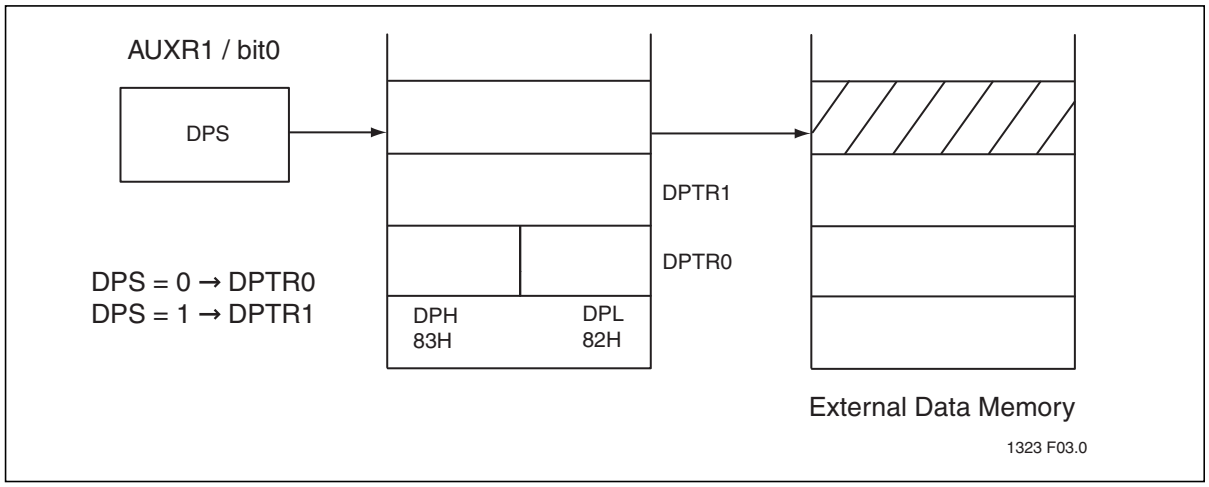

Figure 7: Dual Data Pointer Organization

Table 3: FlashFlex SFR Memory Map

	8 BYTES								
F8H									FFH
F0H	B								F7H
E8H	IEN1								EFH
E0H	ACC								E7H
D8H		SM0CON0	SM0STA	SM0DAT	SM0ADR	SM0SCLH	SM0SCLL	SM0CON1	DFH
D0H	PSW	SM1CON0	SM1STA	SM1DAT	SM1ADR	SM1SCLH	SM1SCLL	SM1CON1	D7H
C8H	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2			CFH
C0H	WDTC				SFIS1				C7H
B8H	IP0	S0ADEN						COSR	BFH
B0H	P3	SFCF	SFCM	SFAL	SFAH	SFDT	SFST	IP0H	B7H
A8H	IEN0	SADDR							AFH
A0H	P2	PMC	AUXR1						A7H
98H	S0CON	S0BUF							9FH
90H	P1	IP1	IP1H					SFISO	97H
88H	TCON	TMOD	TL0	TL1	TH0	TH1	AUXR		8FH
80H	P0	SP	DPL	DPH		WDTD		PCON	87H

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Table 4: CPU related SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
ACC[1]	Accumulator	E0H	ACC[7:0]								00H
B[1]	B Register	F0H	B[7:0]								00H
PSW[1]	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00H
SP	Stack Pointer	81H	SP[7:0]								07H
DPL	Data Pointer Low	82H	DPL[7:0]								00H
DPH	Data Pointer High	83H	DPH[7:0]								00H
IEN0[1]	Interrupt Enable	A8H	EA		ET2	ES	ET1	EX1	ET0	EX0	00H
IEN1[1]	Interrupt Enable A	E8H	-	EWD	-	-	-	-	EM1	EM0	x0xxxx00b
IP0	Interrupt Priority Reg	B8H	-	-	PT2	PS0	PT1	PX1	PT0	PX0	xx000000b
IP0H	Interrupt Priority Reg High	B7H	-	-	PT2H	PS0H	PT1H	PX1H	PT0H	PX0H	xx000000b
IP1	Interrupt Priority Reg A	91H	-	PWD	-	-	-	-	PM1	PM0	x0xxxx00b
IP1H	Interrupt Priority Reg A High	92H	-	PWDH	-	-	-	-	PM1H	PM0H	x0xxxx00b
PCON	Power Control	87H	SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL	00x10000b
AUXR	Auxiliary Reg	8EH	-	-	-	-	-	-	EXTRAM	AO	xxxxxxx10b
AUXR1	Auxiliary Reg 1	A2H	-	-	ENBOOT	-	GF2	0	-	DPS	xx1x00x0b
PMC	Power Management Control	A1H	-	-	WDU	TCT	TCT2	SMB0	SMB1	UART	xx000000b

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1. Bit Addressable SFRs

Table 5: Flash Memory Programming SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
SFCF	SuperFlash Configura-tion	B1H	CMD_Status	IAPEN	-	HWIAP	-	SFST_SEL			01x0x000b
SFCM	SuperFlash Command	B2H	-	SFCM[6:0]							x0000000b
SFAL	SuperFlash Address Low	B3H	SuperFlash Low Order Byte Address Register A_7 to A_0 (SFAL)								00H
SFAH	SuperFlash Address High	B4H	SuperFlash High Order Byte Address Register A_{15} to A_8 (SFAH)								00H
SFDT	SuperFlash Data	B5H	SuperFlash Data Register								00H
SFST	SuperFlash Status	B6H SFST_SEL =0H	Manufacturer's ID								BFH
		SFST_SEL =1H	Device ID0 (F7H indicates Device ID1 is real ID)								
		SFST_SEL =2H	Device ID1								
		SFST_SEL =3H	Boot Vector								
		SFST_SEL =4H	-	-	-	PAGE4	PAGE3	PAGE2	PAGE1	PAGE0	xxx11111b
		SFST_SEL =5H	X	Boot From Zero	Boot-From-User-Vector	Enable Clock-Double	Disable-Extern-Host-Cmd	Dis-able-Extern-MOVC	Disable-Extern-Boot	Dis-able-Extern-IAP	x1111111b

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Table 6: Watchdog Timer SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
WDTC	Watchdog Timer Control	C0H	-	WDTON	WDFE	-	WDRE	WDTS	WDT	SWDT	x00x0000b
WDTD	Watchdog Timer Data/ Reload	85H	Watchdog Timer Data/Reload								00H

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Table 7: Timer/Counter SFR

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
TMOD	Timer/Counter Mode Control	89H	Timer 1				Timer 0				00H
			GATE	C/T#	M1	M0	GATE	C/T#	M1	M0	
TCON[1]	Timer/Counter Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
TH0	Timer 0 MSB	8CH	TH0[7:0]								00H
TL0	Timer 0 LSB	8AH	TL0[7:0]								00H
TH1	Timer 1 MSB	8DH	TH1[7:0]								00H
TL1	Timer 1 LSB	8BH	TL1[7:0]								00H
T2CON[1]	Timer/Counter 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#	00H
T2MOD#	Timer 2 Mode Control	C9H	-	-	-	-	-	-	T2OE	DCEN	xxxxxx00b
TH2	Timer 2 MSB	CDH	TH2[7:0]								00H
TL2	Timer 2 LSB	CCH	TL2[7:0]								00H
RCAP2H	Timer 2 Capture MSB	CBH	RCAP2H[7:0]								00H
RCAP2L	Timer 2 Capture LSB	CAH	RCAP2L[7:0]								00H

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1. Bit Addressable SFRs

Table 8: Interface SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
S0BUF	Serial Data Buffer	99H	SBUF[7:0]								Indeterminate
S0CON	Serial Port Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00H
S0ADDR	Slave Address	A9H	S0ADDR[7:0]								00H
S0ADEN	Slave Address Mask	B9H	S0ADEN[7:0]								00H
SM0CON0	SMBus0 Contol0	D9H	SMBEN_0	STA_0	STO_0	SI_0	AA_0	FTE_0	TOE_0	CRSEL_0	00H
SM0STA	SMBus0 Status	DAH	SM0STA[7:3]					0	0	0	F8H
SM0DAT	SMBus0 Data	DBH	SM0DAT[7:0]								00H
SM0ADR	SMBus0 Address	DCH	SM0 Slave Address[6:0]							GC_0	00H
SM0SCLH	SMBus0 SCL High Duty	DDH	SM0SCLH[7:0]								00H
SM0SCLL	SMBus0 SCL LowDuty	DEH	SM0SCLL[7:0]								00H
SM0CON1	SMBus0 Contol1	DFH	1	1	1	1	PWRUP_SI0	PWRUP_EN0	STADY_0	EXHOLD_0	F0H
SM1CON0	SMBus1 Contol0	D1H	SMBEN_1	STA_1	STO_1	SI_1	AA_1	FTE_1	TOE_1	CRSEL_1	00H
SM1STA	SMBus1 Status	D2H	SM1STA[7:3]					0	0	0	F8H
SM1DAT	SMBus1 Data	D3H	SM1DAT[7:0]								00H
SM1ADR	SMBus1 Address	D4H	SM1 Slave Address SM1ADR[7:1]							GC_1	00H
SM1SCLH	SMBus1 SCL High Duty	D5H	SM1SCLH[7:0]								00H
SM1SCLL	SMBus1 SCL LowDuty	D6H	SM1SCLL[7:0]								00H
SM1CON1	SMBus1 Contol1	D7H	1	1	1	1	PWRUP_SI1	PWRUP_EN1	STADY_0	EXHOLD_0	FOH
P0[1]	Port 0	80H	P0[7:0]								FFH
P1[1]	Port 1	90H	-	-	-	-	-	-	T2EX	T2	FFH
P2[1]	Port 2	A0H	P0[7:0]								FFH
P3[1]	Port 3	B0H	RD#	WR#	T1	T0	INT1#	INT0#	TXD	RXD	FFH

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1. Bit Addressable SFRs

Table 9: Feed Sequence SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB LSB	Reset Value
SFIS0	Sequence Reg 0	97H	(Write only)	00H
SFIS1	Sequence Reg 1	C4H	(Write only)	00H

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Table 10: Clock Option SFR

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB						LSB	Reset Value
COSR	Clock Option Register	BFH	-	-	-	-	COEN	CO_REL	CO_IN	0x00000b

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SuperFlash Configuration Register (SFCF)

Location	7	6	5	4	3	2	1	0	Reset Value
B1H	CMD_ Status	IAPEN	-	HWIAP	-	SFST_SEL			01x0x000b

Symbol	Function
CMD_Status	IAP Command Completion Status 0: IAP command is ignored 1: IAP command is completed fully
IAPEN	IAP Enable Bit 0: Disable all IAP commands (Commands will be ignored) 1: Enable all IAP commands
HWIAP	Boot Status Flag 0: System boots up without special pin configuration setup 1:System boots up with both P1[0] and P1[1] pins in logic low state curing reset
SFST_SEL	Provide index to read back information when read to SFST register is executed (See , “SuperFlash Status Register (SFST) (Read Only Register)” on page 20 for detailed settings)

SuperFlash Command Register (SFCM)

Location	7	6	5	4	3	2	1	0	Reset Value
B2H	-	FCM6	FCM5	FCM4	FCM3	FCM2	FCM1	FCM0	x0000000b

Symbol	Function
-	Reserved
FCM[6:0]	Flash operation command
	000_0001b Chip-Erase
	000_1011b Sector-Erase
	000_1101b Partition0-Erase
	000_1100b Byte-Verify
	000_1110b Byte-Program
	000_0011b Secure-Page
	Page-Level Security Commands
	SFAH=90H; Secure-Page0
	SFAH=91H; Secure-Page1
	SFAH=92H; Secure-Page2
	SFAH=93H; Secure-Page3
	SFAH=94H; Secure-Page4
	000-0101b Secure-Chip
	Chip-Level Security Commands
	SFAH=B0H; Disable-Extern-IAP
	SFAH=B1H; Disable-Extern-Boot
	SFAH=B2H; Disable-Extern-MOVC
	SFAH=B3H; Disable-Extern-Host-Cmd
	000-1000b Boot Options
	Boot Option Setting Commands
	SFAH=E0H; Enable-Clock-Double
	SFAH=E1H; Prog-Boot-From-User-Vector
	SFAH=E2H; Prog-Boot-Jumper
	000-1001b Set-User-Boot-Vector
	All other combinations are not implemented, and reserved for future use.

SuperFlash Address Registers (SFAL)

Location	7	6	5	4	3	2	1	0	Reset Value
B3H	SuperFlash Low Order Byte Address Register								00H

Symbol	Function
SFAL	Mailbox register for interfacing with flash memory block. (Low order address register)

SuperFlash Address Registers (SFAH)

Location	7	6	5	4	3	2	1	0	Reset Value
B4H	SuperFlash High Order Byte Address Register								00H

Symbol	Function
SFAH	Mailbox register for interfacing with flash memory block. (High order address register)

SuperFlash Data Register (SFDT)

Location	7	6	5	4	3	2	1	0	Reset Value
B5H	SuperFlash Data Register								00H

Symbol	Function
SFDT	Mailbox register for interfacing with flash memory block. (Data register)

SuperFlash Status Register (SFST) (Read Only Register)

Location	7	6	5	4	3	2	1	0	Reset Value
B6H	SuperFlash Status Register								1011 1111b

Symbol	Function
SFST	This is a read-only register. The read-back value is indexed by SFST_SEL in the SuperFlash Configuration Register (SFCF) SFST_SEL= 0H: Manufacturer's ID 1H: Device ID0 = F7H 2H: Device ID1 = Device ID (Refer to Table 11 on page 32) 3H: Boot Vector 4H: Page-Security bit setting 5H: Chip-Level Security bit setting and Boot Options

Interrupt Enable (IEN0)

Location	7	6	5	4	3	2	1	0	Reset Value
A8H	EA	-	ET2	ES0	ET1	EX1	ET0	EX0	0x000000b

Symbol	Function
EA	Global Interrupt Enable 0 = Disable 1 = Enable
ET2	Timer 2 Interrupt Enable
ES0	Serial Interrupt Enable
ET1	Timer 1 Interrupt Enable
EX1	External 1 Interrupt Enable
ET0	Timer 0 Interrupt Enable
EX0	External 0 Interrupt Enable

Interrupt Enable A (IEN1)

Location	7	6	5	4	3	2	1	0	Reset Value
E8H	-	EWD	-	-	-	-	EM1	EM0	x0xxxx00b

Symbol	Function
EWD	Watchdog Interrupt Enable 0 = Disable 1 = Enable
EM1	SMBus 1 Interrupt Enable
EM0	SMBus 0 Interrupt Enable

Interrupt Priority (IP0)

Location	7	6	5	4	3	2	1	0	Reset Value
B8H	-	-	PT2	PS0	PT1	PX1	PT0	PX0	xx000000b

Symbol	Function
PT2	Timer 2 Interrupt priority bit
PS0	Serial Port Interrupt priority bit
PT1	Timer 1 Interrupt priority bit
PX1	External Interrupt 1 priority bit
PT0	Timer 0 Interrupt priority bit
PX0	External Interrupt 0 priority bit

Interrupt Priority High (IP0H)

Location	7	6	5	4	3	2	1	0	Reset Value
B7H	-	-	PT2H	PS0H	PT1H	PX1H	PT0H	PX0H	xx000000b

Symbol	Function
PT2H	Timer 2 Interrupt priority bit high
PS0H	Serial Port Interrupt priority bit high
PT1H	Timer 1 Interrupt priority bit high
PX1H	External Interrupt 1 priority bit high
PT0H	Timer 0 Interrupt priority bit high
PX0H	External Interrupt 0 priority bit high

Interrupt Priority (IP1)

Location	7	6	5	4	3	2	1	0	Reset Value
91H	-	PWD	-	-	-	-	PM1	PM0	x0xxxx00b

Symbol	Function
PWD	Watchdog interrupt priority bit
PM1	SMBus 1 Interrupt priority bit
PM0	SMBus 0 Interrupt priority bit

Interrupt Priority High (IP1H)

Location	7	6	5	4	3	2	1	0	Reset Value
92H	-	PWDH	-	-	-	-	PM1H	PM0H	x0xxx00b

Symbol	Function
PWDH	Watchdog interrupt priority bit high
PM1H	SMBus 1 Interrupt priority bit high
PM0H	SMBus 0 Interrupt priority bit high

Auxiliary Register (AUXR)

Location	7	6	5	4	3	2	1	0	Reset Value
8EH	-	-	-	-	-	-	EXTRAM	AO	xxxxxx10b

Symbol	Function
EXTRAM	Internal/External RAM access 0: Internal Expanded RAM access within range of 00H to FFH using MOVX @Ri / @DPTR. Beyond 100H, the MCU always accesses external data memory For details, refer to Section , “Expanded Data RAM Addressing” 1: External data memory access
AO	Disable/Enable ALE 0: ALE is emitted at a constant rate of 1/3 the oscillator frequency in 6 clock mode, 1/6 f_{OSC} in 12 clock mode 1: ALE is active only during a MOVX or MOVC instruction

Auxiliary Register 1 (AUXR1)

Location	7	6	5	4	3	2	1	0	Reset Value
A2H	-	-	ENBOOT	-	GF2	0	-	DPS	xx1x00x0b

Symbol	Function
ENBOOT	Enable Partition 1
GF2	General purpose user-defined flag
DPS	DPTR registers select bit 0: DPTR0 is selected 1: DPTR1 is selected

Sequence Register 0 (SFIS0)

Location	7	6	5	4	3	2	1	0	Reset Value
97H	(Write Only)								N/A

Symbol	Function
SFIS0	Register used with SFIS1 to provide a feed sequence to validate writing to WDTC and SFCM. Without a proper feed sequence, writing to SFCM will be ignored and writing to WDTC in Watchdog mode will cause an immediate Watchdog reset.

Sequence Register 1 (SFIS1)

Location	7	6	5	4	3	2	1	0	Reset Value
C4H	(Write Only)								N/A

Symbol	Function
SFIS1	Register used with SFIS0 to provide a feed sequence to validate writing to WDTC and SFCM.

Watchdog Timer Control Register (WDTC)

Location	7	6	5	4	3	2	1	0	Reset Value
C0H	-	WDTON	WDFE	-	WDRE		WDT	SWDT	x00x0000b

Symbol	Function
WDTON	Watchdog timer start control bit (Used in Watchdog mode) 0: Watchdog timer can be started or stopped freely during Watchdog mode. 1: Start Watchdog timer; bit cannot be cleared by software.
WDFE	Watchdog feed sequence error flag 0: Watchdog feed sequence error has not occurred. 1: Due to an incorrect feed sequence before writing to WDTC in Watchdog mode, the hardware entered Watchdog reset and set this flag to '1'. This is for software to detect whether the Watchdog reset was caused by timer expiration or an incorrect feed sequence.
WDRE	Watchdog timer reset enable. 0: Disable Watchdog timer reset. 1: Enable Watchdog timer reset.
WDTS	Watchdog timer reset flag. 0: External hardware reset or power-on reset clears the flag. Flag can also be cleared by writing a 1. Flag survives if chip reset happened because of Watchdog timer overflow. 1: Hardware sets the flag on watchdog overflow.
WDT	Watchdog timer refresh. 0: Hardware resets the bit when refresh is done. 1: Software sets the bit to force a Watchdog timer refresh.
SWDT	Start Watchdog timer. 0: Stop WDT. 1: Start WDT.

Watchdog Timer Data/Reload Register (WDTD)

Location	7	6	5	4	3	2	1	0	Reset Value
85H	Watchdog Timer Data/Reload								00H

Clock Option Register (COSR)

Location	7	6	5	4	3	2	1	0	Reset Value
BFH	-	-	-	-	COEN	CO_SEL		CO_IN	xxxx0000H

Symbol	Function
COEN	Clock Divider Enable 0: Disable Clock Divider 1: Enable Clock Divider
CO_SEL	Clock Divider Selection 00b: 1/4 clock source 01b: 1/16 clock source 10b: 1/256 clock source 11b: 1/1024 clock source
CO_IN	Clock Source Selection 0b: Select clock from 1x clock 1b: Select clock from 2x clock The default value of this bit is set during Power-on reset by copying from Enable_Clock_Double_i non-volatile bit setting. CO_IN can be changed during normal operation to select the double clock option. If the clock source is a 1x clock, the clock divider exports 1/4, 1/16, 1/256, or 1/1024 of the input clock. If the clock source is a 2x clock, the clock divider exports 1/2, 1/8, 1/128, or 1/512 of the input clock.

Power Management Control Register (PMC)

Location	7	6	5	4	3	2	1	0	Reset Value
A1H	-	-	WDU	TCT	TCT2	SMB0	SMB1	UART	xx000000b

Symbol	Function
WDU	Watchdog Timer Clock Control 0:The clock for the Watchdog timer is running 1:The clock for the Watchdog timer is stopped
TCT	Timer 0/1 Clock Control 0:The Timer 0/1 logic is running 1:The Timer 0/1 logic is stopped
TCT2	Timer 2 Clock Control 0:The Timer 2 logic is running 1:The Timer 2 logic is stopped
SMB0	SMBus 0 Clock Control 0:The SMBus0 logic is running 1:The SMBus0 logic is stopped
SMB1	SMBus 1 Clock Control 0:The SMBus0 logic is running 1:The SMBus0 logic is stopped
UART	UART Clock Control 0:The UART logic is running 1:The UART logic is stopped

SMBus0 Control Register0 (SM0CON0)

Location	7	6	5	4	3	2	1	0	Reset Value
D9H	SMBEN_0	STA_0	STO_0	SI_0	AA_0	FTE_0	TOE_0	CRSEL_0	00H

Symbol	Function
SMBEN_0	SMBus Enable 0: Disable SMBus 1: Enable SMBus
STA_0	Start Flag 0: No START condition or repeated START condition will be generated 1: START or repeated START condition will be generated
STO_0	Stop Flag 0: No STOP condition is generated 1: STOP condition is generated
SI_0	Serial Interrupt Flag 0: No serial interrupt is requested, no stretching on the SCL 1: A serial interrupt is requested, the SCL line is stretched (if EA and ES1 are both set)
AA_0	Assert Acknowledge Flag -This bit defines the type of acknowledge returned during the acknowledge cycle on the SCL line. 0: A “not acknowledge” (high level on SDA) is returned during the acknowledge cycle 1: An “acknowledge” (low level on SDA) is returned during the acknowledge cycle
FTE_0	Bus Free (SCL High) Timeout Enable 0: Bus Free timeout disabled 1: Bus Free timeout enabled
TOE_0	SCL Low Timeout Enable 0: SCL Low timeout disabled 1: SCL Low timeout enabled
CRSEL_0	SCL Clock Source Selection 0: SMBus internal baud generator generates the SCL 1: TIMER1 overflow generates the SCL

SMBus0 Control Register1 (SM0CON1)

Location	7	6	5	4	3	2	1	0	Reset Value
DFH	1	1	1	1	PWRUP_SI0	PWRUP_EN0	STADY_0	EXTHOLD_0	F0H

Symbol	Function
PWRUP_SI0	Power-down Wakeup Flag - When the SUBus wakes up the MCU, the flag bit is set by hardware. The bit is in ready-only mode. Only writing '0' to this bit will clear the flag. If SMBus interrupt enable bit is set, then the SMBus interrupt is generated when the flag bit is '1'. 0: No wakeup flag 1: Wakeup flag occurs
PWRUP_EN0	Power-down Wakeup Enable 0: SMBus power-down wakeup function disabled 1: SMBus power-down wakeup function enabled
STADY_0	Start Condition Long Delay Enable 0: Start condition long delay disabled 1: Start condition long delay enabled
EXTHOLD_0	External Data Hold Time Setting 0: SDA hold time is 20 system clock periods 1: SDA hold time is 3 system clock periods

SMBus1 Control Register0 (SM1CON0)

Location	7	6	5	4	3	2	1	0	Reset Value
D1H	SMBEN_1	STA_1	STO_1	SI_1	AA_1	FTE_1	TOE_1	CRSEL_1	00H

Symbol	Function
SMBEN_1	SMBus Enable 0: Disable SMBus 1: Enable SMBus
STA_1	Start Flag 0: No START condition or repeated START condition will be generated 1: START or repeated START condition will be generated
SI_1	Serial Interrupt Flag 0: No serial interrupt is requested, no stretching on the SCL 1: A serial interrupt is requested, the SCL line is stretched (if EA and ES1 are both set)
AA_1	Assert Acknowledge Flag -This bit defines the type of acknowledge returned during the acknowledge cycle on the SCL line. 0: A "not acknowledge" (high level on SDA) is returned during the acknowledge cycle 1: An "acknowledge" (low level on SDA) is returned during the acknowledge cycle
FTE_1	Bus Free (SCL High) Timeout Enable 0: Bus Free timeout disabled 1: Bus Free timeout enabled
TOE_1	SCL Low Timeout Enable 0: SCL Low timeout disabled 1: SCL Low timeout enabled
CRSEL_1	SCL Clock Source Selection 0: SMBus internal baud generator generates the SCL 1: TIMER1 overflow generates the SCL

SMBus1 Control Register1 (SM1CON1)

Location	7	6	5	4	3	2	1	0	Reset Value
D7H	1	1	1	1	PWRUP_SI1	PWRUP_EN1	STADY_1	EXTHOLD_1	F0H

Symbol	Function
PWRUP_SI1	Power-down Wakeup Flag - When the SUBus wakes up the MCU, the flag bit is set by hardware. The bit is in ready-only mode. Only writing '0' to this bit will clear the flag. If SMBus interrupt enable bit is set, then the SMBus interrupt is generated when the flag bit is '1'. 0: No wakeup flag 1: Wakeup flag occurs
PWRUP_EN1	Power-down Wakeup Enable 0: SMBus power-down wakeup function disabled 1: SMBus power-down wakeup function enabled
STADY_1	Start Condition Long Delay Enable 0: Start condition long delay disabled 1: Start condition long delay enabled
EXTHOLD_1	External Data Hold Time Setting 0: SDA hold time is 20 system clock periods 1: SDA hold time is 3 system clock periods

SMBus0 Status Register (SM0STA)

Location	7	6	5	4	3	2	1	0	Reset Value
DAH	SM0STA[7:3]					0	0	0	F8H

Symbol	Function
SM0STA	This is a read-only SFR. The five most significant bits contain the status code. The three least significant bits are always '0'.

SMBus1 Status Register (SM1STA)

Location	7	6	5	4	3	2	1	0	Reset Value
D2H	SM0STA[7:3]					0	0	0	F8H

Symbol	Function
SM1STA	This is a read-only SFR. The five most significant bits contain the status code. The three least significant bits are always '0'.

SMBus0 Data Register (SM0DAT)

Location	7	6	5	4	3	2	1	0	Reset Value
DBH	SM0DAT[7:0]								00H

SMBus1 Data Register (SM1DAT)

Location	7	6	5	4	3	2	1	0	Reset Value
D3H	SM1DAT[7:0]								00H

SMBus01 Address Register 0 (SM0ADR)

Location	7	6	5	4	3	2	1	0	Reset Value
D4H	SM0 Slave Address [7:1]							GC_0	00H

SMBus1 Address Register 1 (SM1ADR)

Location	7	6	5	4	3	2	1	0	Reset Value
D4H	SM1 Slave Address [7:1]							GC_1	00H

SMBus0 High-Duty Setting Register (SM0SCLH)

Location	7	6	5	4	3	2	1	0	Reset Value
DDH	SM0SCLH[7:0]								00H

Symbol	Function
SM0SCLH[7:0]	Set the SCL high duration

SMBus0 Low-Duty Setting Register (SM0SCLL)

Location	7	6	5	4	3	2	1	0	Reset Value
DEH	SM0SCLL[7:0]								00H

Symbol	Function
SM0SCLH[7:0]	Set the SCL low duration

SMBus1 High-Duty Setting Register (SM1SCLH)

Location	7	6	5	4	3	2	1	0	Reset Value
D5H	SM1SCLH[7:0]								00H

Symbol	Function
SM0SCLH[7:0]	Set the SCL high duration

SMBus1 Low-Duty Setting Register (SM1SCLL)

Location	7	6	5	4	3	2	1	0	Reset Value
D6H	SM0SCLL[7:0]								00H

Symbol	Function
SM0SCLH[7:0]	Set the SCL low duration

Power Control Register (PCON)

Location	7	6	5	4	3	2	1	0	Reset Value
87H	SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL	00x10000b

Symbol	Function
SMOD1	Double Baud rate bit. If SMOD1 = 1, Timer 1 is used to generate the baud rate, and the serial port is used in modes 1, 2, and 3.
SMOD0	FE/SM0 Selection bit. 0: SCON[7] = SM0 1: SCON[7] = FE,
POF	Power-on reset status bit, this bit will not be affected by any other reset. POF should be cleared by software. 0: No Power-on reset. 1: Power-on reset occurred
GF1	General-purpose flag bit.
GF0	General-purpose flag bit.
PD	Power-down bit, this bit is cleared by hardware after exiting from power-down mode. 0: Power-down mode is not activated. 1: Activates Power-down mode.
IDL	Idle mode bit, this bit is cleared by hardware after exiting from idle mode. 0: Idle mode is not activated. 1: Activates idle mode.

Serial Port Control Register (S0CON)

Location	7	6	5	4	3	2	1	0	Reset Value
98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00000000b

Symbol	Function
FE	Set SMOD0 = 1 to access FE bit. 0: No framing error 1: Framing Error. Set by receiver when an invalid stop bit is detected. This bit needs to be cleared by software.
SM0	SMOD0 = 0 to access SM0 bit. Serial Port Mode Bit 0
SM1	Serial Port Mode Bit 1

SM0	SM1	Mode	Description	Baud Rate[1]
0	0	0	Shift Register	f_{OSC}/6 (6 clock mode) or f_{OSC}/12 (12 clock mode)
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	f_{OSC}/32 or f_{OSC}/16 (6 clock mode) or f_{OSC}/64 or f_{OSC}/32 (12 clock mode)
1	1	3	9-bit UART	Variable

1. f_{OSC} = oscillator frequency

SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a given or broadcast address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received. In Mode 0, SM2 should be 0.
REN	Enables serial reception. 0: to disable reception. 1: to enable reception.
TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
RB8	In Modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission, Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

Timer/Counter 2 Control Register (T2CON)

Location	7	6	5	4	3	2	1	0	Reset Value
C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#	00H

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflow to be used for the transmit clock.
EXEN2	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/T2#	Timer or counter select (Timer 2) 0: Internal timer (OSC/6 in 6 clock mode, OSC/12 in 12 clock mode) 1: External event counter (falling edge triggered)
CP/RL2#	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Timer/Counter 2 Mode Control (T2MOD)

Location	7	6	5	4	3	2	1	0	Reset Value
C9H	-	-	-	-	-	-	T2OE	DCEN	xxxxxx00b

Symbol	Function
-	Not implemented, reserved for future use. **Note:** User should not write ‘1’s to reserved bits. The value read from a reserved bit is indeterminate.
T2OE	Timer 2 Output Enable bit.
DCEN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter.

Flash Memory Programming

The device internal flash memory can be programmed or erased using In-Application Programming (IAP).

Product Identification

The Read-ID command accesses the Signature Bytes that identify the device and the manufacturer as SST. External programmers primarily use these Signature Bytes in the selection of programming algorithms.

Table 11: Product Identification

	Address	Data
Manufacturer's ID	30H	BFH
Device ID	31H	F7H
Device ID (extended)	32H	A0H

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In-Application Programming

The IAP/ISP functions are issued via the SST mail box scheme. Detailed flash block operations are performed by the flash control unit. While the flash control executes IAP commands, the CPU is on hold since there is only one physical flash block in the SST89C58RC devices. When IAP commands finish, the CPU can resume execution of the application code. So the application code needs to turn off the interrupt or turn off the peripheral modules before it issues IAP commands since the CPU cannot respond to the interrupt or poll the SFR status.

The IAP supports the following commands:

1. Chip-Erase
2. Partition0-Erase
3. Sector-Erase
4. Byte-Program
5. Byte-Verify
6. Secure Page (Page-Level Security Command)
   Secure-Page 0, 1, 2, 3, 4
7. Secure Chip (Chip-Level Security Command)
   Disable-Extern-IAP
   Disable-Extern-Boot
   Disable-Extern-MOVC
   Disable-Extern-Host-Cmd
8. Enable Clock Double
9. Boot Option Command
   Boot-From User-Vector
   Boot-From-Zero
   Set-User-Boot-Vector

Table 12: IAP Commands

Operation	SFCM [6:0]	SFAH	SFAL	SFDT
Chip-Erase	01	XX	XX	55
Partition0-Erase	0D	XX	XX	55
Sector-Erase	0B	AH	AL	XX
Byte-Program	0E	AH	AL	DI
Byte-Verify (Read)	0C	AH	AL	DO
Secure-Page0	03	90	XX	XX
Secure-Page1	03	91	XX	XX
Secure-Page2	03	92	XX	XX
Secure-Page3	03	93	XX	XX
Secure-Page4	03	94	XX	XX
Disable-Extern-IAP	05	B0	XX	XX
Disable-Extern-Boot	05	B1	XX	XX
Disable-Extern-MOVC	05	B2	XX	XX
Disable-Extern-Host-Cmd	05	B3	XX	XX
Enable-Clock-Double	08	E0	XX	XX
Boot-From-User-Vector	08	E1	XX	XX
Boot-From-Zero	08	E2	XX	XX
Set-User-Boot-Vector	09	F0	XX	DI

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Note: Note: VIL = Input Low Voltage: VIH = Input High Voltage; VIH1 = Input High Voltage (XTAL, RST); X = Don't care; AL = Address low order byte; AH = Address high order byte; DI = Data Input; DO = Data Output.

IAP Command Sequence

In order to protect the flash during the power-off condition, the application needs to write a special, sequential command sequence to the SFCM SFR address before issuing a valid IAP command.

Table 13: Command Sequence Table

Action	Access Space in IAP	Feed Sequence
Access FLASH Partition 0	0x0000~0x7FFF	1. Write A2H to SFIS0 (097H) 2. Write DFH to SFIS1 (0C4H) 3. Then write IAP command to SFCM (0B2H)
Access FLASH Partition 1	0X0000~0X07FF	1. Write A2H to SFIS0 (097H) 2. Write FDH to SFIS1 (0C4H) 3. Then write IAP command to SFCM (0B2H)

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All of the following commands can only be initiated in the IAP mode. In all situations, writing the control byte to the SFCM register will initiate all of the operations. A feed sequence is required prior to issuing commands through SFCM. Without the feed sequence all IAP commands are ignored. Sector-Erase, Byte-Program, and Byte-Verify commands will not be carried out on a specific memory page if the security locks are enabled on the memory page.

The Byte-Program command is to update a byte of flash memory. If the original flash byte is not FFH, it should first be erased with an appropriate Erase command.

Warning: Do not attempt to write (Program or Erase) to a sector that the code is currently fetching from. This will cause unpredictable program behavior and may corrupt program data.

Chip-Erase

Chip-Erase IAP command erases all bytes in both memory partitions. This command is only allowed when EA# = 0 (external memory execution).

Chip-Erase ignores the Security setting status and will erase all settings on all pages and the different chip-level security restrictions, returning the device to its Unlocked state. The Chip-Erase command will also erase the boot vector setting. Upon completion of Chip-Erase command, the chip will boot from the default setting. See Table 14 for the default boot vector setting

Table 14: Default Boot Vector Settings

Device	Address
SST89C58RC	0F800H

T0-0.1 25100

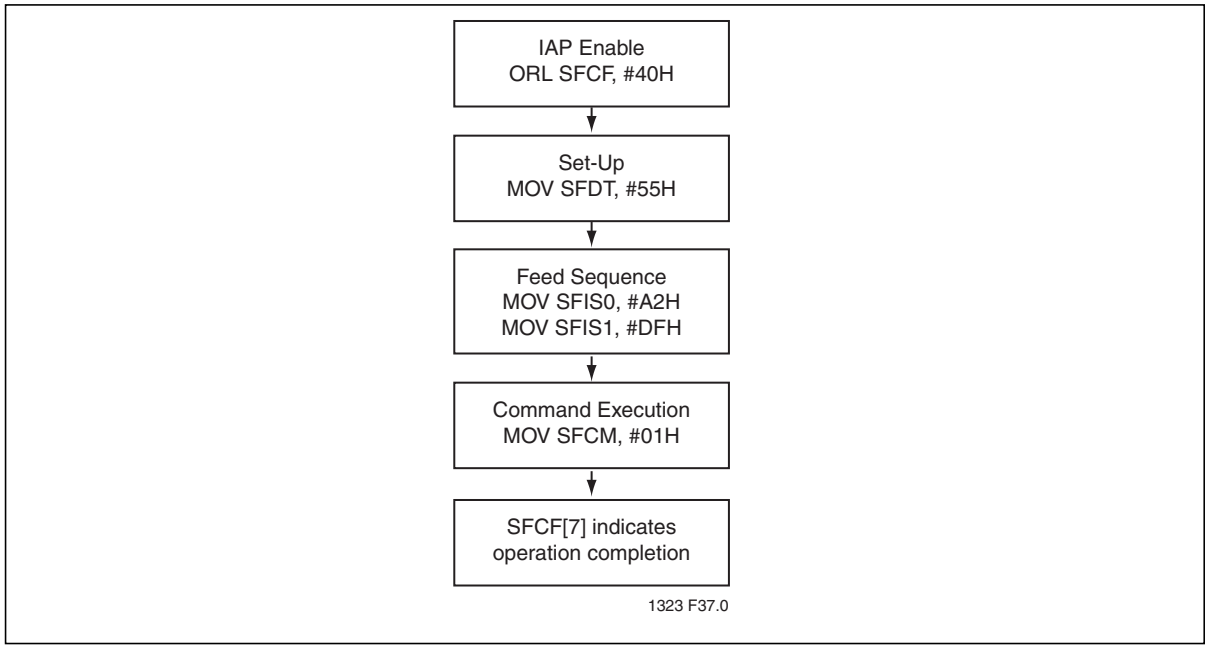

Figure 8: Chip-Erase

Partition0-Erase

The Partition0-Erase command erases all bytes in memory partition 0. All security bits associated with Page0-3 are also reset.

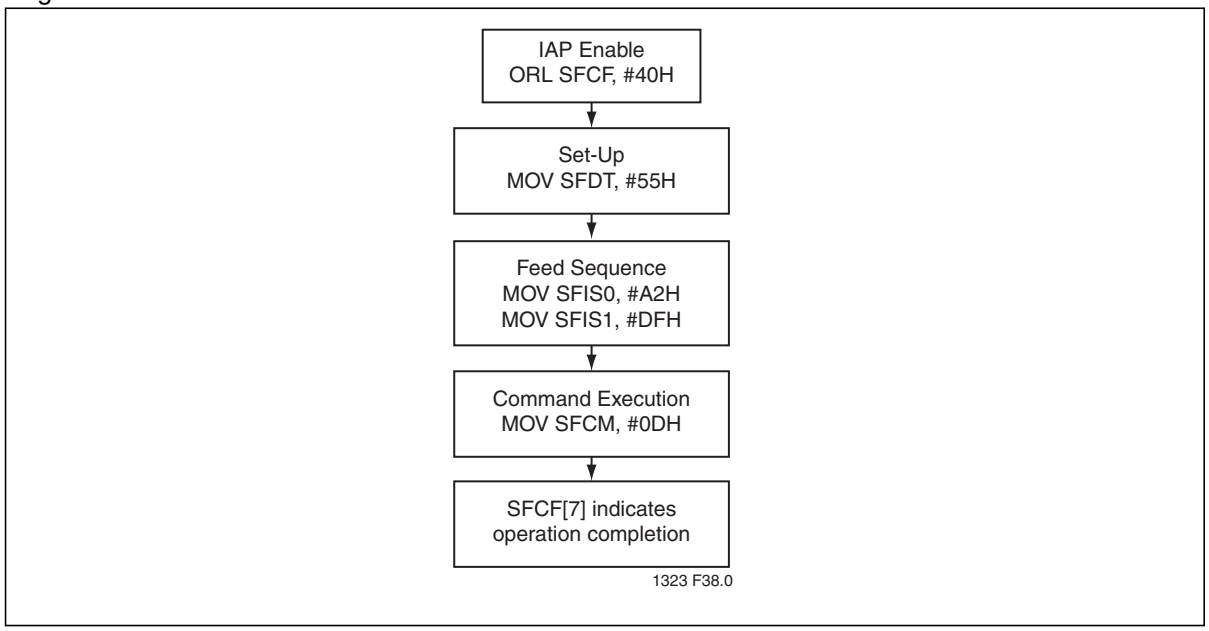

Figure 9: Partition0-Erase

Sector-Erase

The Sector-Erase command erases all of the bytes in a sector. The sector size for the flash memory blocks is 128 Bytes. The selection of the sector to be erased is determined by the contents of SFAH and SFAL.

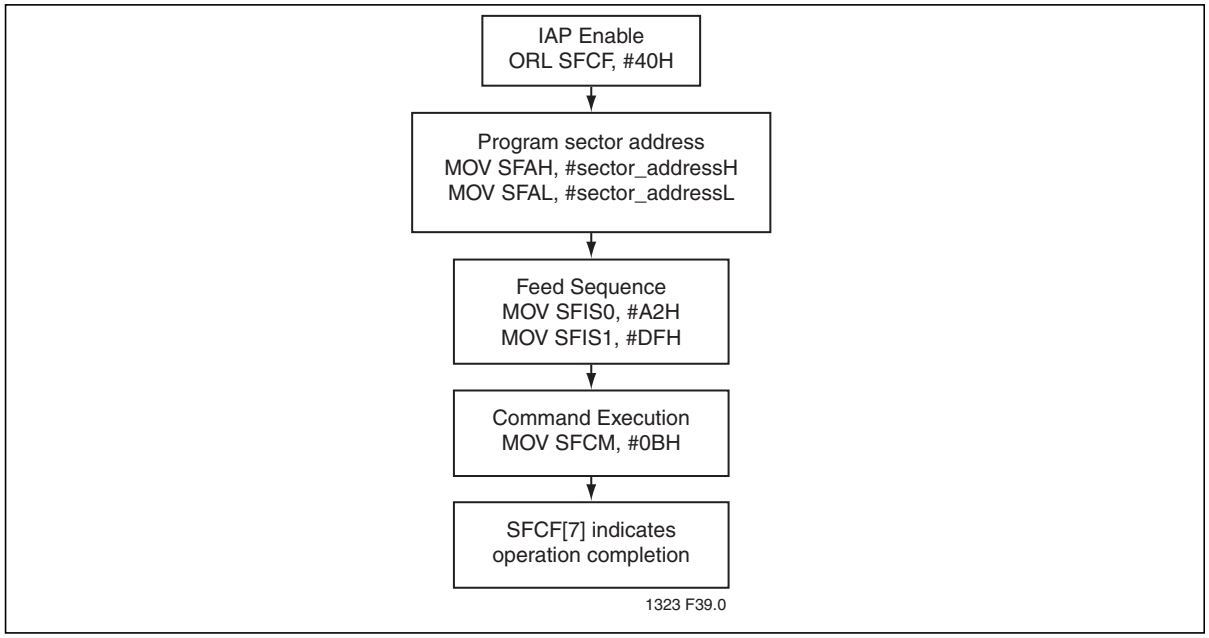

Figure 10: Sector-Erase

Byte-Program

The Byte-Program command programs data into a single byte. The address is determined by the contents of SFAH and SFAL. The data byte is in SFDT.

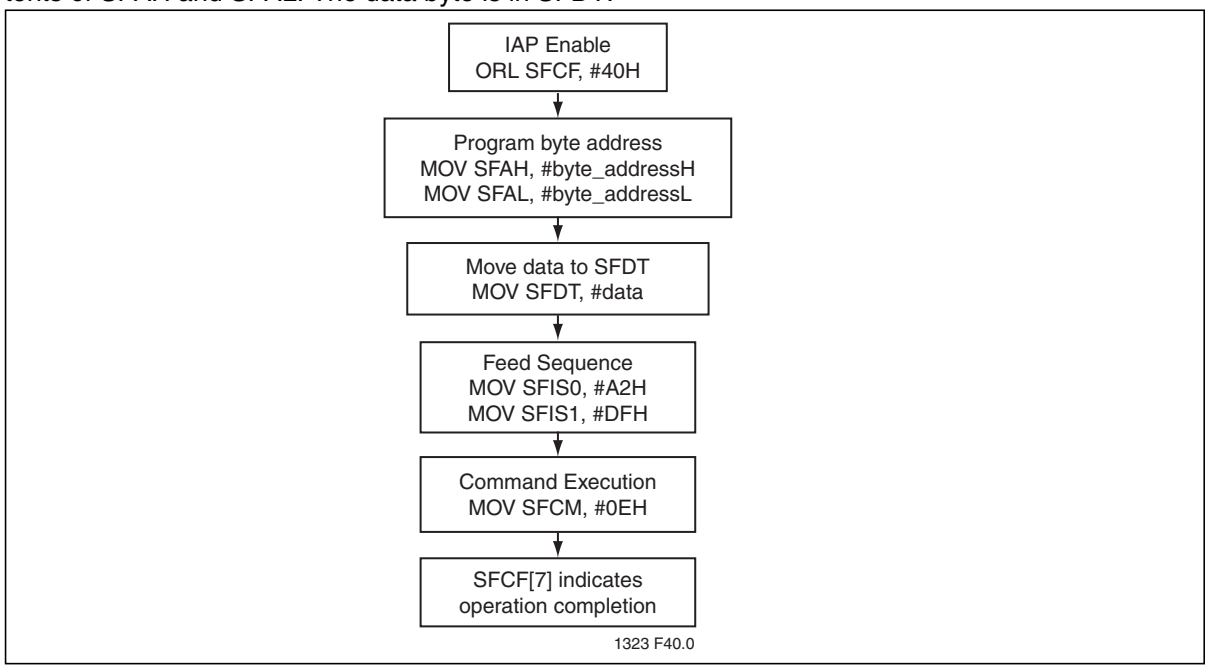

Figure 11: Byte-Program

Byte-Verify

The Byte-Verify command allows the user to verify that the device has correctly performed an Erase or Program command. Byte-Verify command returns the data byte in SFDT if the command is successful. The previous flash operation has to be fully completed before a Byte-Verify command can be issued.

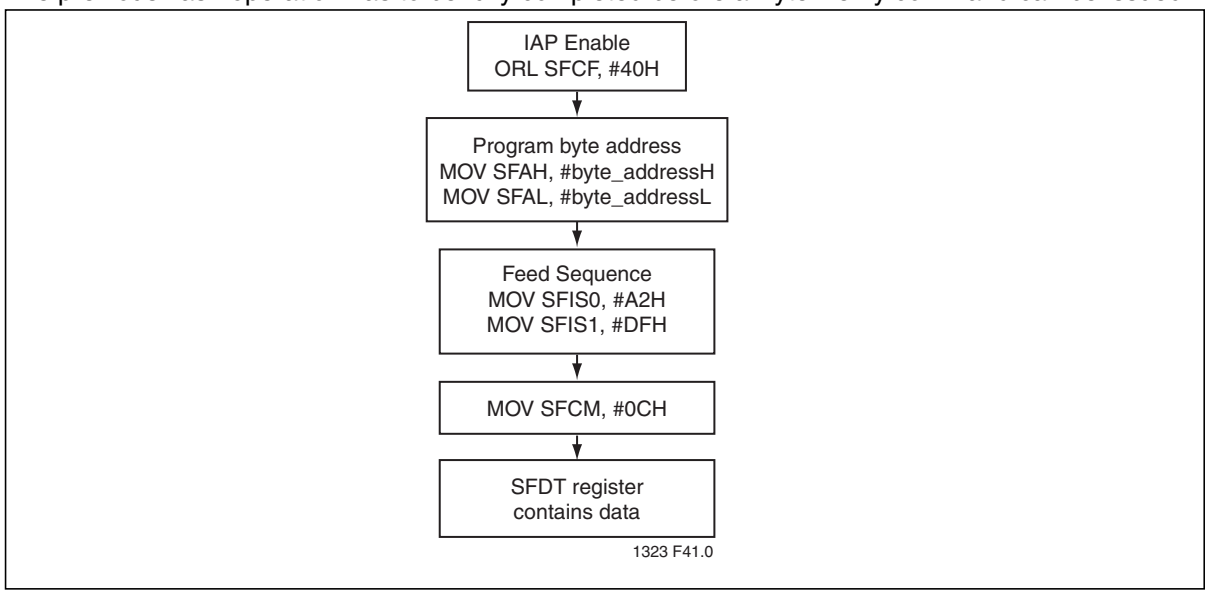

Figure 12: Byte-Verify

Secure-Page0, Secure-Page1, Secure-Page2, Secure-Page3, and Secure-Page4

Secure-Page0, Secure-Page1, Secure-Page2, Secure-Page3, and Secure-Page4 commands are used to program the page security bits. Upon completion of any of these commands, the page security options will be updated immediately.

Page security bits previously in un-programmed state can be programmed by these commands. The factory setting for these bits is all '1's which indicates the pages are not security locked.

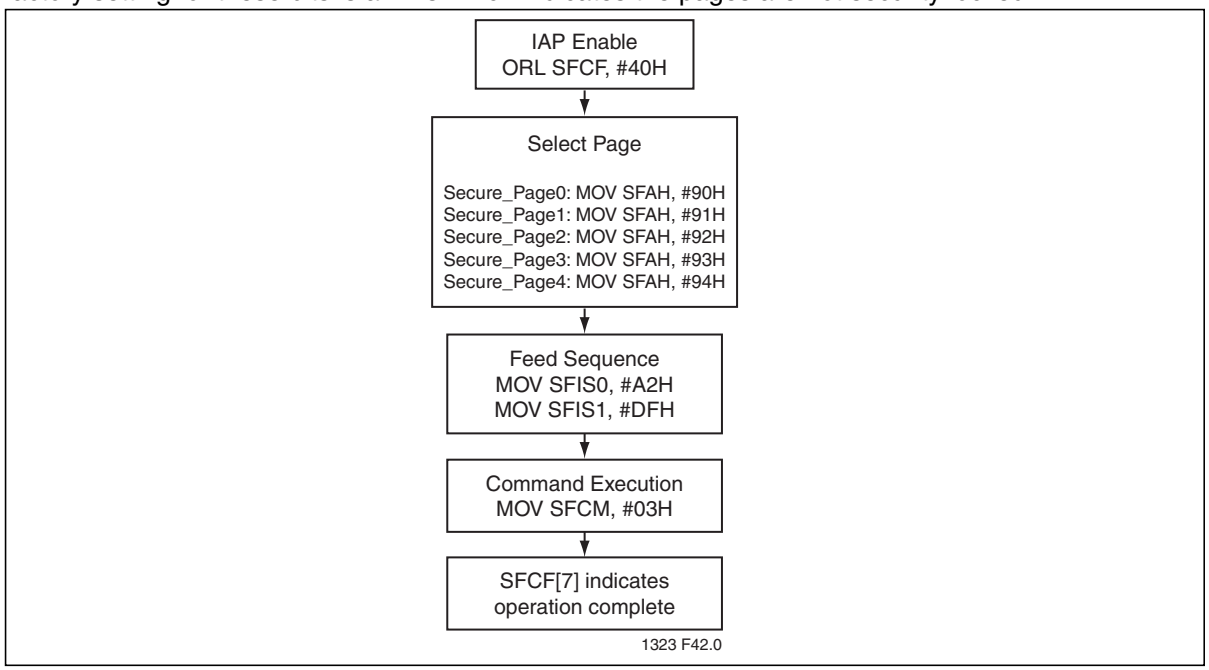

Figure 13: Secure-Page0-4

Enable-Clock-Double

Enable-Clock-Double command is used to make the MCU run at 6 clocks per machine cycle. The standard (default) is 12 clocks per machine cycle (i.e. clock double command disabled).

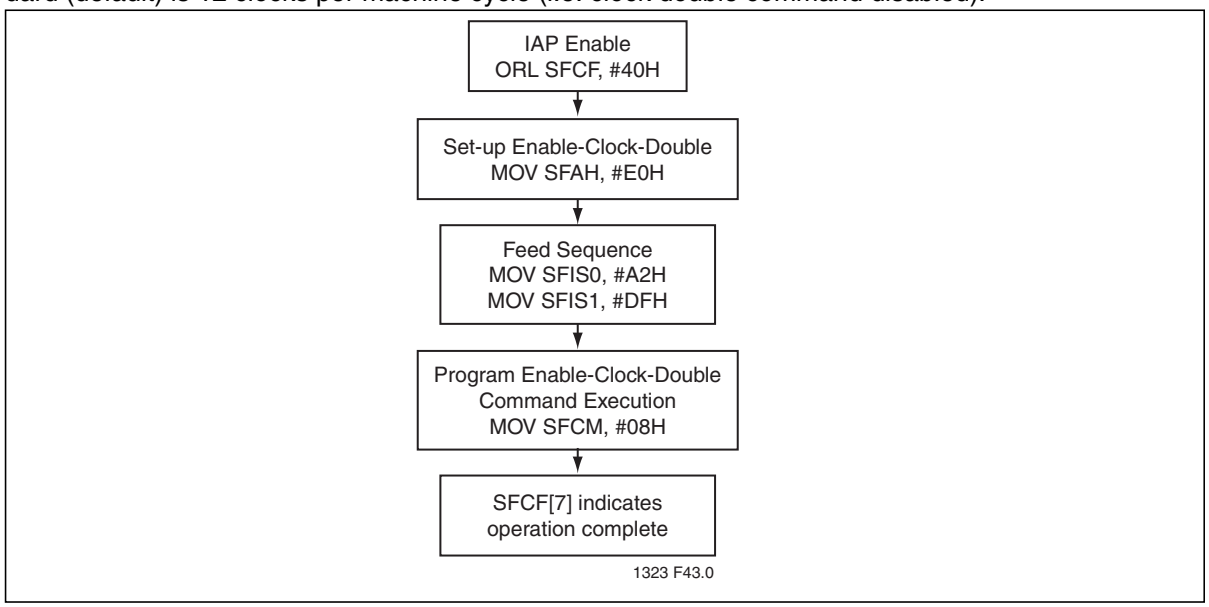

Figure 14: Enable-Clock-Double

In-System Programming

The bootstrap loader (BSL) is located in partition 1 and cannot be accessed unless the SFR AUXR1 (Address = A2H), Bit 5 is enabled. The default value of this bit after reset is '1' unless the "Boot-From-Zero" bit is non-zero during reset, or P1.0 and P1.1 are pulled low while EA# is held high on the falling edge of the reset.

Normal Mode

If the “Boot-From-Zero” bit is ‘0’, the MCU boots from 0x0000. If both the “Boot-From-Zero” bit and the “Boot-From-User-Vector” bit are ‘1’, the USER Boot Vector is applicable (0xF800).

If the “Boot-From-Zero” bit is ‘1’ and the “Boot-From-User-Vector” bit is ‘0’, the USER Boot Vector is applicable. This is used as the high byte of the program counter (PC) starting address while the lower byte of PC is 00H. See Figure 15.

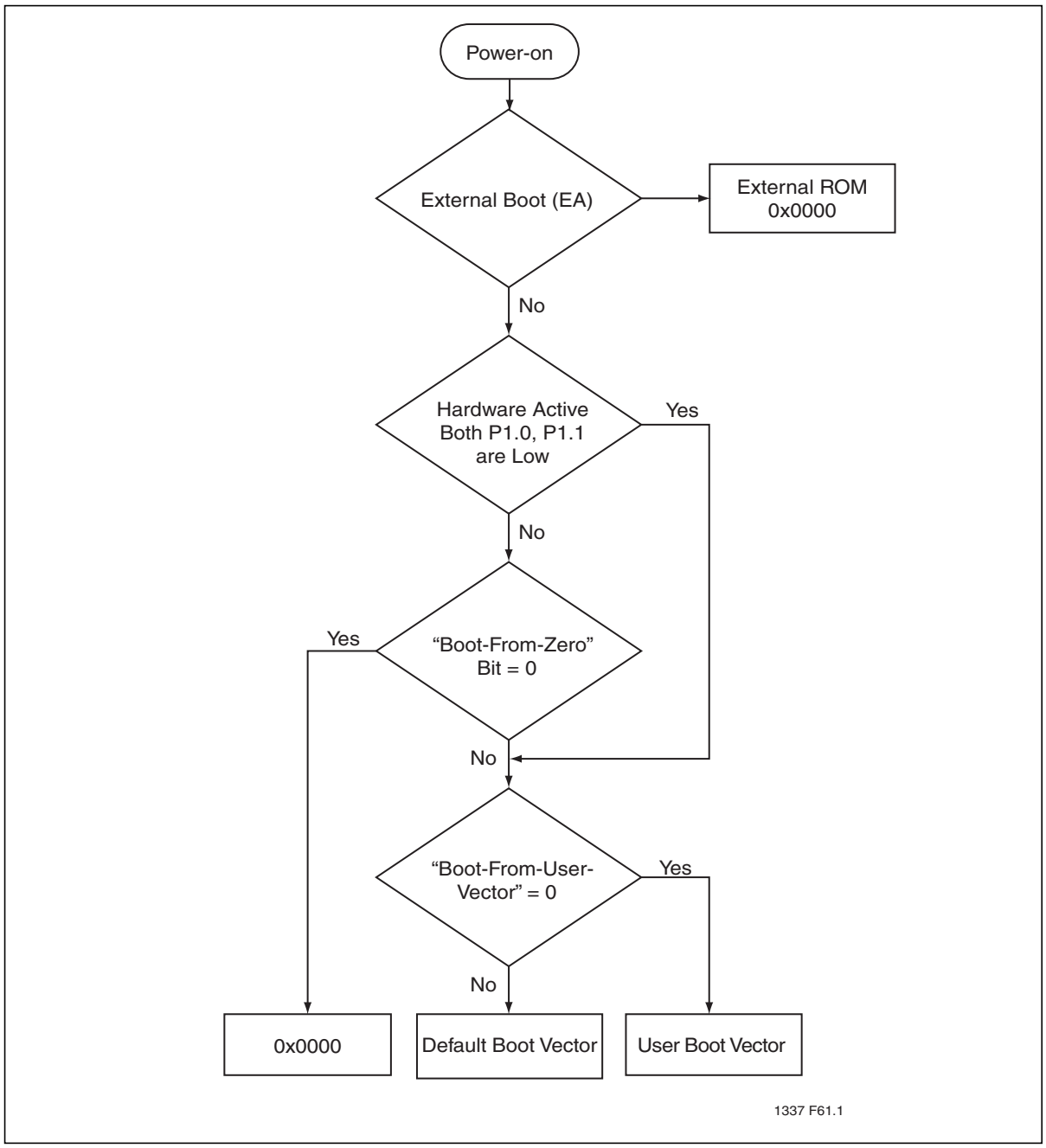

Figure 15: Boot Sequence Flowchart

Hardware Enter Mode

The hardware checks P1.0 and P1.1 at the falling edge of the reset. If both P1.0 and P1.1 are '0', then the program starts based on the boot vector value regardless of the Boot Vector Jumper bit value. The software checks the Boot status bit in the SFCF register to determine whether the latest boot was based on the hardware enter mode. See Figure 16.

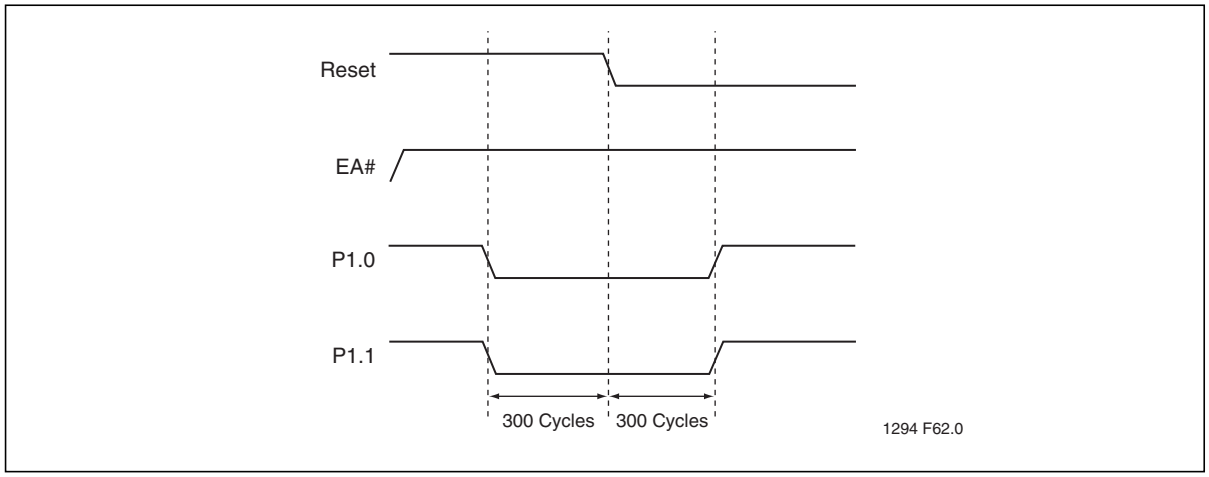

Figure 16: Hardware Enter Mode

Timers/Counters

Timers

The device has three 16-bit registers that can be used as either timers or event counters. The three timers/counters are denoted Timer 0 (T0), Timer 1 (T1), and Timer 2 (T2). Each is designated a pair of 8-bit registers in the SFRs. The pair consists of a most significant (high) byte and least significant (low) byte. The respective registers are TL0, TH0, TL1, TH1, TL2, and TH2.

Timer Set-up

Refer to Table 7 for TMOD, TCON, and T2CON registers regarding timers T0, T1, and T2. The following tables provide TMOD values to be used to set up Timers T0, T1, and T2.

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set separately to turn the timer on.

Table 15: Timer/Counter 0

	Mode	Function	TMOD	
			Internal Control[1]	External Control[2]
Used as Timer	0	13-bit Timer	00H	08H
	1	16-bit Timer	01H	09H
	2	8-bit Auto-Reload	02H	0AH
	3	Two 8-bit Timers	03H	0BH
Used as Counter	0	13-bit Timer	04H	0CH
	1	16-bit Timer	05H	0DH
	2	8-bit Auto-Reload	06H	0EH
	3	Two 8-bit Timers	07H	0FH

T0-0.0 25100

1. The Timer is turned ON/OFF by setting/clearing bit TR0 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT0# (P3.2) when TR0 = 1 (hardware control).

Table 16: Timer/Counter 1

	Mode	Function	TMOD	
			Internal Control[1]	External Control[2]
Used as Timer	0	13-bit Timer	00H	80H
	1	16-bit Timer	10H	90H
	2	8-bit Auto-Reload	20H	A0H
	3	Does not run	30H	B0H
Used as Counter	0	13-bit Timer	40H	C0H
	1	16-bit Timer	50H	D0H
	2	8-bit Auto-Reload	60H	E0H
	3	Not available	-	-

T0-0.0 25100

1. The Timer is turned ON/OFF by setting/clearing bit TR1 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT1# (P3.3) when TR1 = 1 (hardware control).

Table 17: Timer/Counter 2

	Mode	T2CON	
		Internal Control[1]	External Control[2]
Used as Timer	16-bit Auto-Reload	00H	08H
	16-bit Capture	01H	09H
	Baud rate generator receive and transmit same baud rate	34H	36H
	Receive only	24H	26H
	Transmit only	14H	16H
Used as Counter	16-bit Auto-Reload	02H	0AH
	16-bit Capture	03H	0BH

T0-0.0 25100

1. Capture/Reload occurs only on timer/counter overflow.
2. Capture/Reload occurs on timer/counter overflow and a 1 to 0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generating mode.

Programmable Clock-Out

A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed:

1. to input the external clock for Timer/Counter 2, or
2. to output a 50% duty cycle clock ranging from 122 Hz to 8 MHz at a 16 MHz operating frequency (61 Hz to 4 MHz in 12 clock mode).

To configure Timer/Counter 2 as a clock generator, bit C/#T2 (in T2CON) must be cleared and bit T20E in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$\frac{\text{Oscillator Frequency}}{n \times (65536 - \text{RCAP2H, RCAP2L})}$$

n =2 (in 6 clock mode) or 4 (in 12 clock mode)

Where (RCAP2H, RCAP2L) = the contents of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode, Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will not be the same.

Serial I/O

Full-Duplex, Enhanced UART

The device serial I/O port is a full-duplex port that allows data to be transmitted and received simultaneously in hardware by the transmit and receive registers, respectively, while the software is performing other tasks. The transmit and receive registers are both located in the Serial Data Buffer (SBUF) special function register. Writing to the SBUF register loads the transmit register, and reading from the SBUF register obtains the contents of the receive register.

The UART has four modes of operation which are selected by the Serial Port Mode Specifier (SM0 and SM1) bits of the Serial Port Control (SCON) special function register. In all four modes, transmission is initiated by any instruction that uses the SBUF register as a destination register. Reception is initiated in mode 0 when the Receive Interrupt (RI) flag bit of the Serial Port Control (SCON) SFR is cleared and the Reception Enable/ Disable (REN) bit of the SCON register is set. Reception is initiated in the other modes by the incoming start bit if the REN bit of the SCON register is set.

Framing Error Detection

Framing Error Detection is a feature, which allows the receiving controller to check for valid stop bits in modes 1, 2, or 3. Missing stops bits can be caused by noise in serial lines or from simultaneous transmission by two CPUs.

Framing Error Detection is selected by going to the PCON register and changing SMOD0 = 1 (see Figure 17). If a stop bit is missing, the Framing Error bit (FE) will be set. Software may examine the FE bit after each reception to check for data errors. After the FE bit has been set, it can only be cleared by software. Valid stop bits do not clear FE. When FE is enabled, RI rises on the stop bit, instead of the last data bit (see Figure 18 and Figure 19).

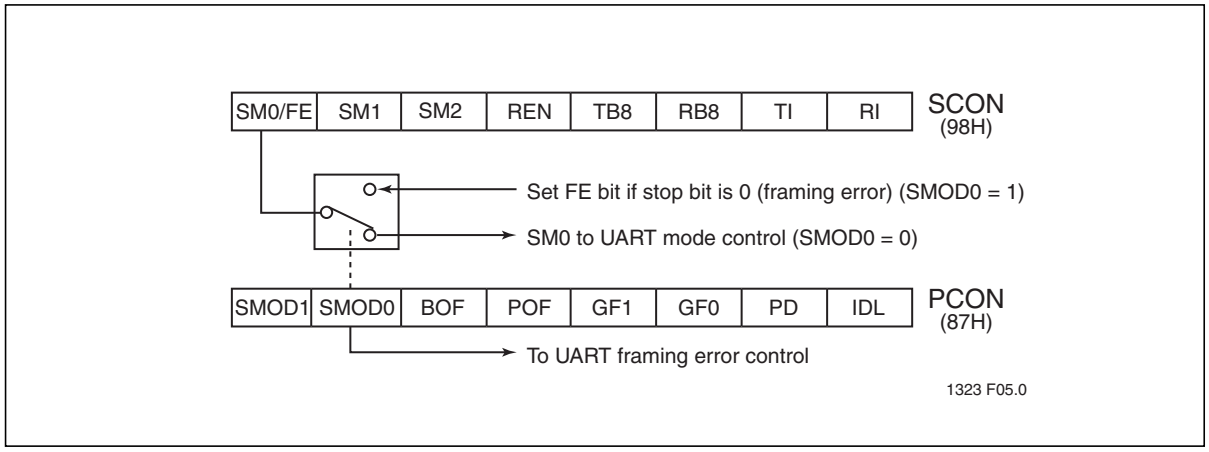

Figure 17: Framing Error Block Diagram

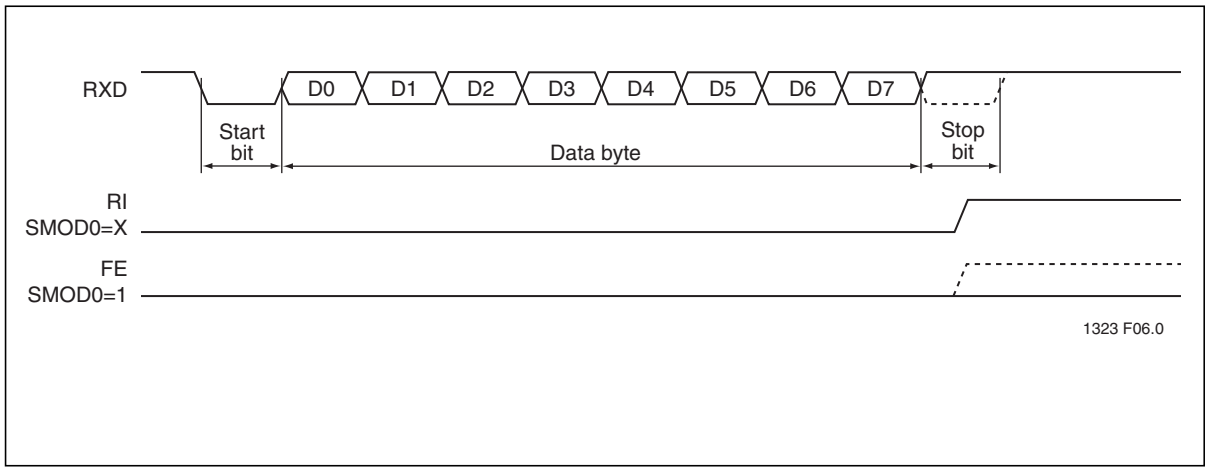

Figure 18: UART Timings in Mode 1

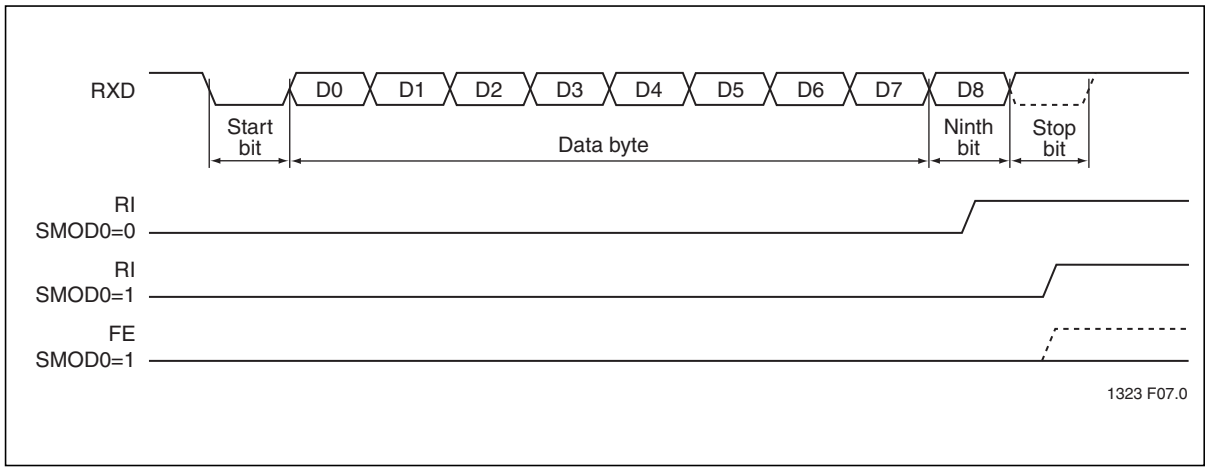

Figure 19: UART Timings in Modes 2 and 3

Automatic Address Recognition

Automatic Address Recognition (AAR) helps to reduce the time and power required to communicate with multiple serial devices. Each device shares the same serial link, but has its own address. In this configuration, a device is only interrupted when it receives its own address, thus eliminating the software overhead to compare addresses.

This same feature helps to save power because it can be used in conjunction with idle mode to reduce the system's overall power consumption. AAR allows the other slaves to remain in idle mode while only one is interrupted. By limiting the number of interruptions, the total current draw on the system is reduced.

There are two ways to communicate with slaves: a group of them at once, or all of them at once. To communicate with a group of slaves, the master sends out an address called the given address. To communicate with all the slaves, the master sends out an address called the "broadcast" address.

AAR can be configured as mode 2 or 3 (9-bit modes) and setting the SM2 bit in SCON. Each slave has its own SM2 bit set waiting for an address byte (9th bit = 1). The Receive Interrupt (RI) flag will only be set when the received byte matches either the given address or the broadcast address. Next, the slave then clears its SM2 bit to enable reception of the data bytes (9th bit = 0) from the master. When the 9th bit = 1, the master is sending an address. When the 9th bit = 0, the master is sending actual data.

If mode 1 is used, the stop bit takes the place of the 9th bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit. Note that mode 0 cannot be used. Setting SM2 bit in the SCON register in mode 0 will have no effect.

Each slave's individual address is specified by SFR SADDR. SFR SADEN is a mask byte that defines "don't care" bits to form the given address when combined with SADDR. See the example below:

Using the Given Address to Select Slaves

Any bits masked off by a 0 from SADEN become a "don't care" bit for the given address. Any bit masked off by a 1, becomes ANDED with SADDR. The "don't cares" provide flexibility in the user-defined addresses to address more slaves when using the given address.

Shown in the example above, Slave 1 has been given an address of 1111 0001 (SADDR). The SADEN byte has been used to mask off bits to a given address to allow more combinations of selecting Slave 1 and Slave 2. In this case for the given addresses, the last bit (LSB) of Slave 1 is a "don't care" and the last bit of Slave 2 is a 1. To communicate with Slave 1 and Slave 2, the master would need to send an address with the last bit equal to 1 (e.g. 1111 0001) since Slave 1's last bit is a don't care and Slave 2's last bit has to be a 1. To communicate with Slave 1 alone, the master would send an address with the last bit equal to 0 (e.g. 1111 0000), since Slave 2's last bit is a 1. See the tables below for other possible combinations.

Select Slave 1 Only		
Slave 1	**Given Address**	**Possible Addresses**
	1111 0X0X	1111 0000 1111 0100

Select Slave 2 Only		
Slave 2	**Given Address**	**Possible Addresses**
	1111 0XX1	1111 0111 1111 0011

Select Slaves 1 and 2	
Slaves 1 and 2	**Possible Addresses**
	1111 0001 1111 0101

If the user added a third slave such as the example below:

Slave 1			**Slave 2**			**Slave 3**		
SADDR	=	1111 0001	SADDR	=	1111 0011	SADDR	=	1111
SADEN	=	1111 1010	SADEN	=	1111 1001	SADEN	=	1111
GIVEN	=	1111 0X0X	GIVEN	=	1111 0XX1	GIVEN	=	1111

Select Slave 3 Only		
Slave 2	**Given Address**	**Possible Addresses**
	1111 X0X1	1111 1011 1111 1001

The user could use the possible addresses above to select slave 3 only. Another combination could be to select slave 2 and 3 only as shown below.

Select Slaves 2 and 3 Only	
Slaves 2 and 3	**Possible Addresses**
	1111 0011

More than one slave may have the same SADDR address as well, and a given address could be used to modify the address so that it is unique.

Using the Broadcast Address to Select Slaves

Using the broadcast address, the master can communicate with all the slaves at once. It is formed by performing a logical OR of SADDR and SADEN with 0s in the result treated as “don’t cares”.

Slave 1		
1111 0001	=	SADDR
+1111 1010	=	SADEN
1111 1X11	=	Broadcast

“Don’t cares” allow for a wider range in defining the broadcast address, but in most cases, the broadcast address will be FFH.

On reset, SADDR and SADEN are “0”. This produces an given address of all “don’t cares” as well as a broadcast address of all “don’t cares.” This effectively disables Automatic Addressing mode and allows the micro controller to function as a standard 8051, which does not make use of this feature.

Enhanced SMBus Interface

The SST89C58RC includes two enhanced SUBus interfaces. The enhanced SMBus uses two wires (SDA and SCL) to transfer information between devices connected to the bus.

SUBus Features

- Only two lines required (SDA and SCL)
- Master and slave modes
- 7-bit slave address support
- Supports 0-400 Kbit data transfer speed
- SCL line low duration time-out
- Bus idle state detection interrupt
- SCL configurable duty cycle
- SDA line hold time configuration

SMBus Description

The SST89C58RC complies with the System Management Bus Specification, version 2.0. Reads and writes are byte oriented with the SMBus interface to independently control the serial transfer of data from the system controller to the interface. See figure 6-4 for a typical SMBus configuration.

By using the system clock as the bit rate clock source, data is transferred at speeds up to 400 Kbits per second as a master or a slave. However, when using the TIMER1 as the bit rate clock source, data transfer is reduced to speeds only up to 200 Kbits. These data transfer speeds are faster than those specified by the SMBus specifications.

A typical SMBus configuration is shown in Figure 20 and Figure 21 shows how data transfer is accomplished on the bus.

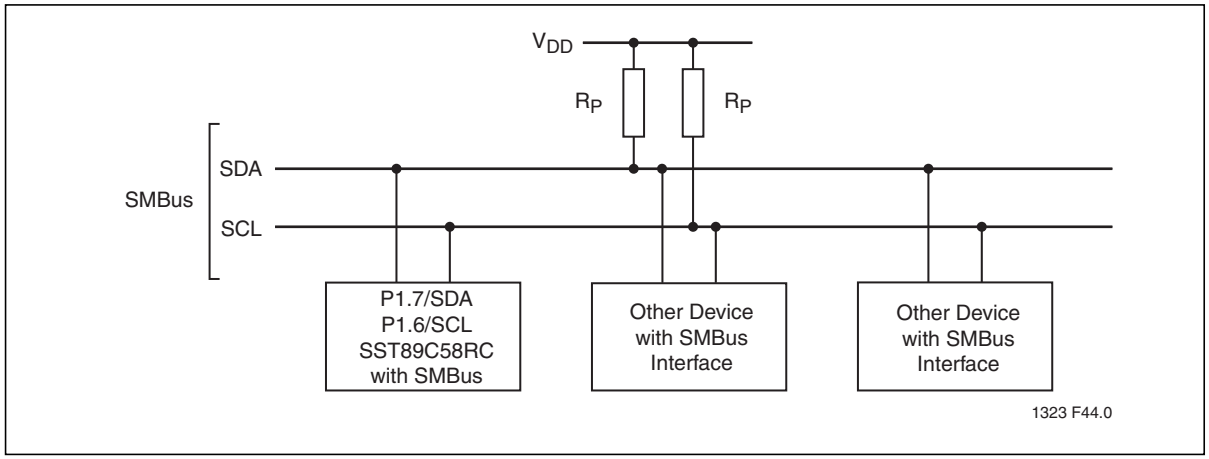

Figure 20: Typical SMBus Configuration

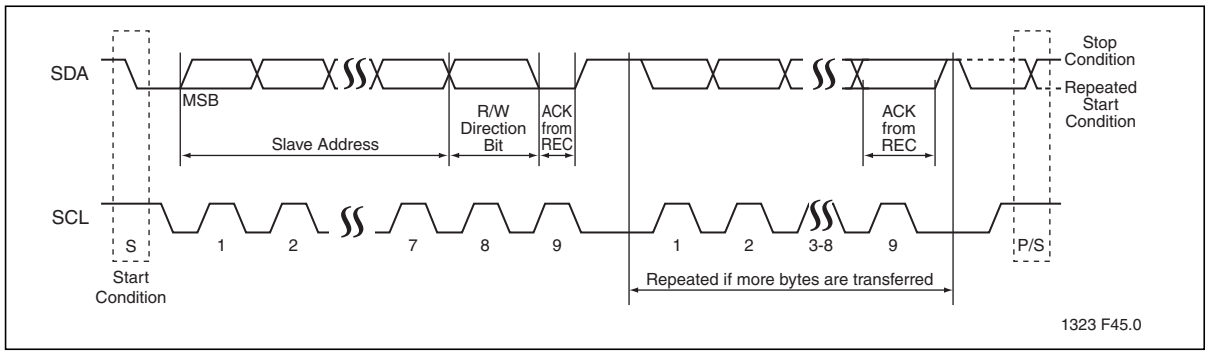

Figure 21: Data Transfer on the SUBus

SDA (Serial Data Line)

The SDA line is the SMBus serial data line, and is primarily driven by the master or slave transmitter. The SDA is changeable when SCL is low, and SDA is stable when SCL is high. Perform bus arbitration on SDA when SCL is high.

SCL (Serial Clock Line)

The SCL line is the SMBus serial clock line which provides synchronized transmissions between master and slave devices and is driven by the master devices. When multiple masters drive the SCL simultaneously, a wired-AND combines all signals into one synchronized clock signal. The slowest clock determines the synchronized LOW period and the fastest clock determines the HIGH period.

SMBus Modes of Operation

The SMBus transaction begins with a START which is followed by an address byte and data, and then ends with a STOP. An acknowledge bit from the receiver follows the address byte, which consists of a 7-bit address plus a direction bit, and each data byte. The direction bit (R/W), which occupies the least significant bit position of the address, indicates a READ operation when set to logic ‘1’, and a WRITE operation when set to logic ‘0’. The master can address multiple slaves simultaneously using a general call address (0x00 + R/W), which is recognized by all slave devices.

The master initiates all transactions with one or more target-addressed slave devices. After generating a START condition, the master transmits the address and direction bit. For a master-to-slave WRITE operation, data is transmitted a byte at a time from the master; waiting for an acknowledge after each byte from the slave. For a slave-to-master READ operation, the slave awaits an acknowledge after each byte from the master. The master generates a STOP which ends the transaction and frees the bus at the completion of the data transfer.

At any time, the SMBus is configured to operate in either master or slave mode.

Master Transmitter Mode

The serial data is output through SDA while SCL supplies the serial clock. The first transmitted byte contains the slave address and the data direction bit. In this WRITE operation mode, the data direction bit (R/W) will be logic ‘0’ and the master transmits serial data. After each byte is transmitted, an acknowledge bit is received from the slave. START and STOP conditions are output by the master to indicate the beginning and the end of a serial transfer.

Master Receiver Mode

The serial data is received via SDA while SCL supplies the serial clock. The first master-transmitted byte contains the slave address and the data direction bit. In this READ mode, the data direction bit (R/W) will be logic ‘1’. Serial data is received from the slave via SDA while SCL outputs the serial clock from the master. After each byte is received from the slave, an acknowledge bit is transmitted by the master. START and STOP conditions are output to indicate the beginning and end of a serial transfer.

Slave Receiver Mode

The serial data is output through SDA while SCL supplies the serial clock. The first transmitted byte contains an address and the data direction bit. In this READ mode, the data direction bit (R/W) will be logic ‘1’. Serial data is transmitted to the master if the address received matches the slave’s assigned address or if a general call address is received. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer.

Slave Transmitter Mode

The serial data is received via SDA while SCL supplies the serial clock. The first transmitted byte contains an address and the data direction bit. In this WRITE operation mode, the data direction bit (R/W) will be logic ‘0’. Serial data is transmitted to the master if the address received matches the slave’s assigned address or if a general call address is received. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer.

Timeouts

SCL Low Timeout

Use the TOE bit to enable monitoring of the SCL low timeout function. When the TOE is set, the SMBUS controls the TIMER1 to count during every SCL low period. At every falling-edge of the SCL, a reload counter pulse is generated to TIMER1. At every rising-edge of the SCL, a count stop pulse is generated to TIMER1. If the TIMER1’s counter is reloaded and counting, the last count stop pulse will cause the TIMER1 to generate an interrupt for SCL low timeout.
1 = SCL Low timeout enable
0 = SCL Low timeout disabled

SCL High (SMBus Free) Timeout

According to SMBus specifications, the bus is designated as free if the device holds the SCL and SDA lines high for more than 10 SMBus bit rate cycles.

SMBus SFR

The SST89C58RC has two identical SMBus interfaces, each identical with the exception of the SFR addresses and the I/O pins associated with each interface.

The SMBus interfaces operate as a master and/or slave and can function on a bus with multiple masters. The SMBus controls the SDA, the generation and synchronization of the SCL, the arbitration logic, and the control and generation of START/STOP. The following SFRs are associated with the SMBus.

Table 18: SMBus SFR Functions

SFR	Function
SM0CON0 / SM0CON1	Configures SMBus0
SM0STA	Controls status of SMBus0
SM0DAT	Data register for transmitting and receiving SMBus0 data
SM0ADR	Indicates SMBus0 slave address
SM0SCLH / SM0SCLL	Configures SMBus0 High/Low duty
SM1CON0 / SM1CON1	Configures SMBus1
SM1STA	Controls status of SMBus1
SM1DAT	Data register for transmitting and receiving SMBus1 data
SM1ADR	Indicates SMBus1 slave address
SM1SCLH / SM1SCLL	Configures SMBus1 High/Low duty

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SMBus Control Register

SMBus control register SM0CON0 configures and controls the SMBus interface making all bits in the register software readable and writable. The SMBus hardware sets the Serial Interrupt flag (SI_0, SMCON0.4) to logic ‘1’ when a valid serial interrupt condition occurs; and clears the Stop flag (STO_5, SM0CON0.4) to logic ‘0’ when a STOP condition is present on the bus.

Enable the SMBus interface, by setting the SMBEN_0 flag to logic ‘1’; disable and remove it from the bus by clearing the ENSMB flag to logic ‘0’. To reset the SMBus communication, momentarily clear the SMBEN flag and then reset it to logic ‘1’. Using SMBEN to temporarily remove a device from the bus will result in lost information. The best method to temporarily remove a device from the bus is to use the Assert Acknowledge (AA) flag.

If the bus is idle, SMBus generates a START condition after a delay of 1.5 baud rate clock cycle when the Start flag (STA_0, Sm0CON0.6) is set. If STA and STADY bits are both set in the first transmission (that is, the SMBEN is set from “0” to “1”) and bus is idle, a START condition will be generated after 10 baud rate clock cycles. If SMBUS is already in the master mode and one or more than one bytes has been transmitted or received, a repeated START condition will be generated when STA bit is set. If SMBus is in addressed slave mode and the STA is set, no START condition will be generated until SMBus enters “not addressed slave” mode and the bus is idle. STA bit only can be cleared by software.

In master mode, a STOP condition is transmitted on the bus when the Stop flag (STO_0, SM0CON0.5) is set. And STO bit is cleared by hardware automatically after a STOP condition is detected on the bus. If STA and STO bits are both set, the STOP condition is transmitted firstly, and then the START condition is transmitted.

In slave mode, STO is set to recover SMBus from an error condition or generate a internal STOP for a forced access to the bus. No STOP condition will be transmitted on the bus and the hardware behaves as if a STOP condition has been received, SMBUS switches to “not addressed” slave receiver mode. STO bit is cleared by hardware after one system clocks. STO bit can not be set when SMBEN is zero.

The Serial Interrupt flag (SI_0, SM0CON0.4) can be set in any possible SMBus status except for status “0xD0” and status “0xF8. If EA and ES1 bits are set, an interrupt will requested when SI is set. When SI flag is set by hardware, the SCL line is held to LOW until it is cleared by software (except for the status “0xD0”, which will not hold the SCL line low). Only “0” can be written to clear SI flag, writing “1” has no effect to the flag. When SI flag is cleared, SMBSTA register changes to “0xF8”.

During the acknowledge clock cycle on the SCL line, the Assert Acknowledge flag (AA_0, SM0CON0.3) sets the level of the SDA line.

In slave transmitter mode, the AA flag is used to determine whether the last data byte will be transmitted or enables whether to respond its slave address or general call address.

In master receiver mode, the AA flag is used to determine to return ACK or NACK after receiving a byte. In slave receiver mode, the AA flag is used to determine to return ACK or NACK and enables whether to respond its slave address or general call address.

1 = When set to 1, an acknowledge (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line on the following situations:

1. The “own slave address” has been received.
2. The general call address has been received while the general call bit (GC) in SMBADR is set.
3. A data byte has been received while the SMBUS interface is in the Master Receiver Mode.
4. A data byte has been received while the SMBUS interface is in the addressed Slave Receiver Mode.

0 = When cleared to 0, an non-acknowledge (high level to SDA) will be returned during the acknowledge clock pulse on the SCL line on the following situations:

1. A data byte has been received while the SMBUS interface is in the Master Receiver Mode.
2. A data byte has been received while the SMBUS interface is in the addressed Slave Receiver Mode.

To enable the SMBus Free Timeout feature, set the SMBus Free Timer Enable bit (FTE, SM0CON0.2) to logic ‘1’. The bus is considered free and, if pending, a Start is generated when SCL and SDA remain high for the SMBus Free Timeout given in the SMBUS Clock Rate Register.

To enable monitoring SCL low timeout function, set the SMBus Time out Enable bit (TOE_0, SM0CON0.1) to logic ‘1’. When TOE is set, SMBUS will control the TIMER1 to count during the every SCL low period. At every SCL falling-edge of the SCL, a reload counter pulse is generated to TIMER1; at every SCL rising-edge of the SCL, a count stop pulse is generated to TIMER1. If the TIMER1’s counter is reloaded and counting, the latest count stop pulse will cause the TIMER1 to generate an interrupt for SCL low timeout.

Data Register

The SMBus Data register (SM0DAT0) holds a byte of recently received or ready-to-transmit serial data. When SI is set to logic '1', the data in the register is stable. In this state, software safely reads or writes the data register. However, when the SMBus is enabled and the SI flag is cleared to logic '0', the software must not access the SM0DAT register because the hardware may be shifting a data byte in or out of the register.

After the SM0DAT receives a byte of data, the first bit of the serial data byte is located at the MSB. As data is shifted out of the SM0DAT, beginning with the MSB, data from the bus is simultaneously shifted in.

The last data byte on the bus is always contained in the SM0DAT; thereby, ensuring that correct data is transmitted from the master to the slave in the event of lost arbitration.

Address Register

The slave address is held in the SM0ADR Address register. When in slave mode, the 7-bit address is held in the seven most significant bits, the least of which is bit 0. Bit 0 recognizes the general call address (0x00) when set to logic '1'. When the SMBus hardware is operating in master mode, the contents of the SM0ADR Address register are ignored.

Status Register

The status of the SMBus is held in the SM0STA Status register as one of 31 different 8-bit status codes. Each 8-bit status code corresponds to a unique SMBus state. When SI = '1', the three least significant bits of the status code are set to zero and the five most significant bits vary. All possible status codes are multiples of eight; which, in software, allows the status code to act as an index to branch to service routines by allowing 8 bytes of code to service the state or jump to a more extensive routine.

Set the SI flag to logic '1' to define the contents of the SM0STA register for software use. Software must not write to the SM0STA because doing so yields uncertain results. Refer to Tables 6-1 through 6-4 for the 31 SMBus states and their corresponding status codes.

Table 19: Master Transmitter Mode (1 of 2)

Status Code (SM0STA)	SMBus1 Hardware Status	Application Software Response					SMBus Hardware - Next Action
		To/From SM0DAT	To SM0CON				
			STA	STO	SI	AA	
08H	START condition transmitted	Load SLA+W	X	0	0	X	SLA+W transmitted; ACK bit received
10H	Repeat START transmitted	Load SLA+W or	X	0	0	X	SLA+W transmitted; ACK bit received
		Load SLA+R	X	0	0	X	SLA+W transmitted; SMBus switched to MST/REC mode
18H	SLA+W transmitted; ACK received	Load data byte or	0	0	0	X	Data byte transmitted; ACK received
		No SM0DAT action	1	0	0	X	Repeat START transmitted
			0	1	0	X	STOP condition transmitted STO flag reset
			1	1	0	X	STOP condition followed by START condition transmitted; STO flag reset

Table 19: Master Transmitter Mode (Continued) (2 of 2)

Status Code (SM0STA)	SMBus1 Hardware Status	Application Software Response					SMBus Hardware - Next Action
		To/From SM0DAT	To SM0CON				
			STA	STO	SI	AA	
20H	SLA+W transmitted; NOT ACK received	Load data byte or	0	0	0	X	Data byte transmitted; ACK bit received
		No SM0DAT action	1	0	0	X	Repeat START transmitted
			0	1	0	X	STOP condition transmitted; STO flag reset
			1	1	0	X	STOP condition followed by START condition transmitted; STO flag reset
28H	Data byte in SM0DAT transmitted; ACK received	Load data byte or	0	0	0	X	Data byte transmitted; ACK bit received
		No SM0DAT action	1	0	0	X	Repeat START transmitted
			0	1	0	X	STOP condition transmitted; STO flag reset
			1	1	0	X	STOP condition followed by START condition transmitted; STO flag reset
30H	Data byte in SM0DAT transmitted; NOT ACK received	Load data byte or	0	0	0	X	Data byte transmitted; ACK bit received
		No SM0DAT action	1	0	0	X	Repeat START transmitted
			0	1	0	X	STOP condition transmitted; STO flag reset
			1	1	0	X	STOP condition followed by START condition transmitted; STO flag reset
38H	Arbitration lost in SLA+RW or data bytes	No SM0DAT action	0	0	0	X	SMBus released; non-addressed slave entered
			1	0	0	X	A START condition is transmitted once the bus is free

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Table 20: Master Receiver Mode

Status Code (SM0STA)	SMBus Hardware Status	Application Software Response					SMBus Hardware - Next Action
		To/From SM0DAT	To SM0CON				
			STA	STO	SI	AA	
08H	START condition transmitted	Load SLA+W	X	0	0	X	SLA+W transmitted; ACK bit received
10H	Repeat START transmitted	Load SLA+W or	X	0	0	X	SLA+W transmitted; ACK bit received
		Load SLA+R	X	0	0	X	SLA+W transmitted; SMBus switched to MST/TRX mode
38H	Arbitration lost in NOT ACK bit	No SM0DAT action	0	0	0	X	SMBus released; SMBus enters slave mode
			1	0	0	X	A START condition is transmitted once the bus is free
40H	SLA+R transmitted; ACK received	No SM0DAT action	0	0	0	0	Data byte received; NOT ACK bit returned
			0	0	0	1	Data byte received; ACK bit returned
48H	SLA+R transmitted; NOT ACK received	No SM0DAT action	1	0	0	X	Repeat START transmitted
			0	1	0	X	STOP condition transmitted; STO flag reset
			1	1	0	X	STOP condition followed by START condition transmitted; STO flag reset
50H	Data byte received; ACK returned	Read data byte	0	0	0	0	Data byte received; NOT ACK bit returned
			0	0	0	1	Data byte received; ACK bit returned
58H	Data byte received; NOT ACK returned	Read data byte	1	0	0	X	Repeat START transmitted
			0	1	0	X	STOP condition transmitted; STO flag reset
			1	0	0	X	STOP condition followed by START condition transmitted; STO flag reset

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Table 21: Slave Receiver Mode (1 of 2)

Status Code (SM0STA)	SMBus Hardware Status	Application Software Response					SMBus Hardware - Next Action
		To/From SM0DAT	To SM0CON				
			STA	STO	SI	AA	
60H	Own SLA+W received; ACK returned	No SM0DAT action	X	0	0	X	Data byte received; NOT ACK bit returned
			X	0	0	1	Data byte received; ACK returned
68H	Arbitration lost in master SLA+R/W; Own SLA+W received, ACK returned	No SM0DAT action	X	0	0	0	Data byte received; NOT ACK bit returned
			X	0	0	1	Data byte received; ACK returned
70H	General call address (00H) received; ACK returned	No SM0DAT action	X	0	0	0	Data byte received; NOT ACK bit returned
			X	0	0	1	Data byte received; ACK returned
78H	Arbitration lost in master SLA+R/W; General call address (00H) received; ACK returned	No SM0DAT action	X	0	0	0	Data byte received; NOT ACK bit returned
			X	0	0	1	Data byte received; ACK returned
80H	Previously SLV addressed: DATA received; ACK returned	Read data byte	X	0	0	0	Data byte received; NOT ACK bit returned
			X	0	0	1	Data byte received; ACK returned
88H	Previously SLV addressed: DATA received; NOT ACK returned	Read data byte	0	0	0	0	Switch to non-addressed SLV mode; own SLA / general call address not recognized
			0	0	0	1	Switch to non-addressed SLV mode; recognizes own SLA; recognizes general call address if SM0ADR.0 = logic ‘1’
			1	0	0	0	Switch to non-addressed SLV mode; own SLA / general call address not recognized A START is transmitted once bus is free
			1	0	0	1	Switch to non-addressed SLV mode; recognizes own SLA; recognizes general call address if SM0ADR.0 = logic ‘1’. A START is transmitted once bus is free
90H	Previously General Call addressed; DATA byte received; ACK returned	Read data byte	X	0	0	0	Data byte received; NOT ACK bit returned
			X	0	0	1	Data byte received; ACK returned

Table 21: Slave Receiver Mode (Continued) (2 of 2)

Status Code (SM0STA)	SMBus Hardware Status	Application Software Response					SMBus Hardware - Next Action
		To/From SM0DAT	To SM0CON				
			STA	STO	SI	AA	
98H	Previously General Call addressed; DATA byte received; ACK returned	Read data byte	0	0	0	0	Switch to non-addressed SLV mode; own SLA / general call address not recognized
			0	0	0	1	Switch to non-addressed SLV mode; recognizes own SLA; recognizes general call address if SM0ADR.0 = logic ‘1’
			1	0	0	0	Switch to non-addressed SLV mode; own SLA / general call address not recognized A START is transmitted once bus is free
			1	0	0	1	Switch to non-addressed SLV mode; recognizes own SLA; recognizes general call address if SM0ADR.0 = logic ‘1’. A START is transmitted once bus is free
A0H	A STOP condition or a START condition received while addressed as SLV/REC or SLV/TRX	No STDAT action	0	0	0	0	Switch to non-addressed SLV mode; own SLA / general call address not recognized
			0	0	0	1	Switch to non-addressed SLV mode; recognizes own SLA; recognizes general call address if SM0ADR.0 = logic ‘1’
			1	0	0	0	Switch to non-addressed SLV mode; own SLA / general call address not recognized A START is transmitted once bus is free
			1	0	0	1	Switch to non-addressed SLV mode; recognizes own SLA; recognizes general call address if SM0ADR.0 = logic ‘1’. A START is transmitted once bus is free

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Table 22: Slave Transmitter Mode

Status Code (SM0STA)	SMBus Hardware Status	Application Software Response					SMBus Hardware - Next Action
		To/From SM0DAT	To SM0CON				
			STA	STO	SI	AA	
A8H	Own SLA+R received; ACK returned	Load data byte	X	0	0	0	Last data byte transmitted; ACK received
			X	0	0	1	Data byte transmitted; ACK received
B0H	Arbitration lost in master SLA+R/W; Own SLA+R received, ACK returned	Load data byte	X	0	0	0	Last data byte transmitted; ACK received
			X	0	0	1	Data byte transmitted; ACK received
B8H	SM0DAT data byte transmitted; ACK received	Load data byte	X	0	0	0	Last data byte transmitted; ACK received
			X	0	0	1	Data byte transmitted; ACK received
C0H	SM0DAT data byte transmitted; NOT ACK received	No SM0DAT action	0	0	0	0	Switch to non-addressed SLV mode; own SLA / general call address not recognized
			0	0	0	1	Switch to non-addressed SLV mode; recognizes own SLA; recognizes general call address if SM0ADR.0 = logic ‘1’
			1	0	0	0	Switch to non-addressed SLV mode; own SLA / general call address not recognized. A START is transmitted once bus is free
			1	0	0	1	Switch to non-addressed SLV mode; recognizes own SLA; recognizes general call address if SM0ADR.0 = logic ‘1’. A START is transmitted once bus is free
C8H	SLA+R transmitted; NOT ACK received	No SM0DAT action	0	0	0	0	Switch to non-addressed SLV mode; own SLA / general call address not recognized
			0	0	0	1	Switch to non-addressed SLV mode; recognizes own SLA; recognizes general call address if SM0ADR.0 = logic ‘1’
			1	0	0	0	Switch to non-addressed SLV mode; own SLA / general call address not recognized A START is transmitted once bus is free
			1	0	0	1	Switch to non-addressed SLV mode; recognizes own SLA; recognizes general call address if SM0ADR.0 = logic ‘1’. A START is transmitted once bus is free

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Table 23: Miscellaneous Status

Status Code (SM0STA)	SMBus Hardware Status	Application Software Response					SMBus Hardware - Next Action
		To/From SM0DAT	To SM0CON				
			STA	STO	SI	AA	
F8H	No available state information; SI = '0'	No SM0DAT action	No SM0CON action				Wait or proceed with current transfer
00H	Bus error during MST or selected Slave modes caused by illegal START or STOP; or SMBus entered an undefined state	No SM0DAT action	0	1	0	X	Only internal hardware is affected in the SMT or addressed SLV modes. In all cases, the bus is released and SMBus is switched to the not addressed SLV mode. STO is reset.
D0H	SCL high timeout	No SM0DAT action	X	X	0	X	SI flag is cleared. The next work continues.

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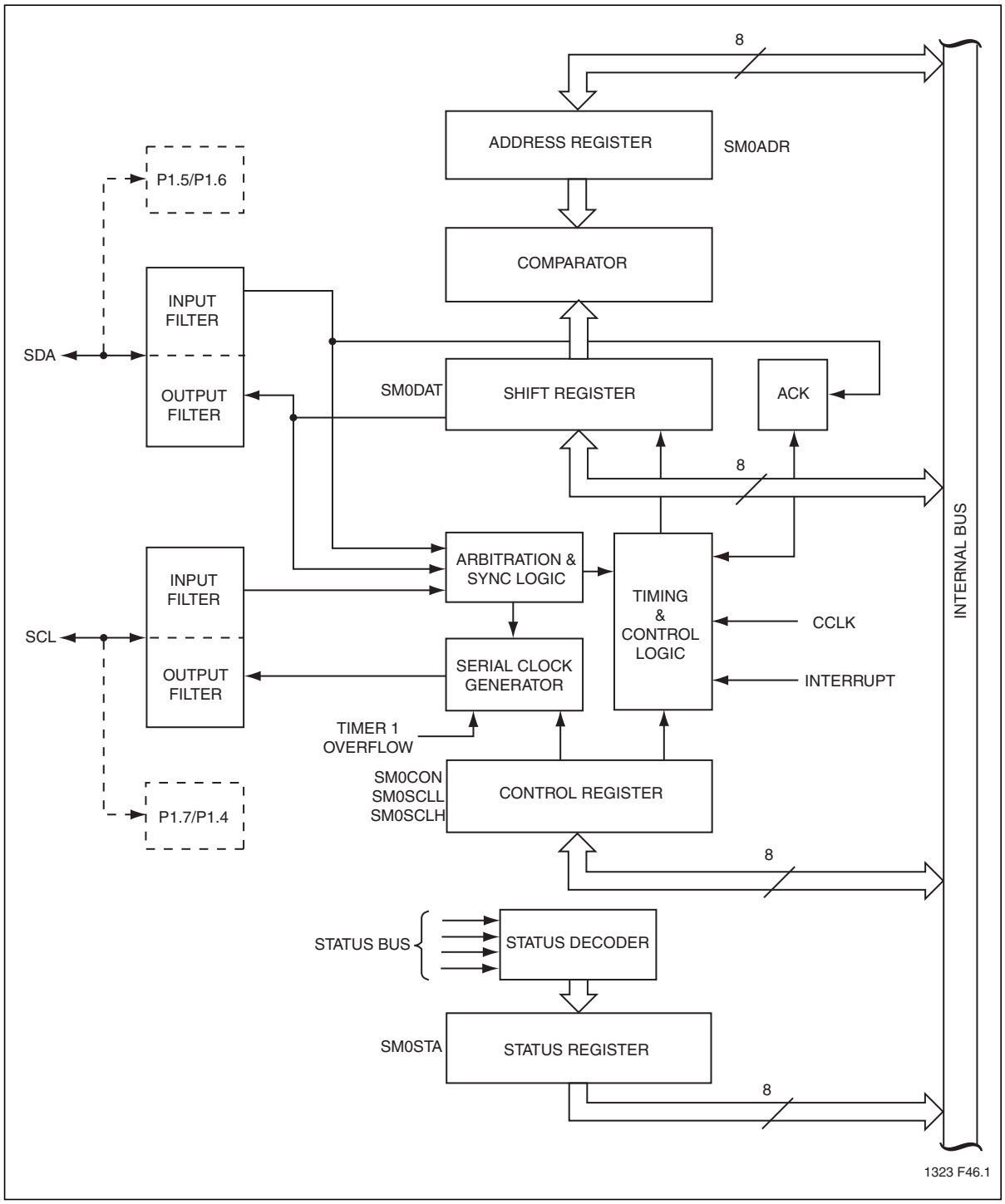

Figure 22: SMBus Serial Interface Block Diagram

SMBus SCL High and Low Duty

SM0SCLH sets the SCL high duration and SM0SCLL sets the SCL low duration. The SM0SCLH and SM0SCLL registers must be set to select the bit rate when the internal clock source for the SMBUS SCL is selected. To select the internal serial clock source for the SM0CLL, set CRSEL = '0' in the SM0CON0 register.

Bit Rate = F_{PCLK} / (4 x (SM0SCLH + SM0SCLL))

The registers can be set to different duty cycles for the SCL. While the values for the SM0SCLH and SM0SCLL registers can be different, the value of the registers must keep the data rate in a data rate range of 0-400 kHz, and ensure that the SCL high period is no less than 600ns and the low period is no less than 1000ns. The values for both SM0SCLH and SM0SCLL should be at least three.

TIMER1 is used as the bit rate clock source when SRSEL is set. To generate the periodic pulse signal that the SMBus uses to generate the bit rate clock, configure TIMER1 to mode 2. When TIMER1 is used, the bit rate is calculated as:

Bit Rate = F_{PCLK} / (96x (256 - TH1))

TH1 and TL1 are the high and low bytes counters for TIMER1. In mode 2, when TL1 counts to 0xFF, the value of TH1 is automatically reloaded into TL1.

Table 24: Bit Rate Configuration[1]

SM0SCLH[2] / SM0SCLL[3]	CRSEL	Bit Rate[4] (Kbit/s) at F_{PCLK}			
		6MHz	12MHz	33MHz	40MHz
6		250	-	-	-
8	0	188	375	-	-
15	0	100	200	-	-
25	0	60	120	330	400
40	0	38	75	197	250
50	0	30	60	165	200
100	0	15	30	83	100
150	0	10	20	55	67
200	0	8	15	42	50
250	0	6	12	33	40
300	0	5	10	28	34
400	0	4	8	21	25
510	0	3	6	16	20
Bit Rate (TIMER1[5] in mode2)		0.25-63Kbps	0.49-125Kbps	1.34-172Kbps	1.63-208Kbps

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1. SCL Bus Rise transition time (T_r) must be less than 300 ns.
2. SM0SCLH minimum value is 1400 ns/(4*CYCSYSCLK), but cannot be less than 3.
3. SM0SCLL minimum value is 1100 ns/(4*CYCSYSCLK), but cannot be less than 3.
4. Baud rate setting must not exceed 400 Kbit per second.
5. If using TIMER1 as the baud rate clock source, TH1 must be 0-254 if the system clock is higher than 20 MHz. If the system clock is lower than or equal to 20 MHz, TH1 can only be 0-255.

Watchdog timer

The programmable Watchdog Timer (WDT) is for fail safe protection against software deadlock and for automatic recovery.

The Watchdog timer is utilized as a watchdog or a timer. To use the Watchdog timer as a watchdog, set WDRE (WDTC[3]) to '1'. To use the Watchdog timer as a timer only, set WDRE to '0' so timer overflows generate an interrupt. Set EWD (IEA[6]) to '1' to enable the interrupt.

Watchdog Timer Mode

To protect the system against software deadlock, WDT (WDTC[1]) should be refreshed within a user-defined time period. Without a periodic refresh, an internal hardware reset will initiate when WDRE (WDTC[3]) = 1). Only a power-on reset clears the WDRE bit.

Any Write to WDTC must be preceded by a correct feed sequence. If WDTON (WDTC[6])=0, the start or stop of the watchdog is controlled by SWDT (WDTC[0]). If WDTON = 1, the watchdog starts regardless of SWDT and cannot be stopped until overflowed.

The upper 8 bits of the time base register (WDTD) is used as the reload register of the counter. When WDT (WDTC[1]) is set to '1', the content of WDTD is loaded into the watchdog counter and the prescaler is cleared.

If a watchdog reset occurs, the reset pin will output at least 196 system clocks. The code execution will begin immediately after the reset cycle.

The WDTS flag bit is set by the Watchdog timer overflow and can only be cleared by power-on reset. Users can also clear the WDTS bit by writing '1' to it following a correct feed sequence.

Pure Timer Mode

In Timer mode, the WDTC and WDTD can be written at any time without a feed sequence. Setting or clearing the SWDT bit will start or stop the counter. A timer overflow will set the WDTS bit. Writing '1' to this bit clears it. When an overflow occurs, the content of WDTD is reloaded into the counter and the Watchdog timer immediately begins to count again. If the interrupt is enabled, an interrupt will occur when the timer overflows. The vector address is 053H and it has a nine-level priority by default. A feed sequence is not required in this mode.

Clock Source

The WDT in the device uses the system clock (XTAL1) as its time base, making it a watchdog counter rather than a Watchdog timer. The WDT register will increment every 344,064 crystal clocks. The upper 8-bits of the time base register (WDTD) are used as the reload register of the WDT.

Figure 23 provides a block diagram of the WDT. Two SFRs (WDTC and WDTD) control Watchdog timer operation.

The time-out period of the WDT is calculated as follows:

Period = (255 - WDTD) * 344064 * $1/f_{CLK\ (XTAL1)}$

where WDTD is the value loaded into the WDTD register and f_{OSC} is the oscillator frequency.

Feed Sequence

In Watchdog mode (WDRE=1), a feed sequence is needed to write into the WDTC register.

The correct feed sequence is:

1. write FDH to SFIS1,
2. write 2AH to SFIS0, then
3. write to the WDTC register

An incorrect second or third instruction of the feed sequence causes an immediate reset in Watchdog mode.

In Timer mode, the WDTC and WDTD can be written at any time. A feed sequence is not required.

Power Saving Considerations for Using the Watchdog Timer

During Idle mode, the Watchdog timer will remain active. The device should be awakened and the Watchdog timer refreshed periodically before expiration. During Power-down mode, the Watchdog timer is stopped. When the Watchdog timer is used as a pure timer, users can turn off the clock to save power. See “Power Management Control Register (PMC)” on page 24.

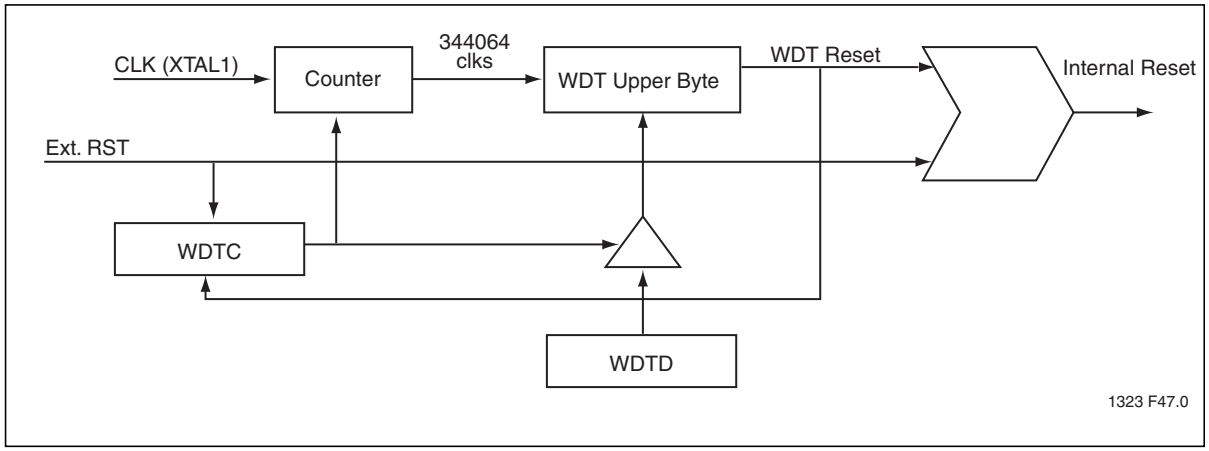

Figure 23: Block Diagram of Programmable Watchdog Timer

Security Lock

The security lock protects against software piracy and prevents the contents of the flash from being read by unauthorized parties. It also protects against code corruption resulting from accidental erasing and programming to the internal flash memory. There are two different types of security locks in the device security lock system: Chip-Level Security Lock and Page-Level Security Lock.

Chip-Level Security Lock

There are four types of chip-level security locks.

1. Disable External MOVC instruction
2. Disable External Host Mode (Except Read Chip ID and Chip-Erase commands)
3. Disable Boot from External Memory
4. Disable External IAP commands (Except Chip-Erase commands)

Users can turn on these security locks in any combination to achieve the security protection scheme. To unlock security locks, the Chip-Erase command must be used.

Disable External MOVC instruction

When Disable-Extern-MOVC command is executed either by External Host Mode command or IAP Mode Command, MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory.

Disable External Host Mode

When Disable-Extern-Host-Cmd command is executed either by External Host Mode Command or IAP Mode Command, all external host mode commands are disabled except Chip-Erase command and Read-ID command.

Upon activation of this option, the device can not be accessed through external host mode. User can not verify and copy the contents of the internal flash

Disable Boot From External Memory

When Disable-Extern-Boot command is executed either by External Host Mode Command or IAP Mode Command, the EA pin value will be ignored during chip Reset and always boot from the internal memory.

Disable External IAP Commands

When Disable-Extern-IAP command is executed either by External Host Mode Command or IAP Mode Command, all IAP commands executed from external memory are disabled except Chip-Erase command. All IAP commands executed from internal memory are allowed if the Page Lock is not set.

Page-Level Security Lock

When any of Secure-Page0, Secure-Page1, Secure-Page2, Secure-Page3, or Secure-Page4 command is executed, the individual page (Page0, Page1, Page2, Page3, or Page4) will enter secured mode. No part of the page can be verified by either External Host mode commands or IAP commands. MOVC instructions are also unable to read any data from the page.

To unlock the security locks on Page0-3 of the primary partition (Partition0), the Partition0-Erase command must be used. To unlock the security lock on Page4, the Chip-Erase command must be used.

Read Operation Under Lock Condition

The following three cases can be used to indicate the Read operation is targeting a locked, secured memory area:

1. External host mode: Read-back = 55H (locked)
2. IAP command: Read-back = previous SFDT data
3. MOVC: Read-back = 00H (blank)

Reset

A system reset initializes the MCU and begins program execution at program memory location 0000H or the boot vector address. The reset input for the device is the RST pin. In order to reset the device, a logic level high must be applied to the RST pin for at least two machine cycles (24 clocks), after the oscillator becomes stable. ALE and PSEN# are weakly pulled high during reset. During reset, ALE and PSEN# output a high level in order to perform a proper reset. This level must not be affected by external element. A system reset will not affect the 512 Bytes of on-chip RAM while the device is running, however, the contents of the on-chip RAM during power up are indeterminate. Following reset, all Special Function Registers (SFR) return to their reset values outlined in Tables 4 to 8.

Power-on Reset

At initial power up, the port pins will be in a random state until the oscillator has started and the internal reset algorithm has weakly pulled all pins high.

When power is applied to the device, the RST pin must be held high long enough for the oscillator to start up (usually several milliseconds for a low frequency crystal), in addition to two machine cycles for a valid power-on reset. An example of a method to extend the RST signal is to implement a RC circuit by connecting the RST pin to V_{DD} through a 10 µF capacitor and to V_{SS} through an 8.2KΩ resistor as shown in Figure 24. Note that if an RC circuit is being used, provisions should be made to ensure the V_{DD} rise time does not exceed 1 millisecond and the oscillator start-up time does not exceed 10 milliseconds.

For a low frequency oscillator with slow start-up time the reset signal must be extended in order to account for the slow start-up time. This method maintains the necessary relationship between V_{DD} and RST to avoid programming at an indeterminate location. The POF flag in the PCON register is set to indicate an initial power up condition. The POF flag will remain active until cleared by software. Please refer to Section 3.5, PCON register definition, for detailed information.

For more information on system level design techniques, please review the **Design Considerations for the SST FlashFlex Family Microcontroller** application note.

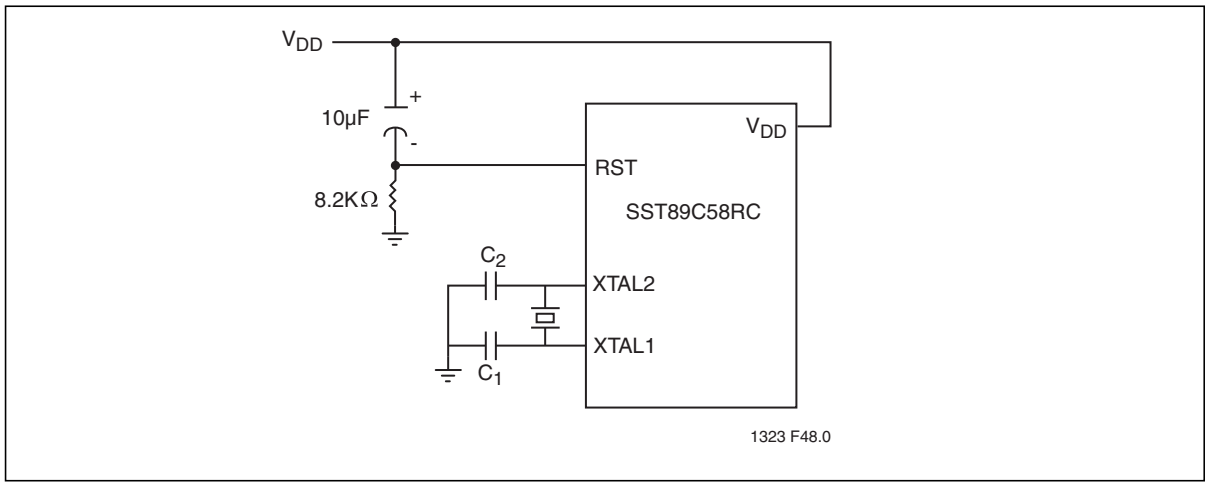

Figure 24: Power-on Reset Circuit

Interrupt Priority and Polling Sequence

The device supports seven interrupt sources under a four level priority scheme. Table 25 and Figure 25 summarize the polling sequence of the supported interrupts.

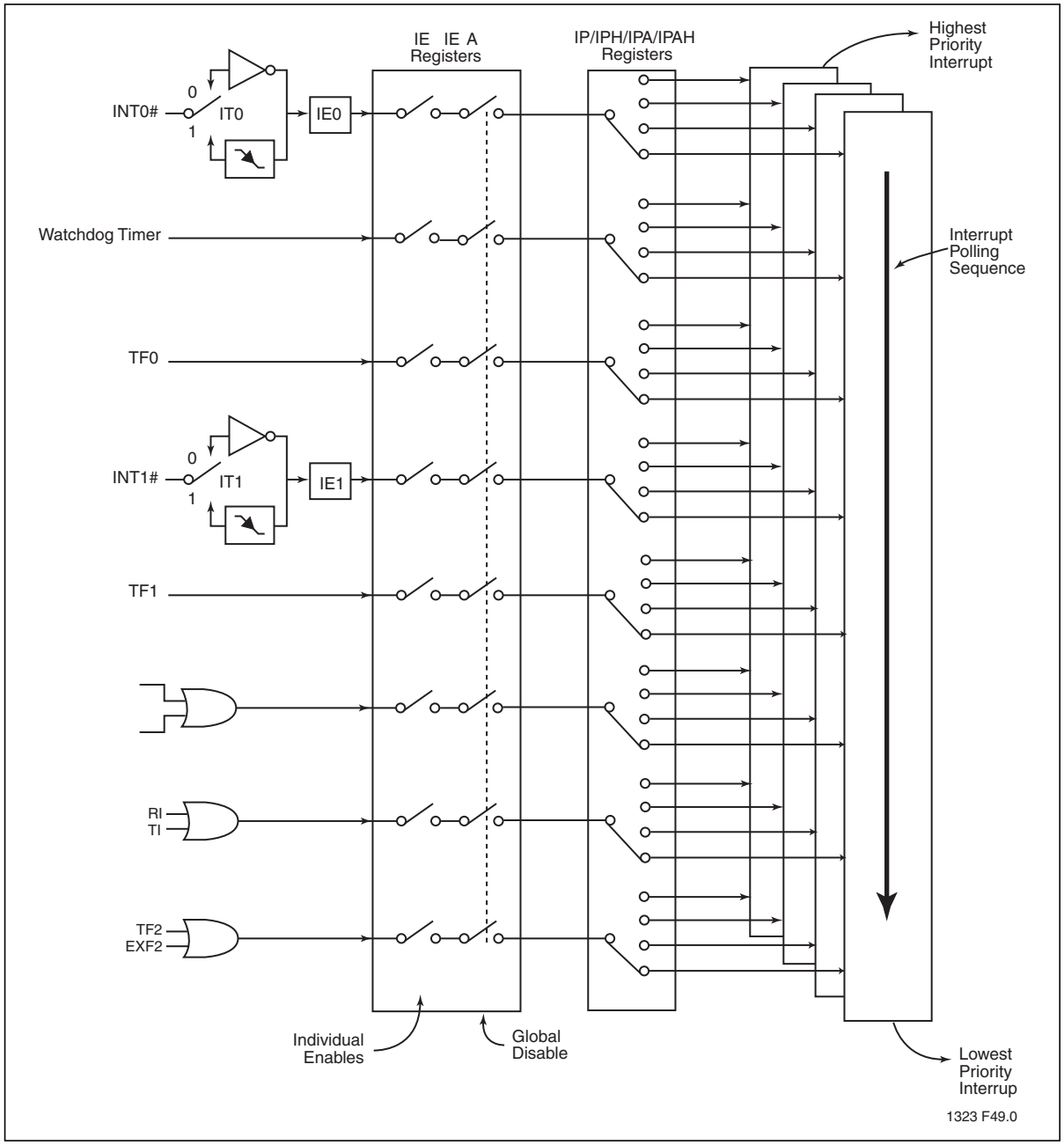

Figure 25: Interrupt Sequence

Table 25: Interrupt Table

Description	Interrupt Flag	Vector Address	Service Priority	Wake-Up Power-down
Ext. Int0	IE0	0003H	1(highest)	yes
SMBus0	-	002BH	2	yes
T0	TF0	000BH	3	no
Ext. Int1	IE1	0013H	4	yes
T1	TF1	001BH	5	no
UART	TI/RI	0023H	6	no
T2	TF2, EXF2	003BH	7	no
SMBus1	-	0043H	8	yes
Watchdog	-	0053H	9	no

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Power-Saving Modes

The device provides two power saving modes of operation for applications where power consumption is critical. The two modes are idle and power-down, see Table 26.

Idle Mode

Idle mode is entered setting the IDL bit in the PCON register. In idle mode, the program counter (PC) is stopped. The system clock continues to run and all interrupts and peripherals remain active. The on-chip RAM and the special function registers hold their data during this mode.

The device exits idle mode through either a system interrupt or a hardware reset. Exiting idle mode via system interrupt, the start of the interrupt clears the IDL bit and exits idle mode. After exit the Interrupt Service Routine, the interrupted program resumes execution beginning at the instruction immediately following the instruction which invoked the idle mode. A hardware reset starts the device similar to a power-on reset.

Power-down Mode

The power-down mode is entered by setting the PD bit in the PCON register. In the power-down mode, the clock is stopped and external interrupts are active for level sensitive interrupts only. SRAM contents are retained during power-down, the minimum V_{DD} level is 2.0V.

The device exits power-down mode through either an enabled external level sensitive interrupt or a hardware reset. The start of the interrupt clears the PD bit and exits power-down. Holding the external interrupt pin low restarts the oscillator, the signal must hold low at least 1024 clock cycles before bringing back high to complete the exit. Upon interrupt signal restored to logic $V_{IH,}$ the interrupt service routine program execution resumes beginning at the instruction immediately following the instruction which invoked power-down mode. A hardware reset starts the device similar to power-on reset.

To exit properly out of power-down, the reset or external interrupt should not be executed before the V_{DD} line is restored to its normal operating voltage. Be sure to hold V_{DD} voltage long enough at its normal operating level for the oscillator to restart and stabilize (normally less than 20 ms).

When the MCU is in power-down mode, a falling edge on the SDA pin of the SMBUS will wakeup the MCU. Because the first byte may not be received by the SMBus correctly, the first START condition may be missed because the oscillators will not start up.

Table 26: Power Saving Modes

Mode	Initiated by	State of MCU	Exited by
Idle	Software (Set IDL bit in PCON) MOV PCON, #01H;	• CLK is running. • Interrupts, serial port and timers/counters are active. • Program Counter is stopped. • ALE and PSEN# signals at a HIGH level during Idle. • All registers remain unchanged.	Enabled interrupt or hardware reset. Start of interrupt clears IDL bit and exits idle mode, after the ISR RETI instruction, program resumes execution beginning at the instruction following the one that invoked idle mode. A user could consider placing two or three NOP instructions after the instruction that invokes idle mode to eliminate any problems. A hardware reset restarts the device similar to a power-on reset.
Power-down	Software (Set PD bit in PCON) MOV PCON, #02H;	• CLK is stopped. • On-chip SRAM and SFR data is maintained. • ALE and PSEN# signals at a LOW level during power - down. • External Interrupts are only active for level sensitive interrupts, if enabled.	Enabled external level sensitive interrupt or hardware reset. Start of interrupt clears PD bit and exits power-down mode, after the ISR RETI instruction program resumes execution beginning at the instruction following the one that invoked power-down mode. A user could consider placing two or three NOP instructions after the instruction that invokes power-down mode to eliminate any problems. A hardware reset restarts the device similar to a power-on reset.

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System Clock and Clock Options

Clock Input Options and Recommended Capacitor Values for Oscillator

Shown in Figure 26 are the input and output of an internal inverting amplifier (XTAL1, XTAL2), which can be configured for use as an on-chip oscillator.

When driving the device from an external clock source, XTAL2 should be left disconnected and XTAL1 should be driven.

At start-up, the external oscillator may encounter a higher capacitive load at XTAL1 due to interaction between the amplifier and its feedback capacitance. However, the capacitance will not exceed 15 pF once the external signal meets the V_{IL} and V_{IH} specifications.

Crystal manufacturer, supply voltage, and other factors may cause circuit performance to differ from one application to another. C1 and C2 should be adjusted appropriately for each design. Table 27, shows the typical values for C1 and C2 vs. crystal type for various frequencies

Table 27: Recommended Values for C1 and C2 by Crystal Type

Crystal	C1 = C2
Quartz	20-30pF
Ceramic	40-50pF

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More specific information about on-chip oscillator design can be found in the **FlashFlex Oscillator Circuit Design Considerations** application note.

Clock Doubling Option

By default, the device runs at 12 clocks per machine cycle (x1 mode). The device has a clock doubling option to speed up to 6 clocks per machine cycle. Please refer to Table 28 for detail.

Clock double mode can be enabled either via the external host mode or the IAP mode. Please refer to Table 12 for the IAP mode enabling command (When cleared, the Enable-Clock-Double bit in the SFST register will indicate 6-clock mode.).

The clock double mode is only for doubling the internal system clock and the internal flash memory, i.e. EA#=1. To access the external memory and the peripheral devices, careful consideration must be taken. Also note that the crystal output (XTAL2) will not be doubled.

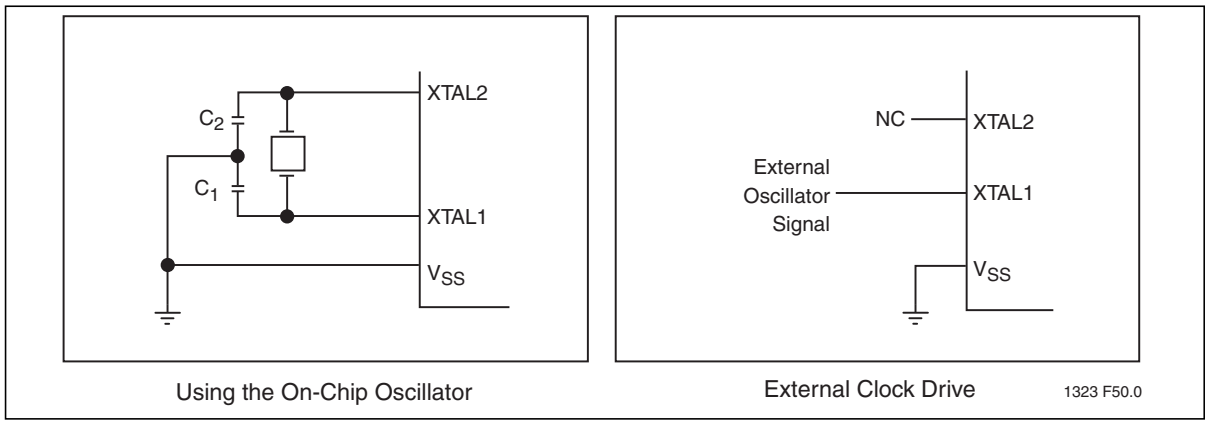

Figure 26: Oscillator Characteristics

Table 28: Clock Doubling Features

Device	Standard Mode (x1)		Clock Double Mode (x2)	
	Clocks per Machine Cycle	Max. External Clock Frequency (MHz)	Clocks per Machine Cycle	Max. External Clock Frequency (MHz)
SST89C58RC	12	40	6	20

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Electrical Specification

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Ambient Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature. . . . . -65°C to +150°C
Voltage on EA# Pin to V_{SS}. . . . . -0.5V to +14.0V
D.C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20ns) on Any Other Pin to V_{SS} . . . . . -1.0V to V_{DD}+1.0V
Maximum I_{OL} per I/O Pins P1.4, P1.5, P1.6, P1.7. . . . . 20mA
Maximum I_{OL} per I/O for All Other Pins 15mA
Package Power Dissipation Capability (T_A = 25°C). 1.5W
Through Hole Lead Soldering Temperature (10 Seconds) . . . . . 300°C
Surface Mount Solder Reflow Temperature[1]. . . . . 260°C for 10 seconds
Output Short Circuit Current[2] . . . . . 50 mA

1. Excluding certain with-Pb 32-PLCC units, all packages are 260°C capable in both non-Pb and with-Pb solder versions. Certain with-Pb 32-PLCC package types are capable of 240°C for 10 seconds; please consult the factory for the latest information.
2. Outputs shorted for no more than one second. No more than one output shorted at a time. (Based on package heat transfer limitations, not device power consumption.

Note: This specification contains preliminary information on new products in production. The specifications are subject to change without notice.

Table 29: Operating Range

Symbol	Description	Min.	Max	Unit
T_A	Ambient Temperature Under Bias			
	Standard	0	+70	°C
	Industrial	-40	+85	°C
V_{DD}	Supply Voltage			
	SST89C58RC	2.7	5.5	V
F_{OSC}	Oscillator Frequency			
	SST89C58RC	0	40	MHz
	Oscillator Frequency for In-Application programming			
	SST89C58RC	25	40	MHz

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Table 30: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 31: AC Conditions of Test[1]

Input Rise/Fall Time	Output Load
10 ns	C_L = 100 pF

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1. See Figures 31 and 33

Table 32: Recommended System Power-up Timings

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	100	µs

T0-0.2 25100

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter

Table 33: Pin Impedance (VDD=3.3V, TA=25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	15 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	12 pF
L_{PIN}[2]	Pin Inductance		20 nH

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. Refer to PCI spec.

DC Electrical Characteristics

Table 34: DC Characteristics for SST89C58RC: T_A = -40°C to +85°C; V_{DD} = 2.7-5.5V; V_{SS} = 0V

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{DD}	Operating Voltage		2.7	5.5	V
V_{IL1}	Input Low Voltage P0, P1, P2, P3, EA#	3.6V<V_{DD}<=5.5V	0	0.8	V
		2.7V<=V_{DD}=3.6V	0	0.6	V
V_{IL2}	Input Low Voltage RST	3.6V<V_{DD}<=5.5V	0	0.8	V
		2.7V<=V_{DD}=3.6V	0	0.6	V
V_{IL3}	Input Low Voltage XTAL	3.6V<V_{DD}<=5.5V	0	0.8	V
		2.7V<=V_{DD}=3.6V	0	0.4	V
V_{IL4}	Input Low Voltage P1.4/SCL1, P1.5/SDA1, P1.6/SDA0, P1.7/SCL0	3.6V<V_{DD}<=5.5V	0	0.3V_{DD}	V
		2.7V<=V_{DD}=3.6V	0	0.3V_{DD}	V
V_{IH1}	Input High Voltage P0, P1, P2, P3, EA#	3.6V<V_{DD}<=5.5V	2.4	V_{DD} + 0.2	V
		2.7V<=V_{DD}=3.6V	2.0	V_{DD} + 0.2	V
V_{IH2}	Input High Voltage RST	3.6V<V_{DD}<=5.5V	2.4	V_{DD} + 0.2	V
		2.7V<=V_{DD}=3.6V	2.0	V_{DD} + 0.2	V
V_{IH3}	Input High Voltage XTAL[1]	3.6V<V_{DD}<=5.5V	2.4	V_{DD} + 0.2	V
		2.7V<=V_{DD}=3.6V	2.0	V_{DD} + 0.2	V
V_{IH4}	Input High Voltage P1.4/SCL1, P1.5/SDA1, P1.6/SDA0, P1.7/SCL0	V_{DD}=5.5V	0.7V_{DD}	5.5	V
		V_{DD}=3.0V	0.7V_{DD}	5.5	V
V_{OL1}	Output Low Voltage	V_{DD}=4.5V, I_{OL}=+4mA	-	0.45	V
		V_{DD}=3V, I_{OL}=+4mA	-	0.4	V
V_{OL2}	Output Low Voltage P0, ALE, PSEN#	V_{DD}=4.5V, I_{OL}=+10mA	-	0.45	V
		V_{DD}=3V, I_{OL}=+6mA	-	0.4	V
V_{OL3}	Output Low Voltage P1.4/SCL1, P1.5/ SDA1, P1.6/SDA0, P1.7/SCL0	I_{OL}=3.0 mA	-	0.4	V
V_{OH1}	Output High Voltage P1, P 2, P3	V_{DD}=4.5V, I_{OH}=-120µA	2.4	-	V
		V_{DD}=3.0V, I_{OH}=-45µA	2.4	-	V
V_{OH2}	Output High Voltage P0, ALE, PSEN#	V_{DD}=4.5V, I_{OH}=-8µA	2.4	-	V
		V_{DD}=3.0V, I_{OH}=-3µA	2.4	-	V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN}=0.4V		-100	µA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)	V_{IN}=2V		-650	µA
I_{LI}	Input Leakage Current (Port 0)	0.45 < V_{IN} < V_{DD}-0.3		±10	µA
I_{DD}	Power Supply Current	Active Mode @ 40MHz		15	mA
		Idle Mode @ 40MHz		6.8	mA
		Power-down Mode (min V= 5V)		100	µA

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1. XTAL2 is not 5-volt tolerant pin

AC Electrical Characteristics

AC Characteristics:

(Over Operating Conditions: Load Capacitance for Port 0, ALE, and PSEN# = 100pF; Load Capacitance for All Other Outputs = 80pF)

Table 35: AC Electrical Characteristics T_A = -40°C to +85°C, 2.7-5.5V@40MHz, V_{SS} = 0V

		Oscillator				
		40 MHz (x1 Mode) 20 MHz (x2 Mode)[1]		Variable		
Symbol	Parameter	Min	Max	Min	Max	Units
$1/T_{CLCL}$	x1 Mode Oscillator Frequency	0	40	0	40	MHz
$1/2T_{CLCL}$	x2 Mode Oscillator Frequency	0	20	0	20	MHz
T_{LHLL}	ALE Pulse Width	35		$2T_{CLCL}$ - 15		ns
T_{AVLL}	Address Valid to ALE Low	10		T_{CLCL} - 15 (5V)		ns
T_{LLAX}	Address Hold After ALE Low	10		T_{CLCL} - 15 (5V)		ns
T_{LLIV}	ALE Low to Valid Instr In		55		$4T_{CLCL}$ - 45 (5V)	ns
T_{LLPL}	ALE Low to PSEN# Low	10		T_{CLCL} - 15 (5V)		ns
T_{PLPH}	PSEN# Pulse Width	60		$3T_{CLCL}$ - 15 (5V)		ns
T_{PLIV}	PSEN# Low to Valid Instr In		25		$3T_{CLCL}$ - 50 (5V)	ns
T_{PXIX}	Input Instr Hold After PSEN#			0		ns
T_{PXIZ}	Input Instr Float After PSEN#		10		T_{CLCL} - 15 (5V)	ns
T_{PXAV}	PSEN# to Address valid	17		T_{CLCL} - 8		ns
T_{AVIV}	Address to Valid Instr In		65		$5T_{CLCL}$ - 60 (5V)	ns
T_{PLAZ}	PSEN# Low to Address Float		10		10	ns
T_{RLRH}	RD# Pulse Width	120		$6T_{CLCL}$ - 30 (5V)		ns
T_{WLWH}	Write Pulse Width (WE#)	120		$6T_{CLCL}$ - 30 (5V)		ns
T_{RLDV}	RD# Low to Valid Data In		75		$5T_{CLCL}$ - 50 (5V)	ns
T_{RHDX}	Data Hold After RD#	0		0		ns
T_{RHDZ}	Data Float After RD#		38		$2T_{CLCL}$ - 12 (5V)	ns
T_{LLDV}	ALE Low to Valid Data In		150		$8T_{CLCL}$ - 50 (5V)	ns
T_{AVDV}	Address to Valid Data In		150		$9T_{CLCL}$ - 75 (5V)	ns
T_{LLWL}	ALE Low to RD# or WR# Low	60	90	$3T_{CLCL}$ - 15 (5V)	$3T_{CLCL}$ + 15 (5V)	ns
T_{AVWL}	Address to RD# or WR# Low	70		$4T_{CLCL}$ - 30 (5V)		ns
T_{QVWX}	Data Valid to WR# High to Low Transition		5	T_{CLCL} - 20		ns
T_{WHQX}	Data Hold After WR#	5		T_{CLCL} - 20 (5V)		ns
T_{QVWH}	Data Valid to WR# High	125		$7T_{CLCL}$ - 50 (5V)		ns
T_{RLAZ}	RD# Low to Address Float		0		0	ns
T_{WHLH}	RD# to WR# High to ALE High	10	40	T_{CLCL} - 15 (5V)	T_{CLCL} + 15 (5V)	ns
T_{OFSB}	SMBUS Output fall time from VIH min to VIL max with a bus capacitance100pf			30 (5V)	250 (5V)	ns

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1. Calculated values are for x1 Mode only

Explanation of Symbols

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW or ALE
P: PSEN#
Q: Output data
R: RD# signal
T: Time
V: Valid
W: WR# signal
X: No longer a valid logic level
Z: High Impedance (Float)

For example:

T_{AVLL} = Time from Address Valid to ALE Low

T_{LLPL} = Time from ALE Low to PSEN# Low

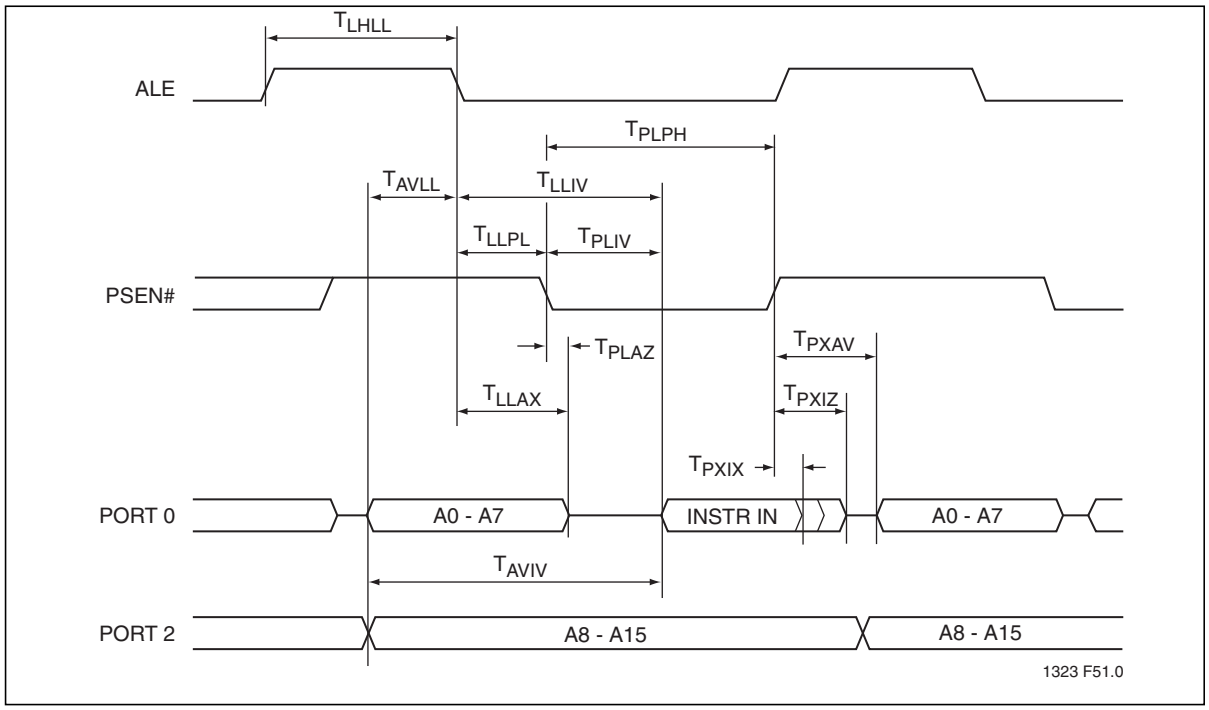

Figure 27: External Program Memory Read Cycle

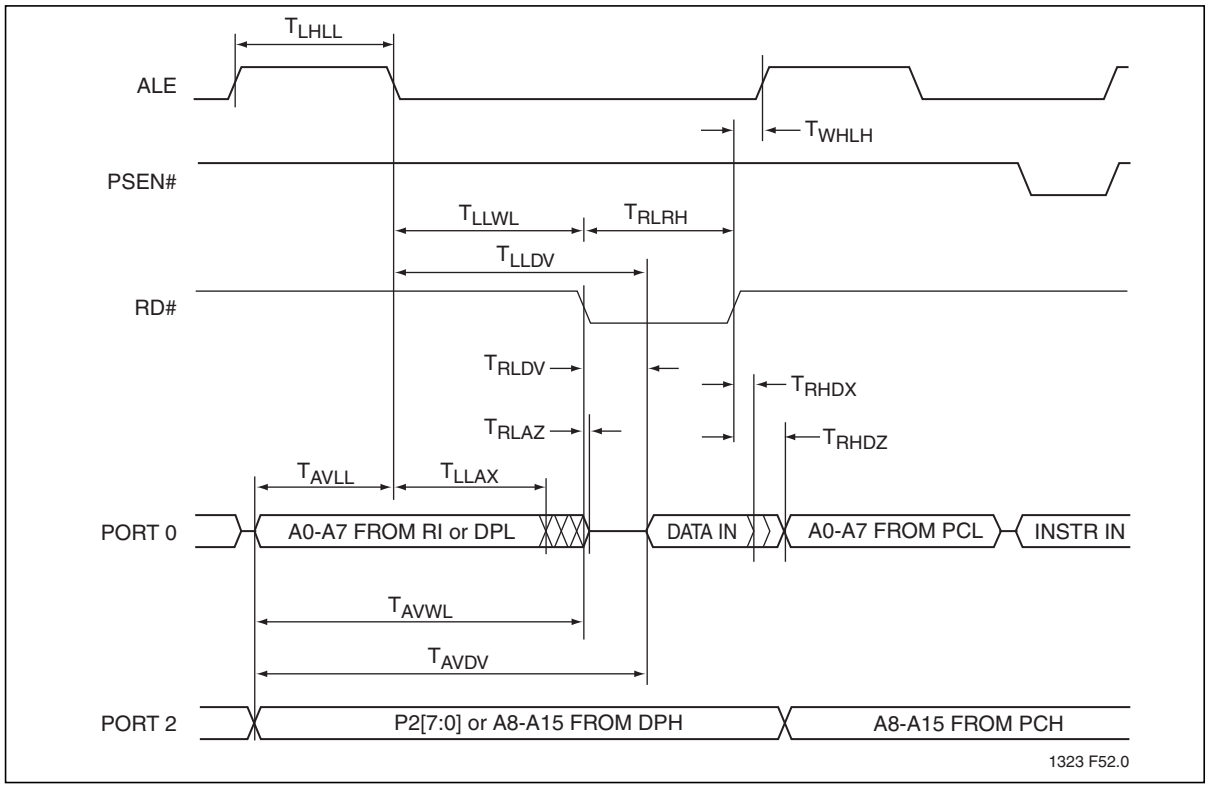

Figure 28: External Data Memory Read Cycle

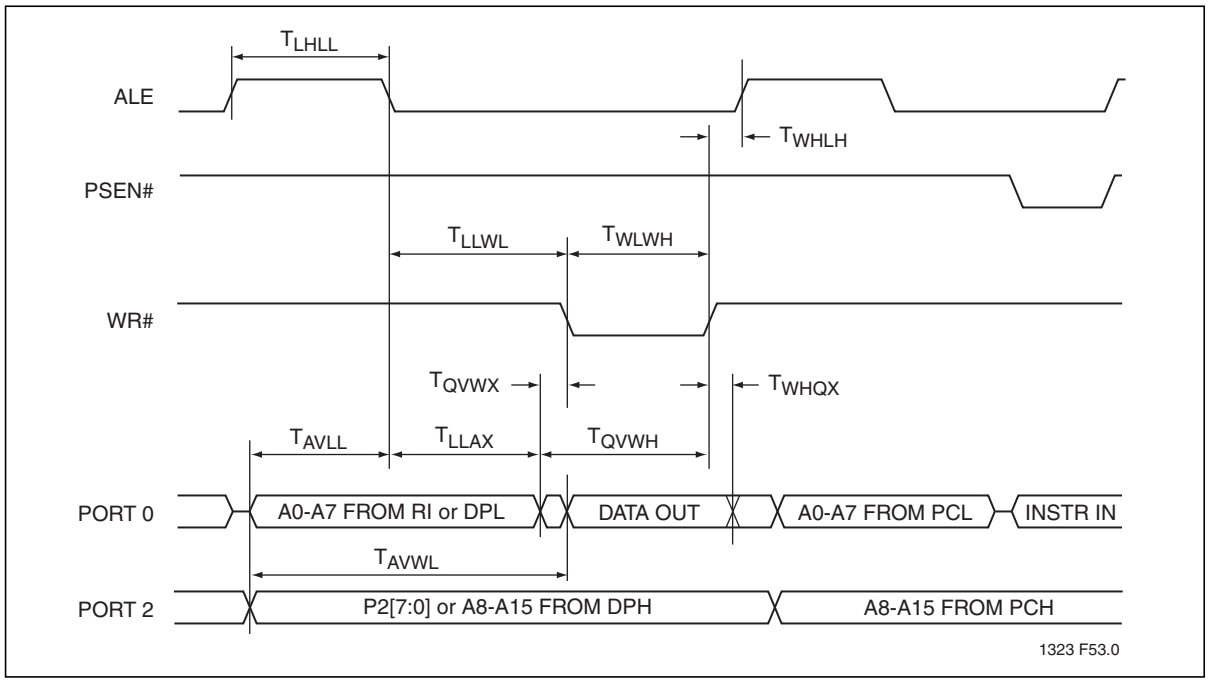

Figure 29: External Data Memory Write Cycle

Table 36: Serial Port Timing

Symbol	Parameter	Oscillator						Units
		12MHz		40MHz		Variable		
		Min	Max	Min	Max	Min	Max	
T_{XLXL}	Serial Port Clock Cycle Time	1.0		0.3		$12T_{CLCL}$		µs
T_{QVXH}	Output Data Setup to Clock Rising Edge	700		117		$10T_{CLCL}$ - 133		ns
T_{XHQX}	Output Data Hold After Clock Rising Edge	50				$2T_{CLCL}$ - 117		ns
				0		$2T_{CLCL}$ - 50		ns
T_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		700		117		$10T_{CLCL}$ - 133	ns

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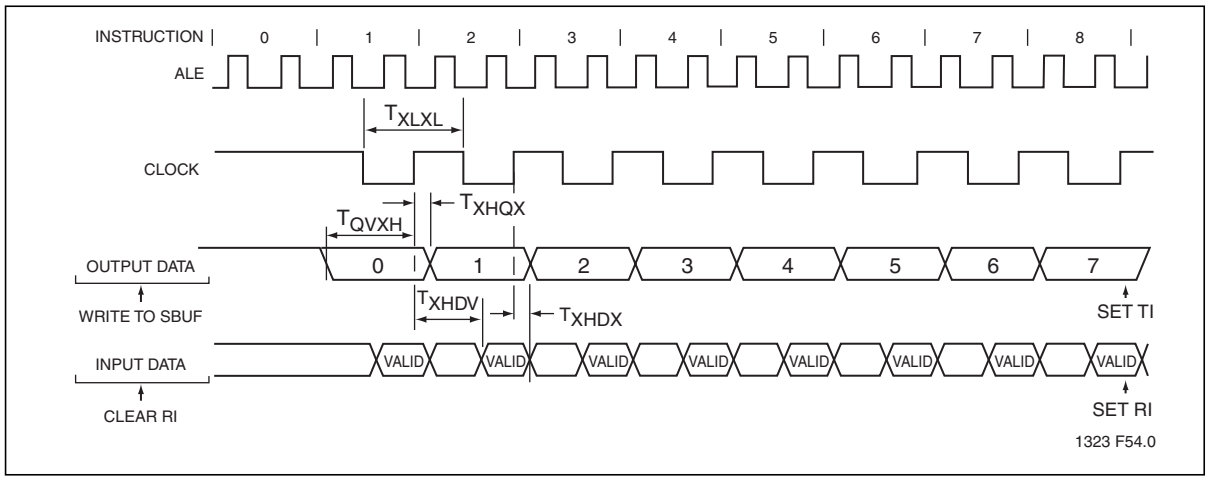

Figure 30: Shift Register Mode Timing Waveforms

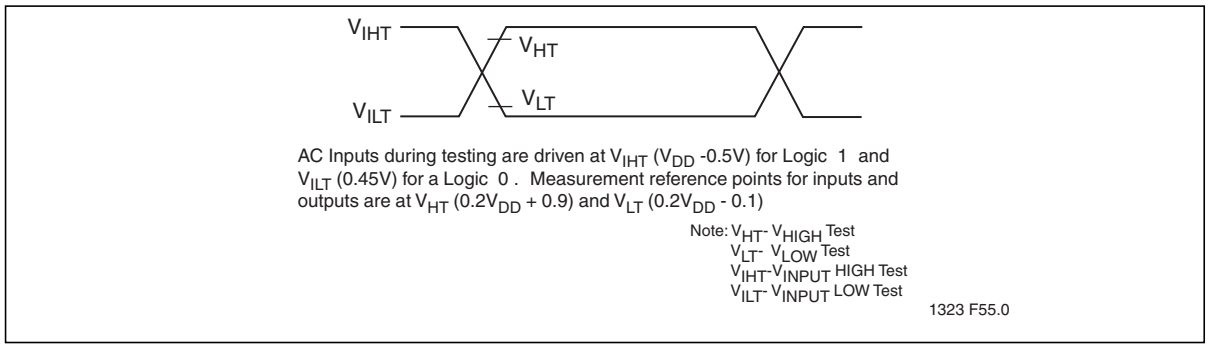

Figure 31: AC Testing Input/Output Test Waveform

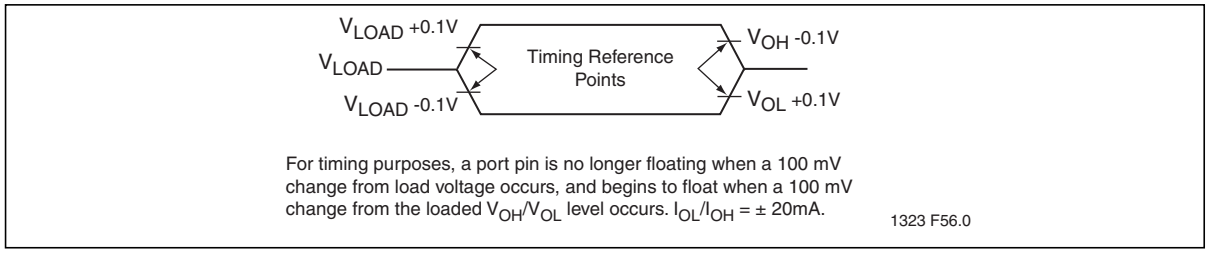

Figure 32: Float Waveform

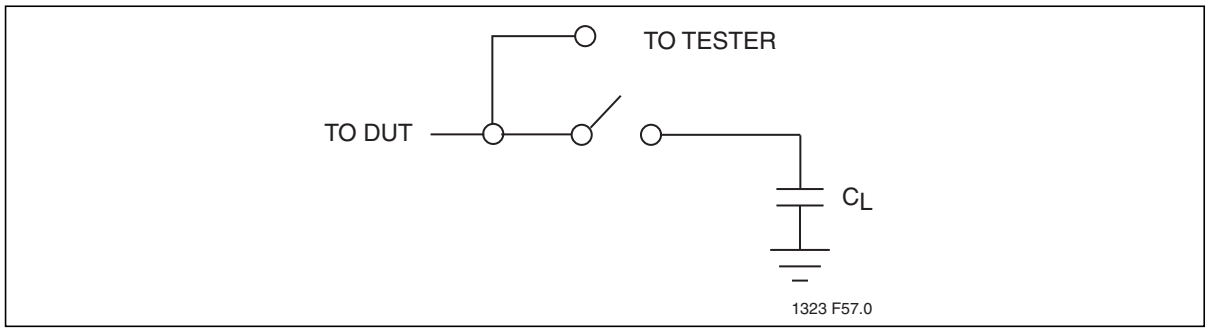

Figure 33: A Test Load Example

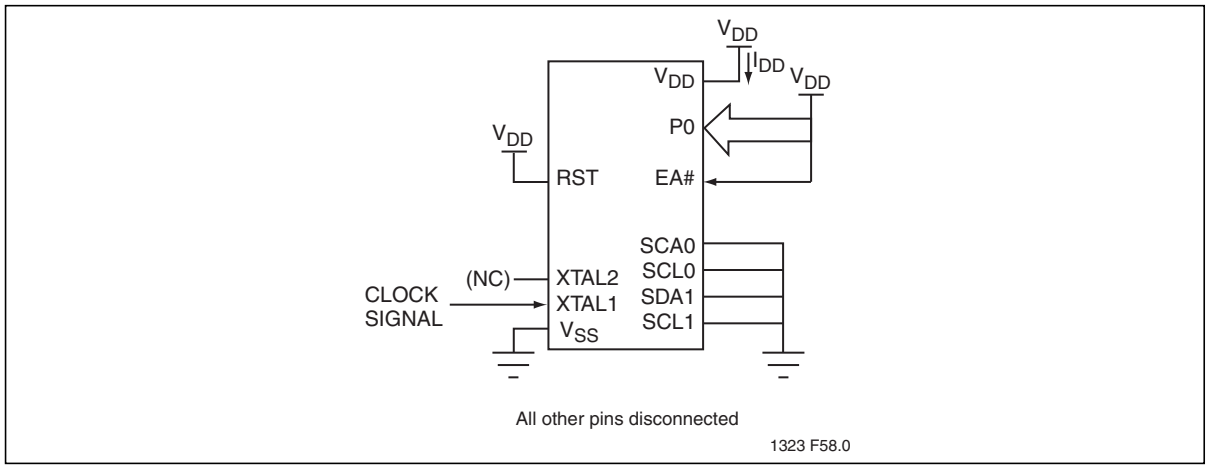

Figure 34: I_{DD} Test Condition, Active Mode

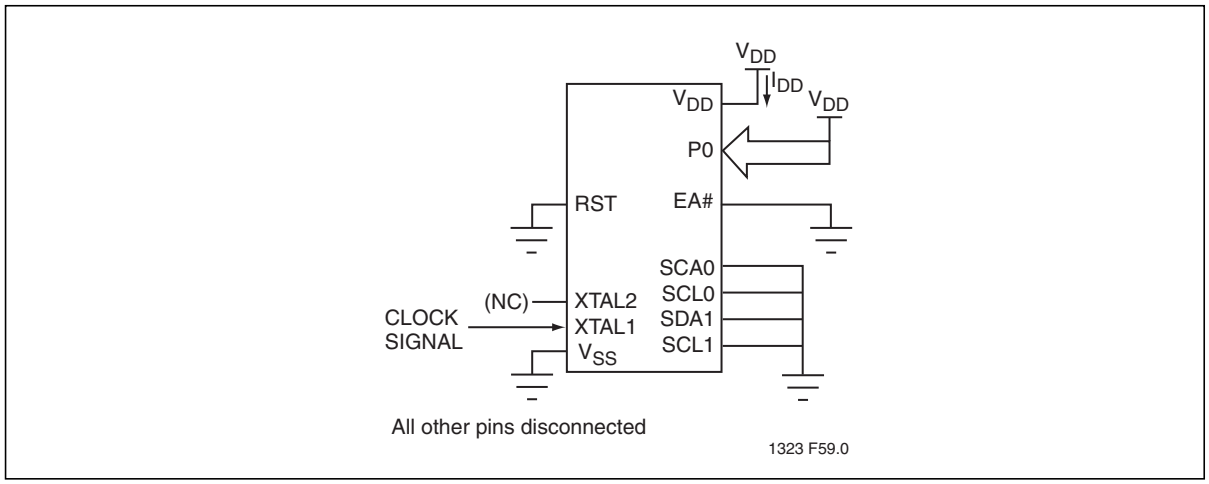

Figure 35: I_{DD} Test Condition, Idle Mode

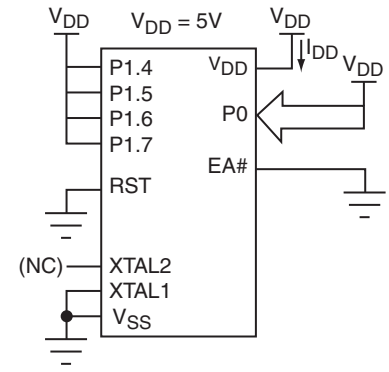

Figure 36: I_{DD} Test Condition, Power-down Mode

Table 37: Flash Memory Programming/Verification Parameters[1]

Parameter[2]	Max	Units
Chip-Erase Time	50	ms
Block-Erase Time	50	ms
Sector-Erase Time	10	ms
Byte-Program Time[3]	80	µs
Re-map or Security bit Program Time	100	µs

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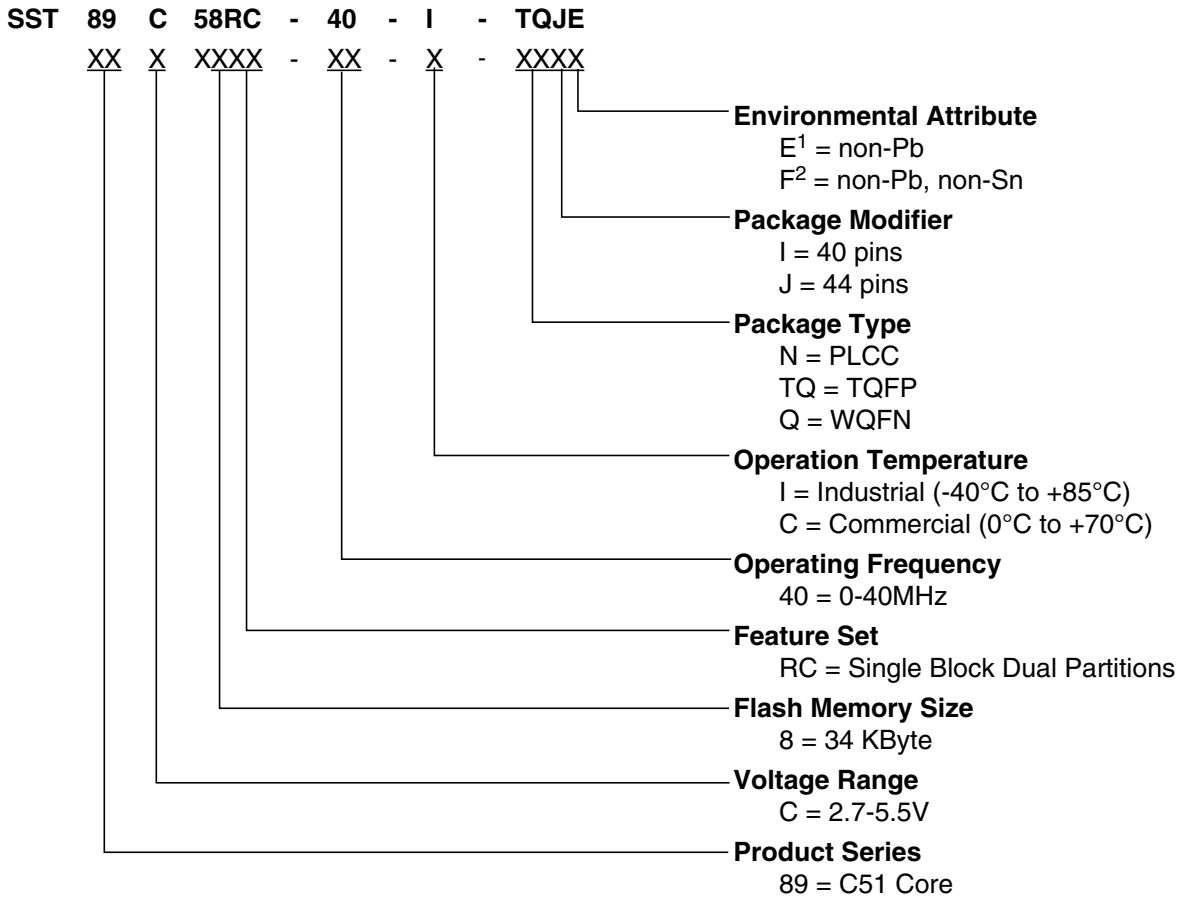
1. For IAP operations, the program execution overhead must be added to the above timing parameters. The Test condition shows as
   follows: TA = -40°C to +85°C, 2.7-5.5V@1MHz, VSS = 0V.
2. Program and Erase times will scale inversely proportional to programming clock frequency.
3. Each byte must be erased before programming.

Product Ordering Information



1. Environmental suffix “E” denotes non-Pb solder. SST non-Pb solder devices are “RoHS Compliant”.
2. Environmental suffix “F” denotes non-Pb/non-SN solder. SST non-Pb/non-Sn solder devices are “RoHS Compliant”.

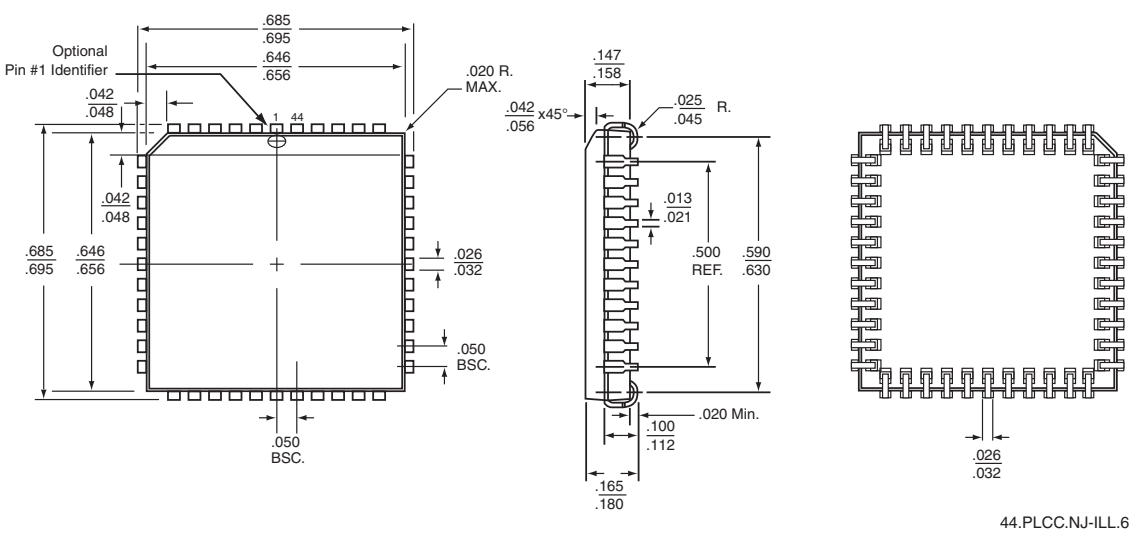
Valid Combinations

Valid combinations for SST89C58RC

SST89C58RC-40-I-NJE SST89C58RC-40-I-TQJE SST89C58RC-40-C-QIF

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Packaging Diagrams



Note:
1. Complies with JEDEC publication 95 MS-018 AC dimensions (except as noted), although some dimensions may be more stringent.
= JEDEC min is .650; SST min is *less*stringent
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
4. Coplanarity: ± 4 mils.

Figure 37: 44-lead Plastic Lead Chip Carrier (PLCC)
SST Package Code: NJ

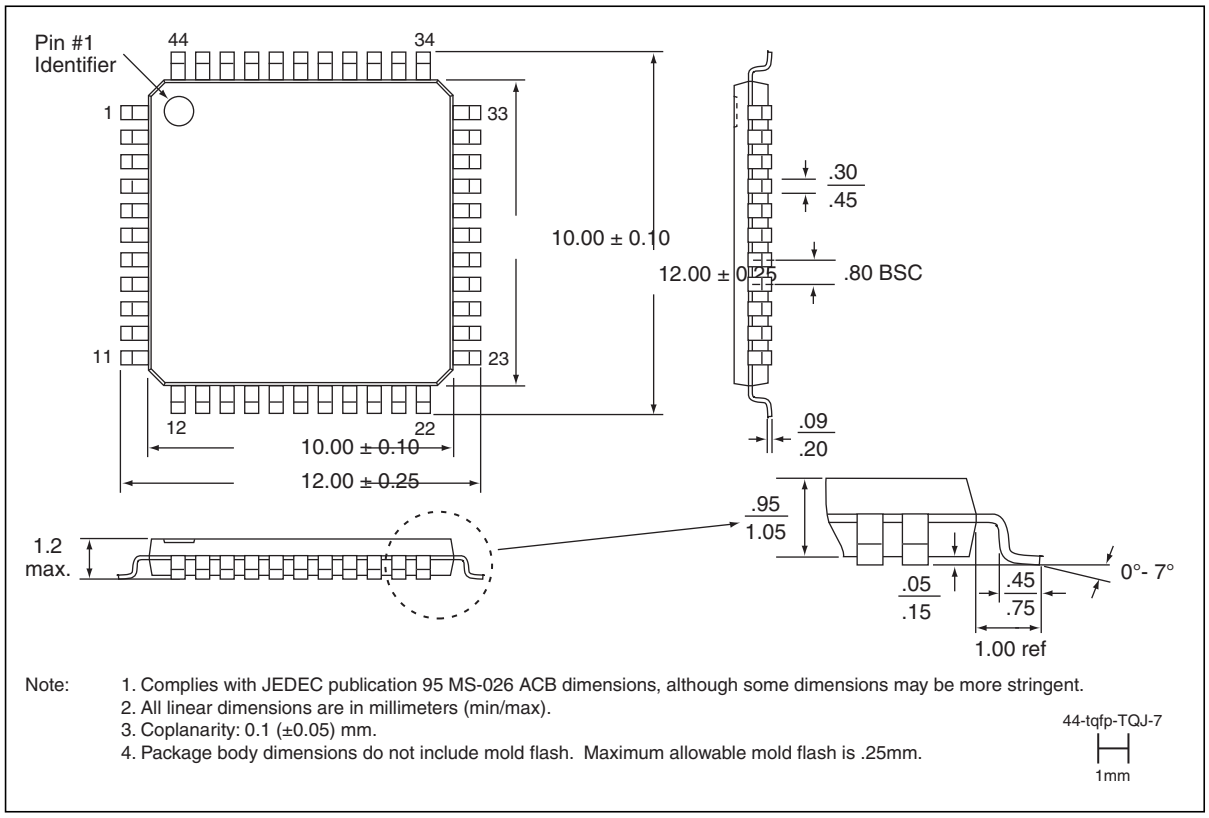


Figure 38: 44-lead Thin Quad Flat Pack (TQFP)
SST Package Code: TQJ

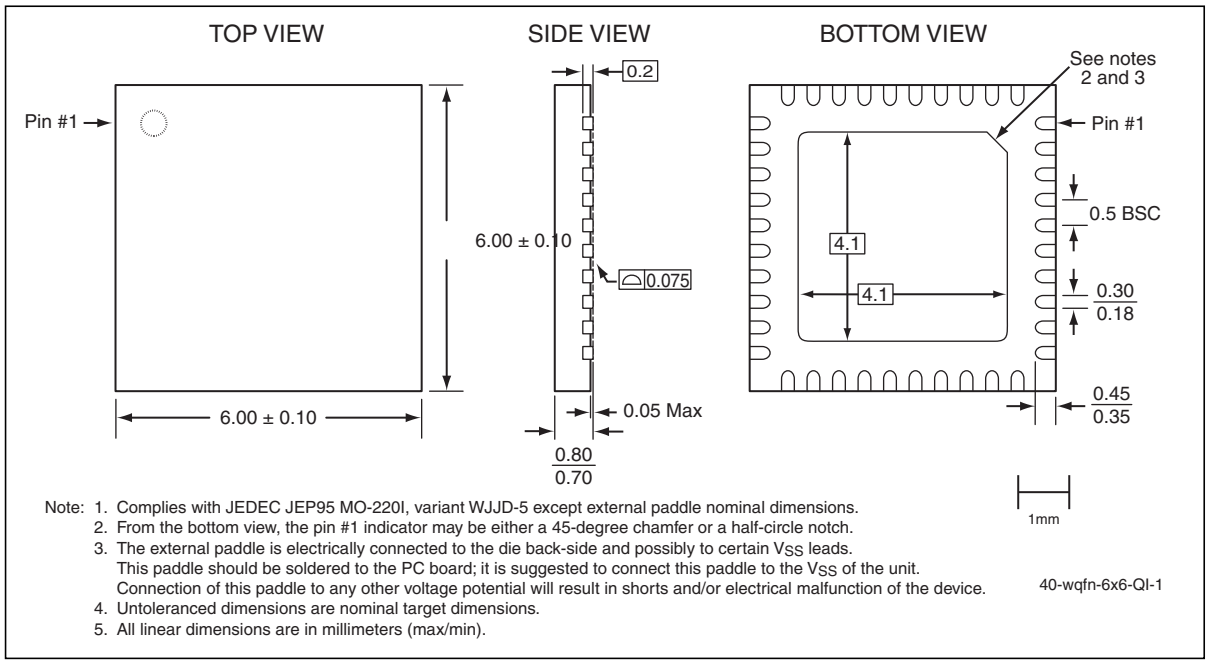


Figure 39: 40-Contact Very-Very-Thin Quad Flat No-lead (WQFN)
SST Package Code: QI

Table 38: Revision History

Revision	Description	Date
00	• Initial Release of data sheet	May 2007
01	• Added QIF non-pb (F) ordering info • Edited Product Description • Fixed typo in Figure 2, edited Table 1 • Text changes on page 11 and text changes to Figure 5 • Changes to tables 3-2, 3-3, 3-4, 3-5 and 3-7 • Removed note on page 20 and changed Reset Value • Changes to registers on pages 21-29 • Text changes on page 33 to section , Table 12, and inTable 13 • Edited sections 4.3, 4.3.1 and Figure 15 • Edited Figure 20. Edited Tables 20, 21, 22. • Edits in AMSR on page 64 • Edited inTable 34 and 35 and Figure 36 • Changed VIH4 parameter on page 66	Aug 2007
02	• Removed “Fast Mode” from Product Description • Edited description for P0[7:0], P1[7:0], P2[7:0], PSEN#, RST, EA#, and ALE/PROG# in Pin Description Table 1 • Replaced body text Section , “SCL Low Timeout” • Edited body text Section , “SCL High (SMBus Free) Timeout” • Edited body text Section , “SMBus SFR” • Replaced body text Section , “SMBus Control Register” • Changed number of 8-bit status codes from 28 to 31 in two places Section , “Status Register” • Replaced globally: S1STA by SM0STA; S1DAT by SM0DAT; S1CON by SM0CON; S1ADR by SM0ADR; SIO1 by SMBus • Edited body text Section , “SMBus SCL High and Low Duty” • Edited title and footnotes for Table 24 • Edited I_{IL} and I_{DD} values in Table 34 • Edited MAX parameters and footnote in Table 37	Feb 2008
03	• Changed Prog-Boot-Default to Prog-Boot-From-User-Vector, page 20 • Changed the value of Boot-From-User-Vector from “1” to “0”, Figure 15, page 37.	Jul 2008
04	• Added Commercial Temperature in Features and Product Ordering Information	Oct 2008
05	• Change “5V tolerant” to “can tolerate VDD +0.5V” in features, page 1, and I/O Descriptions, page 10.	Dec 2008
A	• Applied new document format • Released document under letter revision system • Updated Spec number from S71323 to DS25100	Dec 2011

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