

32-bit Microcontrollers

CMOS

FR60 MB91490 Series

MB91F492 / FV470

■ DESCRIPTION

The MB91490 series is Fujitsu's general-purpose 32-bit RISC microcontroller, which is designed for embedded control applications that require high-speed processing performance.

This series uses the FR60 CPU, which is compatible with the FR* family of CPUs.

* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of Fujitsu Microelectronics Limited.

■ FEATURES

- FR60 CPU
 - 32-bit RISC, load/store architecture, five-stage pipeline
 - Operating frequency of 80 MHz (PLL clock multiplied)
 - 16-bit fixed-length instructions (basic instructions)
 - Instruction execution speed : one instruction per cycle
 - Memory-to-memory transfer, bit processing, barrel shift instructions, etc. : instructions suitable for embedded applications
 - Function entry and exit instructions, multi load/store instructions of register contents : instructions compatible with C language.
 - Register interlock function to facilitate assembly-language coding
 - Built-in multiplier/instruction-level support
 - Signed 32-bit multiplication : 5 cycles
 - Signed 16-bit multiplication : 3 cycles
 - Interrupts (save PC and PS) : 6 cycles, 16 priority levels
 - Harvard architecture allowing program access and data access to be executed simultaneously
 - Instructions compatible with the FR family

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For the information for microcontroller supports, see the following web site.

<http://edevic.fujitsu.com/micom/en-support/>

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- Built-in Peripheral functions
 - I/O ports
 - NMI (Non Maskable Interrupt)
 - External interrupts
 - Bit search module (for REALOS)
Function to search for the position of the first bit that has changed from 1 to 0 in a word starting from the MSB
 - 16-bit reload timers
 - Timing generator
 - 8/16-bit PPG timers
 - Multi-function timer
 - 16-bit free-run timer
 - Input capture (Linked to free-run timer)
 - Output compare (Linked to free-run timer)
 - A/D start up compare (Linked to free-run timer)
 - Wave form generator
Various wave forms are generated by using output compare output, 16-bit PPG timer and 16-bit dead timer.
 - Base timer
Only one timer function can be selected from the 16-bit PWM timer, 16-bit PPG timer, 16/32-bit reload timer, and 16/32-bit PWC timer.
 - 8/16-bit up/down counter
 - Multi-function serial interface
 - Full-duplex double buffer
 - Asynchronous (start-stop synchronization) communication, clock synchronous communication, I²C standard mode (Max 100 kbps), I²C high-speed mode (selectable various modes at maximum of 400 kbps)
 - Selectable parity On/Off
 - Each channel has built-in baud rate generator
 - Error detection function for parity, frame and overrun errors
 - External clock can be used as transfer clock
 - With I²C function
 - 8/10-bit A/D Converter (Successive comparison type)
 - Resolution : 8-bit or 10-bit resolution selectable
 - Conversion time : 1.2 μ s (minimum conversion time for 33 MHz peripheral clock (CLKP))
1.2 μ s (minimum conversion time for 40 MHz peripheral clock (CLKP))
 - DMAC (DMA Controller)
 - Transfers can be started by software or by interrupts from the built-in peripherals
 - Wild register
 - Instructions or data located at a target address can be replaced (in the built-in Flash area only)
 - Low voltage detection interrupt / reset
 - Detects low voltage (3.7 V $\pm$ 0.3 V) and generate external interrupt
 - Detects low voltage (3.0 V $\pm$ 0.24 V) and generate system initialization reset
 - Flash memory security function
 - Protects the content of Flash memory
- Other Features
 - Watchdog timer
 - Low-power consumption modes
 - Sleep/stop function
 - CMOS technologies : 0.18 μ m
 - Power supply : Single power supply (V_{cc} = 2.7 V to 5.5 V)

■ PRODUCT LINEUP

Characteristics	Common EVA of the series	MB91490 series
	MB91FV470	MB91F492
Built-in Flash capacity	512 Kbytes (Flash)	256 Kbytes (Flash)
Flash security	—	○
Built-in RAM capacity	40 Kbytes	12 Kbytes
I/O ports	160	49
External interrupts	NMI 16 channels	NMI 7 channels
Reload timer	2 channels	2 channels
Timing generator	2 units	1 unit
PPG	8-bit × 16 channels 16-bit × 8 channels	8-bit × 8 channels 16-bit × 4 channels (PPG output: 3 channels)
Multi-function timer	2 units	1 unit
Free-run timer	6 channels	3 channels
OCU	12 channels	6 channels
ICU	8 channels	4 channels
A/D activating compare	6 channels	2 channels
Wave form generator	12 channels	6 channels
Base timer	6 channels	2 channels
Up/down counter	2 channels	1 channel
Multi-function serial interface	6 units (w FIFO)	3 units (w/o FIFO)
8/10-bit A/D converter	4 channels × 2 units 16 channels × 1 unit	4 channels × 1 unit 8 channels × 1 unit
Low voltage detection interrupt	—	1 channel
Low voltage detection reset	—	1 channel
DMAC	5 channels	5 channels
Wild register	16 channels	16 channels
Debug function	DSU4	—

○ : Supported

MB91490 Series

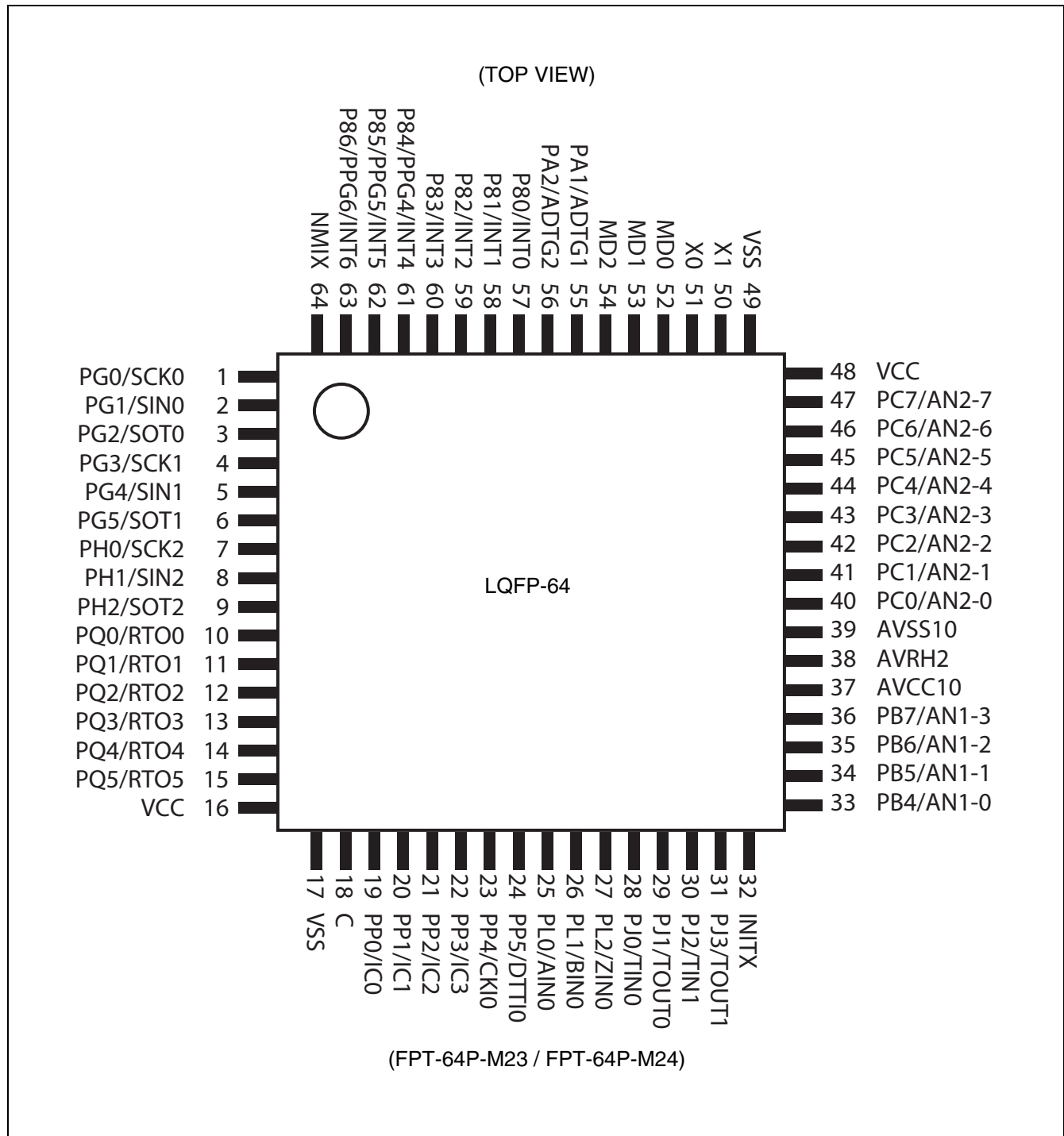
■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB91F492
FPT-64P-M23 (LQFP-0.65 mm)	○
FPT-64P-M24 (LQFP-0.50 mm)	○

○ : Supported

Note : For details of each package, refer to “■ PACKAGE DIMENSIONS”.

PIN ASSIGNMENT



MB91490 Series

■ PIN DESCRIPTION

Pin no.	Pin name	I/O circuit type*	Function
54	MD2	K	Mode pin 2 This pin sets the basic operating mode. During normal communication, input must be at the “L” level. During serial programming to flash memory, input must be at the “H” level.
53	MD1	K	Mode pin 1 This pin sets the basic operating mode. Input must always be at the “L” level.
52	MD0	K	Mode pin 0 This pin sets the basic operating mode. Input must always be at the “L” level.
51	X0	A	Clock (oscillation) input
50	X1	A	Clock (oscillation) output
32	INITX	I	External reset input
64	NMIX	H	NMI (Non Maskable Interrupt) input
57	INT0	D	External interrupt 0 input
	P80		General-purpose I/O port
58	INT1	D	External interrupt 1 input
	P81		General-purpose I/O port
59	INT2	D	External interrupt 2 input
	P82		General-purpose I/O port
60	INT3	D	External interrupt 3 input
	P83		General-purpose I/O port
61	INT4	D	External interrupt 4 input
	PPG4		Output of PPG timer 4
	P84		General-purpose I/O port
62	INT5	D	External interrupt 5 input
	PPG5		Output of PPG timer 5
	P85		General-purpose I/O port
63	INT6	D	External interrupt 6 input
	PPG6		Output of PPG timer 6
	P86		General-purpose I/O port
55	ADTG1	D	External trigger input of 8/10-bit A/D converter 1
	PA1		General-purpose I/O port
56	ADTG2	D	External trigger input of 8/10-bit A/D converter 2
	PA2		General-purpose I/O port

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Pin no.	Pin name	I/O circuit type*	Function
33	AN1-0	G	Analog 0 input of 8/10-bit A/D converter 1
	PB4		General-purpose I/O port
34	AN1-1	G	Analog 1 input of 8/10-bit A/D converter 1
	PB5		General-purpose I/O port
35	AN1-2	G	Analog 2 input of 8/10-bit A/D converter 1
	PB6		General-purpose I/O port
36	AN1-3	G	Analog 3 input of 8/10-bit A/D converter 1
	PB7		General-purpose I/O port
40	AN2-0	G	Analog 0 input of 8/10-bit A/D converter 2
	PC0		General-purpose I/O port
41	AN2-1	G	Analog 1 input of 8/10-bit A/D converter 2
	PC1		General-purpose I/O port
42	AN2-2	G	Analog 2 input of 8/10-bit A/D converter 2
	PC2		General-purpose I/O port
43	AN2-3	G	Analog 3 input of 8/10-bit A/D converter 2
	PC3		General-purpose I/O port
44	AN2-4	G	Analog 4 input of 8/10-bit A/D converter 2
	PC4		General-purpose I/O port
45	AN2-5	G	Analog 5 input of 8/10-bit A/D converter 2
	PC5		General-purpose I/O port
46	AN2-6	G	Analog 6 input of 8/10-bit A/D converter 2
	PC6		General-purpose I/O port
47	AN2-7	G	Analog 7 input of 8/10-bit A/D converter 2
	PC7		General-purpose I/O port
1	SCK0 (SCL0)	D	Clock I/O of multi-function serial interface 0 (used in I ² C mode, SCL0)
	PG0		General-purpose I/O port
2	SIN0	D	Data input of multi-function serial interface 0 (not used in I ² C mode)
	PG1		General-purpose I/O port
3	SOT0 (SDA0)	D	Data output of multi-function serial interface 0 (used in I ² C mode, SDA0)
	PG2		General-purpose I/O port

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Pin no.	Pin name	I/O circuit type*	Function
4	SCK1 (SCL1)	D	Clock I/O of multi-function serial interface 1 (used in I ² C mode, SCL1)
	PG3		General-purpose I/O port
5	SIN1	D	Data input of multi-function serial interface 1 (not used in I ² C mode)
	PG4		General-purpose I/O port
6	SOT1 (SDA1)	D	Data output of multi-function serial interface 1 (used in I ² C mode, SDA1)
	PG5		General-purpose I/O port
7	SCK2 (SCL2)	D	Clock I/O of multi-function serial interface 2 (used in I ² C mode, SCL2)
	PH0		General-purpose I/O port
8	SIN2	D	Data input of multi-function serial interface 2 (not used in I ² C mode)
	PH1		General-purpose I/O port
9	SOT2 (SDA2)	D	Data output of multi-function serial interface 2 (used in I ² C mode, SDA2)
	PH2		General-purpose I/O port
28	TIN0	D	Base timer 0 input
	PJ0		General-purpose I/O port
29	TOUT0	D	Base timer 0 output
	PJ1		General-purpose I/O port
30	TIN1	D	Base timer 1 input
	PJ2		General-purpose I/O port
31	TOUT1	D	Base timer 1 output
	PJ3		General-purpose I/O port
25	AIN0	D	8/16-bit up count input pin for up/down counter 0
	PL0		General-purpose I/O port
26	BIN0	D	8/16-bit down count input pin for up/down counter 0
	PL1		General-purpose I/O port
27	ZIN0	D	8/16-bit reset input pin for up/down counter 0
	PL2		General-purpose I/O port
19	IC0	D	Trigger input of input capture 0
	PP0		General-purpose I/O port
20	IC1	D	Trigger input of input capture 1
	PP1		General-purpose I/O port

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Pin no.	Pin name	I/O circuit type*	Function
21	IC2	D	Trigger input of input capture 2
	PP2		General-purpose I/O port
22	IC3	D	Trigger input of input capture 3
	PP3		General-purpose I/O port
23	CKI0	D	External clock input pin of free-run timer ch.0 to ch.2
	PP4		General-purpose I/O port
24	DTTI0	D	Input signal controlling wave form generator outputs RTO0 to RTO5 of multi-function timer 0
	PP5		General-purpose I/O port
10	RTO0	J	Wave form generator output of multi-function timer 0
	PQ0		General-purpose I/O port
11	RTO1	J	Wave form generator output of multi-function timer 0
	PQ1		General-purpose I/O port
12	RTO2	J	Wave form generator output of multi-function timer 0
	PQ2		General-purpose I/O port
13	RTO3	J	Wave form generator output of multi-function timer 0
	PQ3		General-purpose I/O port
14	RTO4	J	Wave form generator output of multi-function timer 0
	PQ4		General-purpose I/O port
15	RTO5	J	Wave form generator output of multi-function timer 0
	PQ5		General-purpose I/O port

* : Refer to “■ I/O CIRCUIT TYPE” for details on the I/O circuit types.

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Power supply pins and GND pins

Pin no.	Pin name	Function
16 48	VCC	Power supply pins Connect all pins to the same potential.
17 49	VSS	GND pins Connect all pins to the same potential.
18	C	Capacitor coupling pin for internal regulator
37	AVCC10	Analog power supply pin for 8/10-bit A/D converter 1/2
39	AVSS10	Analog GND pin for 8/10-bit A/D converter 1/2
38	AVRH2	Analog reference power supply pin for 8/10-bit A/D converter 1/2

■ I/O CIRCUIT TYPE

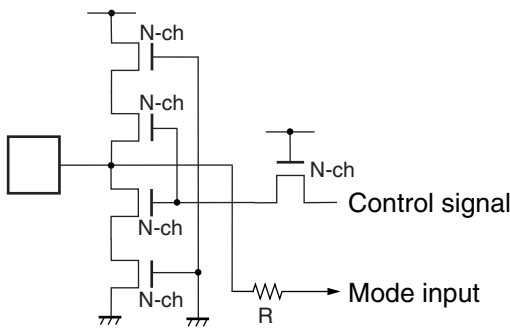
Type	Circuit	Remarks
A		Oscillation feedback resistance for high speed (main clock oscillation) approx. 1 MΩ
D		• CMOS level output • CMOS level hysteresis input • With standby control • With pull-up control
G		• Analog/CMOS level hysteresis I/O pin • CMOS level output • CMOS level hysteresis input (with standby control) • Analog input (Operates as an analog input when the corresponding AICR register bit is "1".) • With pull-up control

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Type	Circuit	Remarks
H		• CMOS level hysteresis input • Without standby control
I		• CMOS level hysteresis input • Without standby control • With pull-up resistance
J		• CMOS level output • CMOS level hysteresis input • With standby control • With pull-up control

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Type	Circuit	Remarks
K		CMOS level input

■ HANDLING DEVICES

- Preventing latch-up

Latch-up phenomenon may occur with CMOS IC, when a voltage higher than V_{CC} or lower than V_{SS} is applied to either the input or output terminals, or when a voltage is applied between V_{CC} pin and V_{SS} pin that exceeds the rated voltage. When latch-up occurs, a significant power-supply current surge results, which may damage some elements due to the excess heat, so great care must be taken to ensure that the maximum rating is never exceeded during use.

- Treatment of unused input pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, for example, using a pull-up or pull-down resistor.

- Power pins

In products with multiple V_{CC} and V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to the same potential power supply and a ground line externally to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance. It is also advisable to connect a ceramic capacitor of approximately 0.1 μF as a bypass capacitor between V_{CC} and V_{SS} pins near this device.

- Crystal oscillator circuit

Noise near the X0 and X1 pins may cause the device to malfunction. Design the printed circuit board so that X0, X1, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended to design the PC board artwork with the X0 and X1 pins surrounded by ground plane because stable operation can be expected with such a layout. Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

- About mode pins (MD0 to MD2)

These pins should be connected directly to V_{CC} pin or V_{SS} pin.

Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and power supply or GND pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

- Operation at start-up

Be sure to execute setting initialized reset (INIT) with INITX pin immediately after start-up.

Immediately after that, also, hold the "L"-level input to the INITX pin for the stabilization wait time required for the oscillator circuit to take the oscillation stabilization wait time for the oscillator circuit and the stabilization wait time for the regulator (For INIT via the INITX pin, the oscillation stabilization wait time setting is initialized to the minimum value).

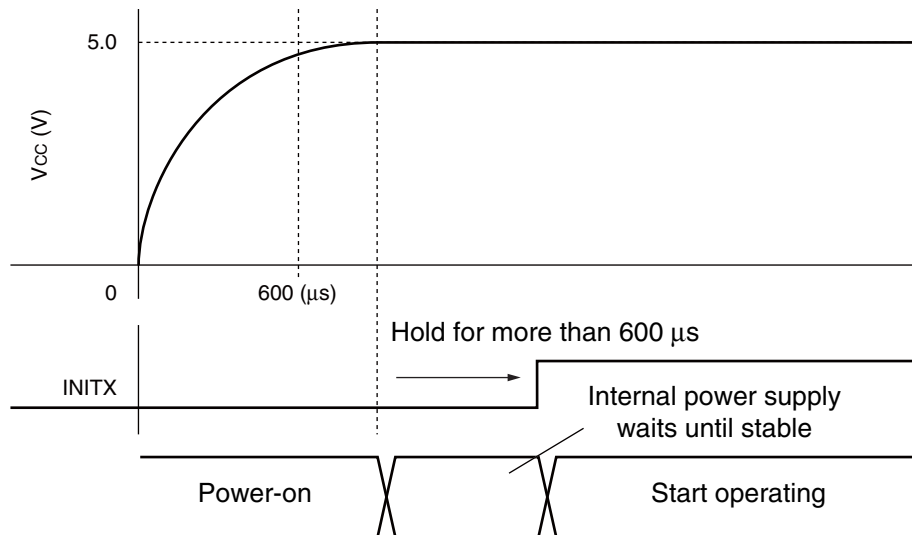
- Notes upon power-on sequence

It requires more than 600 μs (between 0.0 V to 5.0 V) to rise voltage upon power on in order to prevent the device malfunction caused by the overshooting in the built-in voltage step-down circuit.

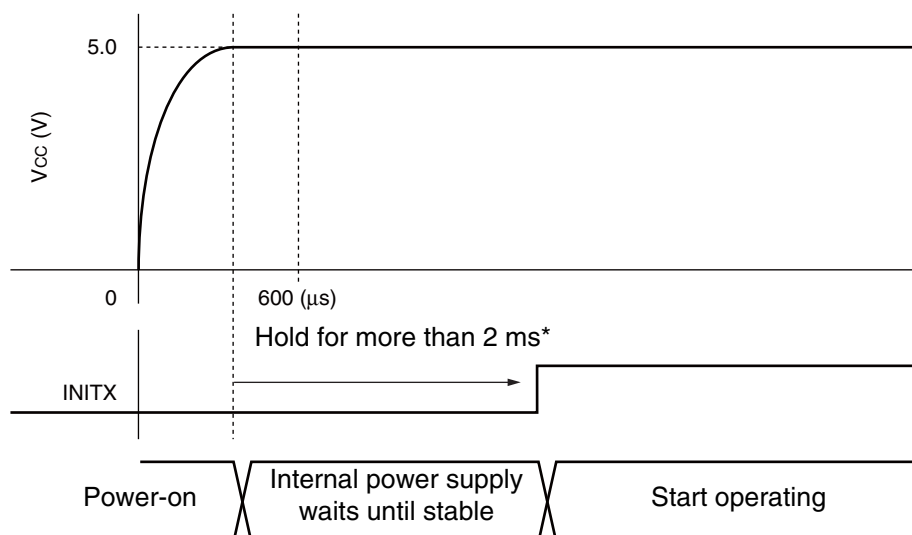
After the supply voltage is stable (voltage is risen) , it takes 600 μs until internal supply is stable. Hold the input to the INITX pin during that period.

If it takes less than 600 μs (between 0.0 V to 5.0 V) for power up, it requires 2 ms* until internal supply is stable after voltage supply is stable (voltage is risen) . Hold the input to the INITX pin during that period.

CASE : voltage rising time is more than 600 μs (0.0 V to 5.0 V)



CASE : voltage rising time is less than 600 μs (0.0 V to 5.0 V)



* : In case of which it takes less than 600 μs (between 0.0 V to 5.0 V) to rise voltage, the time to make internal power supply stable is proportional to the capacitance value of the bypass capacitor for the pin C. It takes 2 ms if the pin C = 4.7 μF ; 4 ms if the pin C = 9.4 μF .

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- Order of power turning ON/OFF

Use the following procedure for turning the power on or off. If not using the A/D converter, connect $AV_{CC} = V_{CC}$ and $AV_{SS} = V_{SS}$. Turn on the power supply in the sequence $V_{CC} \rightarrow AV_{CC} \rightarrow AVR_{H2}$, and turn off the power in the reverse sequence.

- Source oscillation input when turning on the power

When turning the power on, maintain the clock input until the device is released from the oscillation stabilization wait state.

- Cautions for operation during PLL clock mode

Even if the oscillator comes off or the clock input stops with the PLL clock selected for MB91490 series, MB91490 series may continue to operate at the free-run frequency of the PLL's internal self-oscillating oscillator circuit.

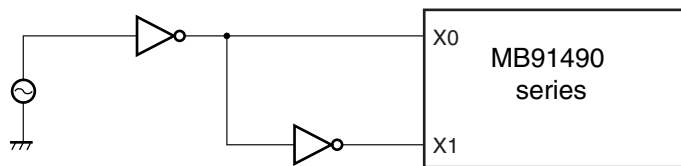
Performance of this operation, however, cannot be guaranteed.

- Using an external clock

When using an external clock, you must always input clock signals with opposite phase from X0 pin to X1 pin simultaneously. However, as the X1 pin halts with an output at the "H" level during stop mode, insert a resistor of approximately 1 k Ω externally to prevent a conflict between the two outputs if using stop mode (oscillation stop mode).

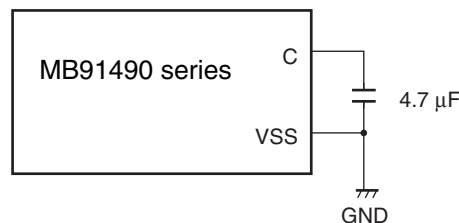
The figure below shows an example of how to use an external clock.

- Example of Using an External Clock



- C pin

As MB91490 series includes an internal regulator, always connect a bypass capacitor of approximately 4.7 μ F to the C pin for use by the regulator.

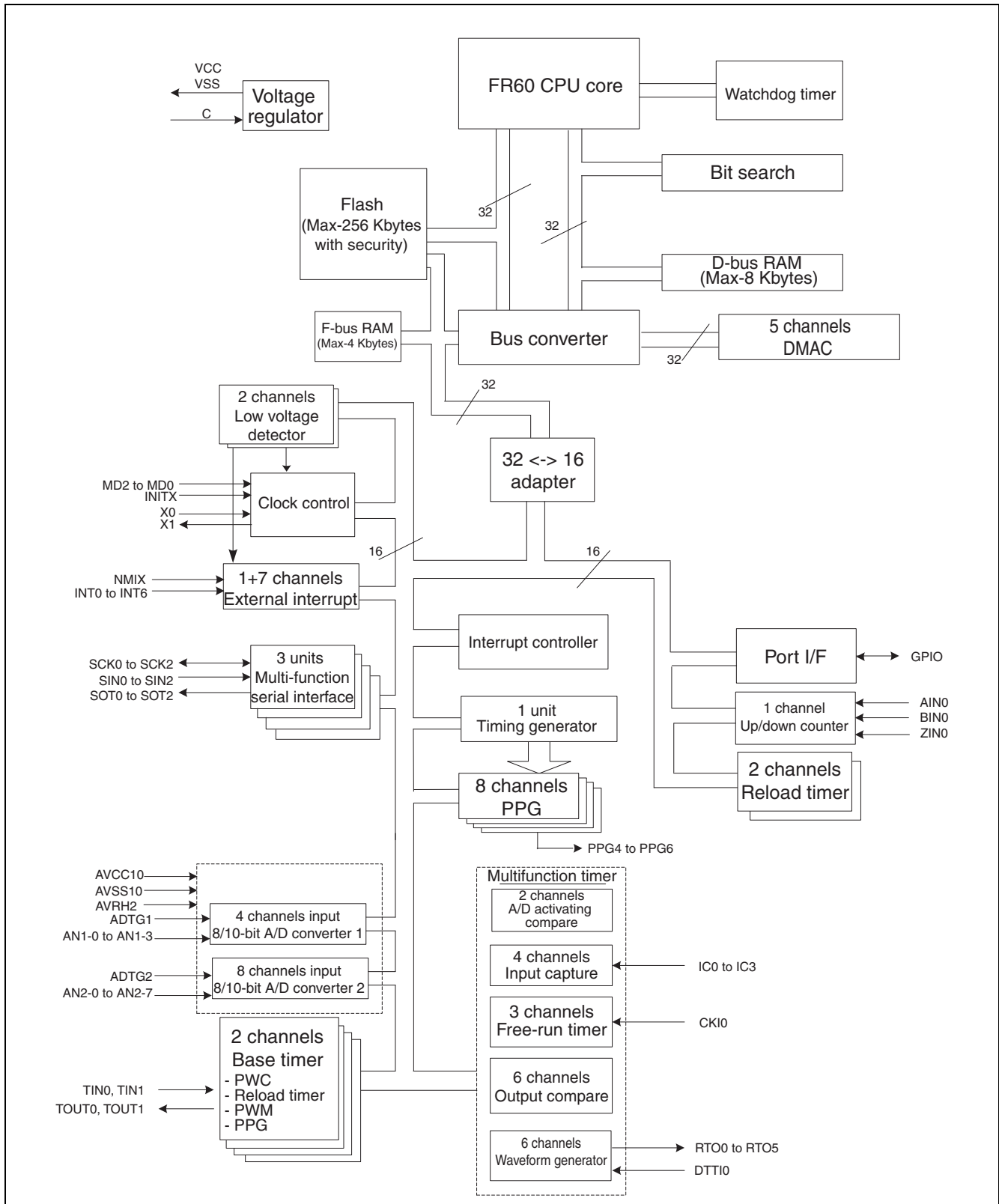


- Software reset on the synchronous mode

Be sure to meet the following two conditions before setting 0 to the SRST bit of STCR (standby control register) when the software reset is used on the synchronous mode.

- Set the interrupt enable flag (I-Flag) to interrupts disabled (I-Flag=0).
- Not used NMI

■ BLOCK DIAGRAM



■ MEMORY SPACE

1. Memory Space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

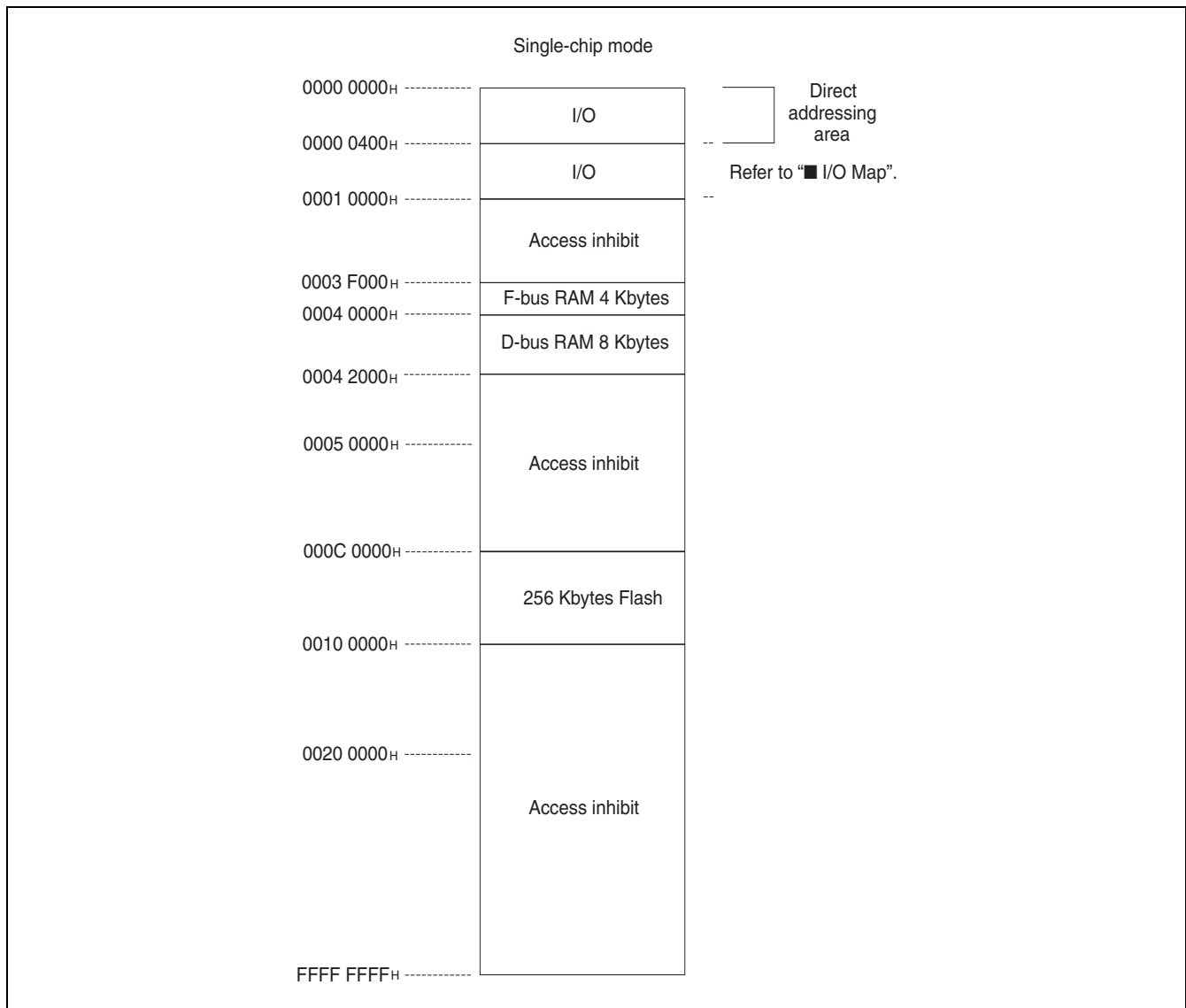
• Direct Addressing Areas

The following address space areas are used as I/O areas.

These areas are called direct addressing areas, in which the address of an operand can be specified directly by the instruction. The size of directly addressable areas depends on the length of the data being accessed as shown below.

- byte data access : 000_H to 0FF_H
- half word data access : 000_H to 1FF_H
- word data access : 000_H to 3FF_H

2. Memory Map



■ I/O MAP

[How to read the table]

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000 _H	PDR0 [R/W] B XXXXXXXX	PDR1 [R/W] B XXXXXXXX	PDR2 [R/W] B XXXXXXXX	PDR3 [R/W] B XXXXXXXX	T-unit Port data register

Read/write attribute, Access unit
(B : byte, H : half word, W : word)

Initial value of register after reset

Register name (column 1 of the register is at address 4n, column 2 is at address 4 n + 1...)

Leftmost register address (For word-length access, column 1 of the register is the MSB of the data.)

Note : Initial values of register bits are represented as follows :

“ 1 ” : Initial Value “ 1 ”

“ 0 ” : Initial Value “ 0 ”

“ X ” : Initial Value “ undefined ”

“ - ” : No physical register at this location

Access to addresses where the data access properties have not been documented is prohibited.

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Address	Register				Block
	+0	+1	+2	+3	
000000 _H	—				(Reserved)
000004 _H	—		PDR8 [R/W] B -XXXXXXX	—	Port data register
000008 _H	PDRA [R/W] B, H -----XX-	PDRB [R/W] B, H XXXX----	PDRC [R/W] B XXXXXXXXXX	—	
00000C _H	—		PDRG [R/W] B, H --XXXXXX	PDRH [R/W] B, H -----XXX	
000010 _H	PDRJ [R/W] B ---XXXX	—	PDRL [R/W] B ----XXX	—	
000014 _H	PDRP [R/W] B, H --XXXXXX	PDRQ [R/W] B, H --XXXXXX	—		
000018 _H to 00003C _H	—				(Reserved)
000040 _H	EIRR0 [R/W] B, H, W 00000000	ENIR0 [R/W] B, H, W 00000000	ELVR0 [R/W] B, H, W 00000000 00000000		External interrupt (INT0 to INT6, Low voltage detection interrupt)
000044 _H	DICR [R/W] B, H -----0	HRCL [R/W, R] B, H 0--11111	—		Delay interrupt/ hold request
000048 _H	TMRLR0 [W] H, W XXXXXXXXXX XXXXXXXXXX		TMR0 [R] H, W XXXXXXXXXX XXXXXXXXXX		Reload timer 0
00004C _H	—		TMCSR0 [R/W, R] B, H ----00-- ---00000		
000050 _H	TMRLR1 [W] H, W XXXXXXXXXX XXXXXXXXXX		TMR1 [R] H, W XXXXXXXXXX XXXXXXXXXX		Reload timer 1
000054 _H	—		TMCSR1 [R/W, R] B, H ----00-- ---00000		
000058 _H , 00005C _H	—				(Reserved)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000060 _H	SSR0 [R/W, R] B, H, W 00000011	ESCR0 [R/W]/ IBSR0 [R/W, R] B, H, W 00000000	SCR0 [R/W] / IBCR0 [R/W, R] B, H, W 00000000	SMR0 [R/W] B, H, W 000-0000	Multi- function serial interface 0
000064 _H	BGR01[R/W] B, H, W 00000000	BGR00 [R/W] B, H, W 00000000	RDR0 [R]/ TDR0 [W] H, W -----0 00000000		
000068 _H	—		ISMK0 [R/W] B, H 01111111	ISBA0 [R/W] B, H 00000000	
00006C _H	—				(Reserved)
000070 _H	SSR1 [R/W, R] B, H, W 00000011	ESCR1 [R/W]/ IBSR1 [R/W, R] B, H, W 00000000	SCR1 [R/W] / IBCR1 [R/W, R] B, H, W 00000000	SMR1 [R/W] B, H, W 000-0000	Multi- function serial interface 1
000074 _H	BGR11 [R/W] B, H, W 00000000	BGR10 [R/W] B, H, W 00000000	RDR1 [R]/ TDR1 [W] H, W -----0 00000000		
000078 _H	—		ISMK1 [R/W] B, H 01111111	ISBA1 [R/W] B, H 00000000	
00007C _H	—				(Reserved)
000080 _H	SSR2 [R/W, R] B, H, W 00000011	ESCR2 [R/W]/ IBSR2 [R/W, R] B, H, W 00000000	SCR2 [R/W] / IBCR2 [R/W, R] B, H, W 00000000	SMR2 [R/W] B, H, W 000-0000	Multi- function serial interface 2
000084 _H	BGR21 [R/W] B, H, W 00000000	BGR20 [R/W] B, H, W 00000000	RDR2 [R]/ TDR2 [W] H, W -----0 00000000		
000088 _H	—		ISMK2 [R/W] B, H 01111111	ISBA2 [R/W] B, H 00000000	
00008C _H	—				(Reserved)

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Address	Register				Block
	+0	+1	+2	+3	
000090 _H to 00009C _H	—				(Reserved)
0000A0 _H	OCCPBH0, OCCPBL0 [W]/ OCCPH0, OCCPL0 [R] H, W 00000000 00000000		OCCPBH1, OCCPBL1 [W]/ OCCPH1, OCCPL1 [R] H, W 00000000 00000000		OCU0
0000A4 _H	OCCPBH2, OCCPBL2 [W]/ OCCPH2, OCCPL2 [R] H, W 00000000 00000000		OCCPBH3, OCCPBL3 [W]/ OCCPH3, OCCPL3 [R] H, W 00000000 00000000		
0000A8 _H	OCCPBH4, OCCPBL4 [W]/ OCCPH4, OCCPL4 [R] H, W 00000000 00000000		OCCPBH5, OCCPBL5 [W]/ OCCPH5, OCCPL5 [R] H, W 00000000 00000000		
0000AC _H	OCSH1 [R/W] B, H, W -110--00	OCSL0 [R/W] B, H, W 00001100	OCSH3 [R/W] B, H, W -110--00	OCSL2 [R/W] B, H, W 00001100	
0000B0 _H	OCSH5 [R/W] B, H -110--00	OCSL4 [R/W] B, H 00001100	OCMOD0 [R/W] B --000000	—	
0000B4 _H	CPCLRBH0, CPCLRBL0 [W]/ CPCLRHO, CPCLRL0 [R] H, W 11111111 11111111		TCDTH0, TCDTL0 [R/W] H, W 00000000 00000000		Free-run timer 0
0000B8 _H	TCCSH0 [R/W] B, H, W 00000000	TCCSL0 [R/W] B, H, W 01000000	TCCSM0 [R/W] B, H, W ----0000	ADTRGC0 [R/W] B, H, W -0-0-0-0	
0000BC _H	CPCLRBH1, CPCLRBL1 [W] / CPCLRHO, CPCLRL1 [R] H, W 11111111 11111111		TCDTH1, TCDTL1 [R/W] H, W 00000000 00000000		Free-run timer 1
0000C0 _H	TCCSH1 [R/W] B, H, W 00000000	TCCSL1 [R/W] B, H, W 01000000	TCCSM1 [R/W] B, H, W ----0000	ADTRGC1 [R/W] B, H, W -0-0-0-0	
0000C4 _H	CPCLRBH2, CPCLRBL2 [W] / CPCLRHO, CPCLRL2 [R] H, W 11111111 11111111		TCDTH2, TCDTL2 [R/W] H, W 00000000 00000000		Free-run timer 2
0000C8 _H	TCCSH2 [R/W] B, H, W 00000000	TCCSL2 [R/W] B, H, W 01000000	TCCSM2 [R/W] B, H, W ----0000	ADTRGC2 [R/W] B, H, W -0-0-0-0	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0000CC _H	—	FRS2 [R/W] B --00--00	FRS1 [R/W] B, H --00--00	FRS0 [R/W] B, H --00--00	Free-run timer selector 0
0000D0 _H	—		FRS4 [R/W] B, H --00--00	FRS3 [R/W] B, H --00--00	
0000D4 _H	IPCPH0, IPCPL0 [R] H, W XXXXXXXX XXXXXXXX		IPCPH1, IPCPL1 [R] H, W XXXXXXXX XXXXXXXX		ICU0
0000D8 _H	IPCPH2, IPCPL2 [R] H, W XXXXXXXX XXXXXXXX		IPCPH3, IPCPL3 [R] H, W XXXXXXXX XXXXXXXX		
0000DC _H	PICSH01 [W, R] B, H, W 00000000	PICSL01 [R/W] B, H, W 00000000	ICSH23 [R] B, H, W -----00	ICSL23[R/W] B, H, W 00000000	
0000E0 _H	TMRRH0, TMRRL0 [R/W] H, W XXXXXXXX XXXXXXXX		TMRRH1, TMRRL1 [R/W] H, W XXXXXXXX XXXXXXXX		Wave form generator 0
0000E4 _H	TMRRH2, TMRRL2 [R/W] H XXXXXXXX XXXXXXXX		—		
0000E8 _H	DTCR0 [R/W] B, H 00000000	DTCR1 [R/W] B, H 00000000	DTCR2 [R/W] B 00000000	—	
0000EC _H	—	SIGCR10 [R/W] B 00000000	—	SIGCR20 [R/W] B 000000-1	
0000F0 _H	ADCOMP0 [W]/ ADCOMPB0 [R] H, W 00000000 00000000		ADCOMP0 [W]/ ADCOMPDB0 [R] H, W 00000000 00000000		
0000F4 _H	—				A/D activating compare 0
0000F8 _H	ADCOMP2 [W]/ ADCOMPB2 [R] H, W 00000000 00000000		ADCOMP2 [W]/ ADCOMPDB2 [R] H, W 00000000 00000000		
0000FC _H	—	ADTGBUF0 [R/W] B -0-0-1-1	ADTGSEL0 [R/W] B, H --00--00	ADTGCE0 [R/W] B, H --00--00	
000100 _H	PRLH0 [R/W] B, H, W XXXXXXXX	PRL0 [R/W] B, H, W XXXXXXXX	PRLH1 [R/W] B, H, W XXXXXXXX	PRL1 [R/W] B, H, W XXXXXXXX	PPG
000104 _H	PRLH2 [R/W] B, H, W XXXXXXXX	PRL2 [R/W] B, H, W XXXXXXXX	PRLH3 [R/W] B, H, W XXXXXXXX	PRL3 [R/W] B, H, W XXXXXXXX	

(Continued)

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Address	Register				Block
	+0	+1	+2	+3	
000108 _H	PPGC0 [R/W] B, H, W 00000000	PPGC1 [R/W] B, H, W 00000000	PPGC2 [R/W] B, H, W 00000000	PPGC3 [R/W] B, H, W 00000000	PPG
00010C _H	PRLH4 [R/W] B, H, W XXXXXXXXXX	PRLL4 [R/W] B, H, W XXXXXXXXXX	PRLH5 [R/W] B, H, W XXXXXXXXXX	PRLL5 [R/W] B, H, W XXXXXXXXXX	
000110 _H	PRLH6 [R/W] B, H, W XXXXXXXXXX	PRLL6 [R/W] B, H, W XXXXXXXXXX	PRLH7 [R/W] B, H, W XXXXXXXXXX	PRLL7 [R/W] B, H, W XXXXXXXXXX	
000114 _H	PPGC4 [R/W] B, H, W 00000000	PPGC5 [R/W] B, H, W 00000000	PPGC6 [R/W] B, H, W 00000000	PPGC7 [R/W] B, H, W 00000000	
000118 _H to 00012C _H	—				(Reserved)
000130 _H	—	TRG [R/W] B 00000000	—	GATEC0 [R/W] B --00--00	PPG
000134 _H	—	REVC [R/W] B 00000000	—	GATEC4 [R/W] B -----00	
000138 _H to 000140 _H	—				(Reserved)
000144 _H	TTCR0 [R/W, W, R] B 11110000	—			Timing generator 0
000148 _H	COMP0 [R/W] B, H, W 00000000	COMP2 [R/W] B, H, W 00000000	COMP4 [R/W] B, H, W 00000000	COMP6 [R/W] B, H, W 00000000	
00014C _H to 00015C _H	—				(Reserved)
000160 _H	BT0TMR [R] B, H, W 00000000 00000000		BT0TMCR [R/W] B, H, W -0000000 00000000		Base timer 0
000164 _H	—	BT0STC [R/W] B 00000000	—		
000168 _H	BT0PCSR/BT0PRLL [R/W] H, W XXXXXXXXXX XXXXXXXXXX		BT0PDUT/BT0PRLH/BT0DTBF [R/W] H, W XXXXXXXXXX XXXXXXXXXX		
00016C _H	—				(Reserved)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000170 _H	AICR2 [R/W] B, H ----- 11111111		—		8/10-bit A/D converter 2 (8 channels)
000174 _H	ADCS2 [R/W, W] B 0000000-	—	ADCH2 [R/W] B, H 00000000	ADMD2 [R/W] B, H 00001111	
000178 _H	ADCD002 [R] B, H, W 10----XX XXXXXXXX		ADCD012 [R] B, H, W 10----XX XXXXXXXX		
00017C _H	ADCD022 [R] B, H, W 10----XX XXXXXXXX		ADCD032 [R] B, H, W 10----XX XXXXXXXX		
000180 _H	ADCD042 [R] B, H, W 10----XX XXXXXXXX		ADCD052 [R] B, H, W 10----XX XXXXXXXX		
000184 _H	ADCD062 [R] B, H, W 10----XX XXXXXXXX		ADCD072 [R] B, H, W 10----XX XXXXXXXX		
000188 _H to 0001FC _H	—				(Reserved)
000200 _H	DMACA0 [R/W] B, H, W * 00000000 ----XXXX XXXXXXXX XXXXXXXX				DMAC
000204 _H	DMACB0 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000208 _H	DMACA1 [R/W] B, H, W * 00000000 ----XXXX XXXXXXXX XXXXXXXX				
00020C _H	DMACB1 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000210 _H	DMACA2 [R/W] B, H, W * 00000000 ----XXXX XXXXXXXX XXXXXXXX				
000214 _H	DMACB2 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000218 _H	DMACA3 [R/W] B, H, W * 00000000 ----XXXX XXXXXXXX XXXXXXXX				
00021C _H	DMACB3 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000220 _H	DMACA4 [R/W] B, H, W * 00000000 ----XXXX XXXXXXXX XXXXXXXX				
000224 _H	DMACB4 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				

(Continued)

MB91490 Series

Address	Register				Block
	+0	+1	+2	+3	
000228 _H to 00023C _H	—				(Reserved)
000240 _H	DMACR [R/W] B, H, W 0--00000 -----				DMAC
000244 _H to 0003EC _H	—				(Reserved)
0003F0 _H	BSD0 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit search module
0003F4 _H	BSD1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8 _H	BSDC [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FC _H	BSRR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400 _H	—				(Reserved)
000404 _H	—		DDR8 [R/W] B -0000000	—	Port direction register
000408 _H	DDRA [R/W] B, H ----00-	DDRB [R/W] B, H 0000----	DDRC [R/W] B 00000000	—	
00040C _H	—		DDRG [R/W] B, H --000000	DDRH [R/W] B, H -----000	
000410 _H	DDRJ [R/W] B ----0000	—	DDRL [R/W] B -----000	—	
000414 _H	DDRP [R/W] B, H --000000	DDRQ [R/W] B, H --000000	—		
000418 _H to 000420 _H	—				(Reserved)
000424 _H	—		PFR8 [R/W] B -000----	—	Port function register
000428 _H	—				(Reserved)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
00042C _H	—		PFRG [R/W] B, H --0-00-0	PFRH [R/W] B, H -----0-0	Port function register
000430 _H	PFRJ [R/W] B ----0-0-	—			
000434 _H	—	PFRQ [R/W] B --000000	—		
000438 _H , 00043C _H	—				(Reserved)
000440 _H	ICR00 [R/W, R] B, H, W ---11111	ICR01 [R/W, R] B, H, W ---11111	ICR02 [R/W, R] B, H, W ---11111	ICR03 [R/W, R] B, H, W ---11111	Interrupt controller
000444 _H	ICR04 [R/W, R] B, H, W ---11111	ICR05 [R/W, R] B, H, W ---11111	ICR06 [R/W, R] B, H, W ---11111	ICR07 [R/W, R] B, H, W ---11111	
000448 _H	ICR08 [R/W, R] B, H, W ---11111	ICR09 [R/W, R] B, H, W ---11111	ICR10 [R/W, R] B, H, W ---11111	ICR11 [R/W, R] B, H, W ---11111	
00044C _H	ICR12 [R/W, R] B, H, W ---11111	ICR13 [R/W, R] B, H, W ---11111	ICR14 [R/W, R] B, H, W ---11111	ICR15 [R/W, R] B, H, W ---11111	
000450 _H	ICR16 [R/W, R] B, H, W ---11111	ICR17 [R/W, R] B, H, W ---11111	ICR18 [R/W, R] B, H, W ---11111	ICR19 [R/W, R] B, H, W ---11111	
000454 _H	—				(Reserved)

(Continued)

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Address	Register				Block
	+0	+1	+2	+3	
000458 _H	ICR24 [R/W, R] B, H, W ---11111	ICR25 [R/W, R] B, H, W ---11111	ICR26 [R/W, R] B, H, W ---11111	ICR27 [R/W, R] B, H, W ---11111	Interrupt controller
00045C _H	ICR28 [R/W, R] B, H, W ---11111	ICR29 [R/W, R] B, H, W ---11111	ICR30 [R/W, R] B, H, W ---11111	ICR31 [R/W, R] B, H, W ---11111	
000460 _H	—	ICR33 [R/W, R] B ---11111	ICR34 [R/W, R] B, H ---11111	ICR35 [R/W, R] B, H ---11111	
000464 _H	ICR36 [R/W, R] B, H, W ---11111	ICR37 [R/W, R] B, H, W ---11111	ICR38 [R/W, R] B, H, W ---11111	ICR39 [R/W, R] B, H, W ---11111	
000468 _H	—	ICR41 [R/W, R] B ---11111	ICR42 [R/W, R] B, H ---11111	ICR43 [R/W, R] B, H ---11111	
00046C _H	ICR44 [R/W, R] B, H, W ---11111	ICR45 [R/W, R] B, H, W ---11111	ICR46 [R/W, R] B, H, W ---11111	ICR47 [R/W, R] B, H, W ---11111	
000470 _H to 00047C _H	—				(Reserved)
000480 _H	RSRR [R/W] B, H, W 1-0-0-00	STCR [R/W] B, H, W 001100-1	TBCR [R/W] B, H, W 00XXX-00	CTBR [W] B, H, W XXXXXXXXXX	Clock control block
000484 _H	CLKR [R/W] B -000-000	—	DIVR0 [R/W] B 00000011	—	
000488 _H to 00050C _H	—				(Reserved)
000510 _H	—	AICR1 [R/W] B ----1111	—		8/10-bit A/D converter 1 (4 channels)
000514 _H	ADCS1 [R/W, W] B 0000000-	—	ADCH1 [R/W] B, H --00--00	ADMD1 [R/W] B, H 00001111	
000518 _H	ADCD001 [R] B, H, W 10----XX XXXXXXXX		ADCD011 [R] B, H, W 10----XX XXXXXXXX		
00051C _H	ADCD021 [R] B, H, W 10----XX XXXXXXXX		ADCD031 [R] B, H, W 10----XX XXXXXXXX		

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000520 _H to 00053C _H	—				(Reserved)
000540 _H	RCR10 [W] B, H, W XXXXXXXXXX	RCR00 [W] B, H, W XXXXXXXXXX	UDCR10 [R] B, H, W 00000000	UDCR00 [R] B, H, W 00000000	Up/down counter 0
000544 _H	CCR0 [R/W] B, H 00000000	CCRL0 [R/W, R] B, H -0001000	—	CSR0 [R/W, R] B 00000000	
000548 _H to 00057C _H	—				(Reserved)
000580 _H	BT1TMR [R] B, H, W 00000000 00000000		BT1TMCR [R/W] B, H, W -0000000 00000000		Base timer 1
000584 _H	—	BT1STC [R/W] B 00000000	—		
000588 _H	BT1PCSR/BT1PRL [R/W] H, W XXXXXXXXXX XXXXXXXXX		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H, W XXXXXXXXXX XXXXXXXXX		
00058C _H to 000600 _H	—				(Reserved)
000604 _H	—		PCR8 [R/W] B -0000000	—	Pull-up resistor control register
000608 _H	PCRA [R/W] B, H -----00-	PCRB [R/W] B, H 0000----	PCRC [R/W] B 00000000	—	
00060C _H	—		PCRG [R/W] B, H --000000	PCRH [R/W] B, H -----000	
000610 _H	PCRJ [R/W] B ----0000	—	PCRL [R/W] B ----000	—	
000614 _H	PCRP [R/W] B, H --000000	PCRQ [R/W] B, H --000000	—		
000618 _H to 000FFC _H	—				(Reserved)

(Continued)

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Address	Register				Block
	+0	+1	+2	+3	
001000 _H	DMASA0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004 _H	DMADA0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008 _H	DMASA1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00100C _H	DMADA1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010 _H	DMASA2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014 _H	DMADA2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018 _H	DMASA3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00101C _H	DMADA3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020 _H	DMASA4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024 _H	DMADA4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028 _H to 006FFC _H	—				(Reserved)
007000 _H	FLCR [R/W, R] B ----X-0-	—			Flash memory
007004 _H	FLWC [R/W] B --11-011	—			
007008 _H to 007010 _H	—				
007014 _H to 00701C _H	—			(Reserved)	
007020 _H	WREN [R/W] H 00000000 00000000		—		Wild register control block
007024 _H to 00702C _H	—				(Reserved)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
007030 _H	WA00 [R/W] W ----- ----XXXX XXXXXXXX XXXXXX--				Wild register control block
007034 _H	WD00 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007038 _H	WA01 [R/W] W ----- ----XXXX XXXXXXXX XXXXXX--				
00703C _H	WD01 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007040 _H	WA02 [R/W] W ----- ----XXXX XXXXXXXX XXXXXX--				
007044 _H	WD02 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007048 _H	WA03 [R/W] W ----- ----XXXX XXXXXXXX XXXXXX--				
00704C _H	WD03 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007050 _H	WA04 [R/W] W ----- ----XXXX XXXXXXXX XXXXXX--				
007054 _H	WD04 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007058 _H	WA05 [R/W] W ----- ----XXXX XXXXXXXX XXXXXX--				
00705C _H	WD05 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007060 _H	WA06 [R/W] W ----- ----XXXX XXXXXXXX XXXXXX--				
007064 _H	WD06 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007068 _H	WA07 [R/W] W ----- ----XXXX XXXXXXXX XXXXXX--				
00706C _H	WD07 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007070 _H	WA08 [R/W] W ----- ----XXXX XXXXXXXX XXXXXX--				
007074 _H	WD08 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

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(Continued)

Address	Register				Block
	+0	+1	+2	+3	
007078 _H	WA09 [R/W] W ----- ----XXXX XXXXXXXXXX XXXXXXX--				Wild register control block
00707C _H	WD09 [R/W] W XXXXXXXX XXXXXXXXXX XXXXXXXXXX XXXXXXXXXX				
007080 _H	WA10 [R/W] W ----- ----XXXX XXXXXXXXXX XXXXXXX--				
007084 _H	WD10 [R/W] W XXXXXXXX XXXXXXXXXX XXXXXXXXXX XXXXXXXXXX				
007088 _H	WA11 [R/W] W ----- ----XXXX XXXXXXXXXX XXXXXXX--				
00708C _H	WD11 [R/W] W XXXXXXXX XXXXXXXXXX XXXXXXXXXX XXXXXXXXXX				
007090 _H	WA12 [R/W] W ----- ----XXXX XXXXXXXXXX XXXXXXX--				
007094 _H	WD12 [R/W] W XXXXXXXX XXXXXXXXXX XXXXXXXXXX XXXXXXXXXX				
007098 _H	WA13 [R/W] W ----- ----XXXX XXXXXXXXXX XXXXXXX--				
00709C _H	WD13 [R/W] W XXXXXXXX XXXXXXXXXX XXXXXXXXXX XXXXXXXXXX				
0070A0 _H	WA14 [R/W] W ----- ----XXXX XXXXXXXXXX XXXXXXX--				
0070A4 _H	WD14 [R/W] W XXXXXXXX XXXXXXXXXX XXXXXXXXXX XXXXXXXXXX				
0070A8 _H	WA15 [R/W] W ----- ----XXXX XXXXXXXXXX XXXXXXX--				
0070AC _H	WD15 [R/W] W XXXXXXXX XXXXXXXXXX XXXXXXXXXX XXXXXXXXXX				
0070B0 _H to 0FFFFC _H	—				(Reserved)

* : The lower 16 bits (DTC15 to DTC0) of DMACA0 to DMACA4 cannot be accessed as bytes.

- Notes :
- Data is undefined in reserved or (—) area.
 - Do not execute read modify write (RMW) instruction on registers having a write-only bit.
 - The initial values are varied depending on the product series. Please refer to the hardware manual of MB91490 series for more details.

■ INTERRUPT VECTOR

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	Decimal	Hexa-decimal			
Reset	0	00	—	3FC _H	000FFFFC _H
Mode vector	1	01	—	3F8 _H	000FFFF8 _H
System reserved	2	02	—	3F4 _H	000FFFF4 _H
System reserved	3	03	—	3F0 _H	000FFFF0 _H
System reserved	4	04	—	3EC _H	000FFFE _C
System reserved	5	05	—	3E8 _H	000FFFE8 _H
System reserved	6	06	—	3E4 _H	000FFFE4 _H
Coprocessor absent trap	7	07	—	3E0 _H	000FFFE0 _H
Coprocessor error trap	8	08	—	3DC _H	000FFFD _C
INTE instruction	9	09	—	3D8 _H	000FFFD8 _H
System reserved	10	0A	—	3D4 _H	000FFFD4 _H
System reserved	11	0B	—	3D0 _H	000FFFD0 _H
Step trace trap	12	0C	—	3CC _H	000FFFC _C
NMI request (tool)	13	0D	—	3C8 _H	000FFFC8 _H
Undefined instruction exception	14	0E	—	3C4 _H	000FFFC4 _H
NMI request	15	0F	—	3C0 _H	000FFFC0 _H
External interrupt 0	16	10	ICR00	3BC _H	000FFFB _C
External interrupt 1	17	11	ICR01	3B8 _H	000FFFB8 _H
External interrupt 2	18	12	ICR02	3B4 _H	000FFFB4 _H
External interrupt 3	19	13	ICR03	3B0 _H	000FFFB0 _H
External interrupt 4	20	14	ICR04	3AC _H	000FFFA _C
External interrupt 5	21	15	ICR05	3A8 _H	000FFFA8 _H
External interrupt 6	22	16	ICR06	3A4 _H	000FFFA4 _H
Low voltage detection interrupt	23	17	ICR07	3A0 _H	000FFFA0 _H
Reload timer 0	24	18	ICR08	39C _H	000FFF9 _C
Reload timer 1	25	19	ICR09	398 _H	000FFF98 _H
Base timer 0 (source 0/source 1)	26	1A	ICR10	394 _H	000FFF94 _H
Multi-function serial interface 0 (UART transmission completed/reception completed/I ² C status)	27	1B	ICR11	390 _H	000FFF90 _H
Multi-function serial interface 1 (UART transmission completed/reception completed/I ² C status)	28	1C	ICR12	38C _H	000FFF8 _C
Base timer 1 (source 0/source 1)	29	1D	ICR13	388 _H	000FFF88 _H

(Continued)

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Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	Decimal	Hexa-decimal			
Up/down counter 0	30	1E	ICR14	384 _H	000FFF84 _H
DTTIO	31	1F	ICR15	380 _H	000FFF80 _H
DMAC0 (end/error)	32	20	ICR16	37C _H	000FFF7C _H
DMAC1 (end/error)	33	21	ICR17	378 _H	000FFF78 _H
DMAC2/3/4 (end/error)	34	22	ICR18	374 _H	000FFF74 _H
Multi-function serial interface 2 (UART transmission completed/reception completed/I ² C status)	35	23	ICR19	370 _H	000FFF70 _H
System reserved	36	24	—	36C _H	000FFF6C _H
System reserved	37	25	—	368 _H	000FFF68 _H
System reserved	38	26	—	364 _H	000FFF64 _H
System reserved	39	27	—	360 _H	000FFF60 _H
PPG0/PPG1	40	28	ICR24	35C _H	000FFF5C _H
PPG2/PPG3	41	29	ICR25	358 _H	000FFF58 _H
PPG4/PPG5	42	2A	ICR26	354 _H	000FFF54 _H
PPG6/PPG7	43	2B	ICR27	350 _H	000FFF50 _H
Wave form generator 0 (underflow)	44	2C	ICR28	34C _H	000FFF4C _H
Wave form generator 1 (underflow)	45	2D	ICR29	348 _H	000FFF48 _H
Wave form generator 2 (underflow)	46	2E	ICR30	344 _H	000FFF44 _H
Timebase timer overflow	47	2F	ICR31	340 _H	000FFF40 _H
System reserved	48	30	—	33C _H	000FFF3C _H
Free-run timer 0 (compare clear)	49	31	ICR33	338 _H	000FFF38 _H
Free-run timer 0 (zero detection)	50	32	ICR34	334 _H	000FFF34 _H
Free-run timer 1 (compare clear)	51	33	ICR35	330 _H	000FFF30 _H
Free-run timer 1 (zero detection)	52	34	ICR36	32C _H	000FFF2C _H
Free-run timer 2 (compare clear)	53	35	ICR37	328 _H	000FFF28 _H
Free-run timer 2 (zero detection)	54	36	ICR38	324 _H	000FFF24 _H
8/10-bit A/D converter 2	55	37	ICR39	320 _H	000FFF20 _H
System reserved	56	38	—	31C _H	000FFF1C _H
8/10-bit A/D converter 1	57	39	ICR41	318 _H	000FFF18 _H
ICU0/ICU1 (capture)	58	3A	ICR42	314 _H	000FFF14 _H
ICU2/ICU3 (capture)	59	3B	ICR43	310 _H	000FFF10 _H
OCU0/OCU1 (match)	60	3C	ICR44	30C _H	000FFF0C _H

(Continued)

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	Decimal	Hexa-decimal			
OCU2/OCU3 (match)	61	3D	ICR45	308 _H	000FFF08 _H
OCU4/OCU5 (match)	62	3E	ICR46	304 _H	000FFF04 _H
Interrupt delay source bit	63	3F	ICR47	300 _H	000FFF00 _H
System reserved (Used by REALOS)	64	40	—	2FC _H	000FFEFC _H
System reserved (Used by REALOS)	65	41	—	2F8 _H	000FFE8 _H
System reserved	66	42	—	2F4 _H	000FFE4 _H
System reserved	67	43	—	2F0 _H	000FFE0 _H
System reserved	68	44	—	2EC _H	000FEEC _H
System reserved	69	45	—	2E8 _H	000FEE8 _H
System reserved	70	46	—	2E4 _H	000FEE4 _H
System reserved	71	47	—	2E0 _H	000FEE0 _H
System reserved	72	48	—	2DC _H	000FFEDC _H
System reserved	73	49	—	2D8 _H	000FFED8 _H
System reserved	74	4A	—	2D4 _H	000FFED4 _H
System reserved	75	4B	—	2D0 _H	000FFED0 _H
System reserved	76	4C	—	2CC _H	000FFEC _H
System reserved	77	4D	—	2C8 _H	000FFEC8 _H
System reserved	78	4E	—	2C4 _H	000FFEC4 _H
System reserved	79	4F	—	2C0 _H	000FFEC0 _H
Used by INT instruction	80 to 255	50 to FF	—	2BC _H to 000 _H	000FFEBC _H to 000FFC00 _H

■ PIN STATUS IN EACH CPU STATE

Terms used as the status of pins mean as follows.

- Input enabled
Means that the input function can be used.
- Input disabled
Indicates that the input function cannot be used.
- Input fixed to "0"
A state of a pin, in which "0" is transmitted to internal circuitry, with the external input shut off by the input gate adjacent to the pin.
- Output Hi-Z
Means to place a pin in a high impedance state by disabling the pin driving transistor from driving.
- Preserving the previous state
Means to output the state existing immediately prior to entering this mode.
That is, to output according to an internal resource with an output when it is operating or to preserve an output when the output is provided, for example, as a port.
- Input enabled when external interrupt function selected and enabled
Inputs are allowed only when the pin is configured as an external interrupt request input pin and the external interrupt request is enabled.

• List of pin status

Pin name	Function	During initialization		In sleep mode	In stop mode	
		INITX = "L"*1 or when Low voltage detection reset occurs	INITX = "H"*2 or when Low voltage detection reset is released		HIZ = 0	HIZ = 1
NMIX	NMIX	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
P80 to P83	INT0 to INT3	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Input enabled	Input enabled	Output Hi-Z/ Input "0" fixed
P84	INT4/PPG4					Input enabled when interrupt function selected and enabled
P85	INT5/PPG5					
P86	INT6/PPG6					
PA1, PA2	ADTG1, ADTG2	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input "0" fixed
PB4 to PB7	AN1-0 to AN1-3	Output Hi-Z/ Input disabled	Output Hi-Z/ Input "0" fixed	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input "0" fixed
PC0 to PC7	AN2-0 to AN2-7					
PG0, PG3	SCK0, SCK1	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/In- put "0" fixed
PG1, PG4	SIN0, SIN1					
PG2, PG5	SOT0, SOT1					
PH0	SCK2					
PH1	SIN2					
PH2	SOT2					
PJ0, PJ2	TIN0, TIN1	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/In- put "0" fixed
PJ1, PJ3	TOUT0, TOUT1					
PL0	AIN0	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/In- put "0" fixed
PL1	BIN0					
PL2	ZIN0					
PP0 to PP3	IC0 to IC3	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/In- put "0" fixed
PP4	CKI0					
PP5	DTTIO					
PQ0 to PQ5	RTO0 to RTO5					

*1 : INITX = "L" : Indicates the pin status with INITX remaining at the "L" level.

*2 : INITX = "H" : Indicates the pin status existing immediately after INITX transition from "L" to "H" level.

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■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V _{CC}	V _{SS} – 0.5	V _{SS} + 6.0	V	
Analog power supply voltage*1,*2,*6	AVCC10	V _{SS} – 0.5	V _{SS} + 6.0	V	
Analog reference voltage*7	AVRH2	V _{SS} – 0.5	V _{SS} + 6.0	V	
Input voltage*1	V _I	V _{SS} – 0.3	V _{CC} + 0.3	V	
Analog pin input voltage*1	V _{IA}	V _{SS} – 0.3	AV _{CC} + 0.3	V	
Output voltage*1	V _O	V _{SS} – 0.3	V _{CC} + 0.3	V	
“L” level maximum output current*3	I _{OL}	—	10	mA	
“L” level average output current*4	I _{OLAV}	—	4	mA	Except port Q0 to Q5
			12	mA	Port Q0 to Q5
“L” level total maximum output current	ΣI _{OL}	—	100	mA	
“L” level total average output current*5	ΣI _{OLAV}	—	50	mA	
“H” level maximum output current*3	I _{OH}	—	–10	mA	
“H” level average output current *4	I _{OHAV}	—	–4	mA	Except port Q0 to Q5
			–12	mA	Port Q0 to Q5
“H” level total maximum output current	ΣI _{OH}	—	–100	mA	
“H” level total average output current*5	ΣI _{OHAV}	—	–50	mA	
Power consumption	P _D	—	430	mW	
Storage temperature	T _{STG}	–55	+125	°C	

*1 : The parameter is based on V_{SS} = AVSS10 = 0 V.

*2 : Be careful not to exceed V_{CC} + 0.3 V, for example, when the power is turned on.
Be careful to set AVCC10 equal V_{CC}, for example, when the power is turned on.

*3 : The maximum output current is the peak value for a single pin.

*4 : The average output is the average current for a single pin over a period of 100 ms.

*5 : The total average output current is the average current for all pins over a period of 100 ms.

*6 : AVCC10 is the analog supply voltage for the 8/10-bit A/D converter.

*7 : AVRH2 is the analog reference voltage for the 8/10-bit A/D converter.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

($V_{SS} = AVSS10 = 0.0\text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	2.7	5.5	V	
Analog power supply voltage	AVCC10	$V_{SS} + 2.7$	$V_{SS} + 5.5$	V	For all 8/10-bit A/D converters (common use)
Analog reference voltage	AVRH2	AVSS10	AVCC10	V	For all 8/10-bit A/D converters (common use)
Operating temperature	T_A	- 40	+ 85	°C	

Note : During power-on, it takes approximately 600 μs for the internal power supply to stabilize after the V_{CC} power supply has stabilized. Continue to assert the INITX pin during this period.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

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3. DC Characteristics

($V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $V_{SS} = AVSS10 = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHS}	CMOS hysteresis input pin	—	$V_{CC} \times 0.8$	—	V_{CC}	V	
"L" level input voltage	V_{ILS}	CMOS hysteresis input pin	—	V_{SS}	—	$V_{CC} \times 0.2$	V	
"H" level output voltage	V_{OH1}	Except port Q0 to Q5	$V_{CC} = 5.0 \text{ V}$, $I_{OH} = 4 \text{ mA}$	$V_{CC} - 0.5$	—	—	V	
	V_{OH2}	Port Q0 to Q5	$V_{CC} = 5.0 \text{ V}$, $I_{OH} = 12 \text{ mA}$	$V_{CC} - 0.5$	—	—	V	*1
			$V_{CC} = 3.0 \text{ V}$, $I_{OH} = 4 \text{ mA}$	$V_{CC} - 0.5$	—	—	V	*2
"L" level output voltage	V_{OL1}	Except port Q0 to Q5	$V_{CC} = 5.0 \text{ V}$, $I_{OL} = 4 \text{ mA}$	—	—	$V_{SS} + 0.4$	V	
	V_{OL2}	Port Q0 to Q5	$V_{CC} = 5.0 \text{ V}$, $I_{OL} = 12 \text{ mA}$	—	—	$V_{SS} + 0.4$	V	*1
			$V_{CC} = 3.0 \text{ V}$, $I_{OL} = 4 \text{ mA}$	—	—	$V_{SS} + 0.4$	V	*2
Input leak current	I_{LI}	—	$V_{CC} = 5.0 \text{ V}$, $V_{SS} < V_i < V_{CC}$	-5	—	—	μA	
Pull-up resistance	R_{PULL}	INITX, pull-up pin	—	—	50	—	k Ω	
Power supply current	I_{CC}	VCC	$V_{CC} = 5.0 \text{ V}$, $f_c = 20 \text{ MHz}$, PLL $\times 4$, CLKB = 80 MHz CLKP = 40 MHz Flash memory 3 wait (4cycle) access	—	60	70	mA	
			$V_{CC} = 5.0 \text{ V}$, $f_c = 10 \text{ MHz}$, PLL $\times 5$, CLKB = 50 MHz CLKP = 25 MHz Flash memory 2 wait (3cycle) access	—	45	55	mA	
			$V_{CC} = 5.0 \text{ V}$, $f_c = 10 \text{ MHz}$, PLL $\times 4$, CLKB = 40 MHz CLKP = 40 MHz Flash memory 2 wait (3cycle) access	—	40	50	mA	

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($V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $V_{SS} = AVSS10 = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCS}	VCC	$V_{CC} = 5.0 \text{ V}$, $f_c = 20 \text{ MHz}$, PLL $\times 4$, CLKB = 80 MHz CLKP = 40 MHz Flash memory 3 wait (4cycle) access	—	15	22	mA	In sleep mode
			$V_{CC} = 5.0 \text{ V}$, $f_c = 10 \text{ MHz}$, PLL $\times 5$, CLKB = 50 MHz CLKP = 25 MHz Flash memory 2 wait (3cycle) access	—	9	15	mA	In sleep mode
			$V_{CC} = 5.0 \text{ V}$, $f_c = 10 \text{ MHz}$, PLL $\times 4$, CLKB = 40 MHz CLKP = 40 MHz Flash memory 2 wait (3cycle) access	—	11	17	mA	In sleep mode
	I_{CCH}	VCC	$V_{CC} = 5.0 \text{ V}$, $T_A = +25 \text{ }^{\circ}\text{C}$	—	60	200	μA	In stop mode
Input capacitance	C_{IN}	Other than VCC, VSS, AVSS10, AVCC10, AVRH2	—	—	5	15	pF	

*1 : $V_{CC} = 4.0 \text{ V to } 5.5 \text{ V}$

*2 : $V_{CC} = 2.7 \text{ V to } 4.0 \text{ V}$

4. Flash Memory Write/Erase Characteristics

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (8 Kbytes sectors)	$V_{CC} = 5.0 \text{ V}$, $T_A = +25 \text{ }^{\circ}\text{C}$	—	0.5	2.0	s	Not including time for internal writing before deletion.
Word write time	$V_{CC} = 5.0 \text{ V}$, $T_A = +25 \text{ }^{\circ}\text{C}$	—	6	100	μs	Not including system-level overhead time.
Chip erase time	$V_{CC} = 5.0 \text{ V}$, $T_A = +25 \text{ }^{\circ}\text{C}$	—	1.8	29.5	s	Not including system-level overhead time.
Erase/write cycle	—	10000	—	—	cycle	
Flash memory data hold time	—	10	—	—	year	

5. AC Characteristics

(1) Clock Timing

($V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $V_{SS} = AVSS10 = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$)

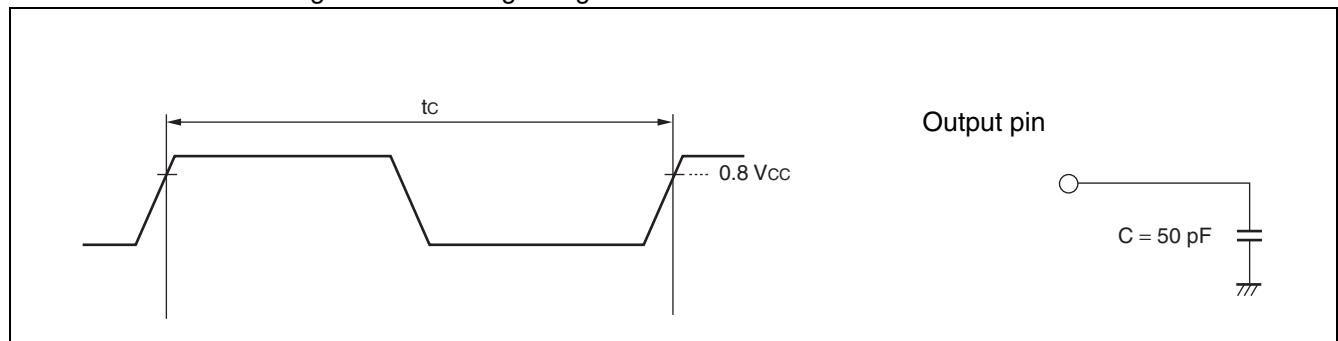
Parameter	Sym- bol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	f _c	X0 X1	—	10*2	—	20	MHz	When using the PLL within the self-oscillating range, set the multiplier so that the internal clock does not exceed the internal operating clock frequency.
Clock cycle time	t _c	X0 X1		50*2	—	100	ns	
Internal operating clock frequency	f _{CPB}	—	When 20 MHz is input as the X0 clock frequency and the oscillator circuit PLL system is set to × 4 multiplication	5*1	—	80	MHz	CPU
	f _{CPP}			5*1	—	40	MHz	Peripheral
Internal operating clock cycle time	t _{CPB}	—		12.5	—	200	ns	CPU
	t _{CPP}			25	—	200	ns	Peripheral

*1 : The values assume a gear cycle of 1/16.

*2 : When the PLL is used, the PLL multiplication rate varies depending on the frequency of the clock input to the X0 and X1 pins. Set the PLL multiplication rate so that the PLL output clock frequency is in the range between 40 MHz and 80 MHz.

PLL Multiplication Rate	1	2	3	4	5	6	7	8	Unit
PLL output clock frequency when X0 = 10 MHz	(Setting not allowed)			40	50	60	70	80	MHz
PLL output clock frequency when X0 = 20 MHz	(Setting not allowed)	40	60	80	(Setting not allowed)				

• Conditions for measuring the clock timing ratings



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(2) PLL Oscillation stabilization time (LOCK UP TIME)

($V_{CC} = 2.7 \text{ V}$ to 5.5 V , $V_{SS} = AVSS10 = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
PLL Oscillation stabilization wait time (LOCK UP TIME)	t_{LOCK}^*	—	—	600	—	μs

* : The length of time to wait for the PLL oscillations to stabilize.

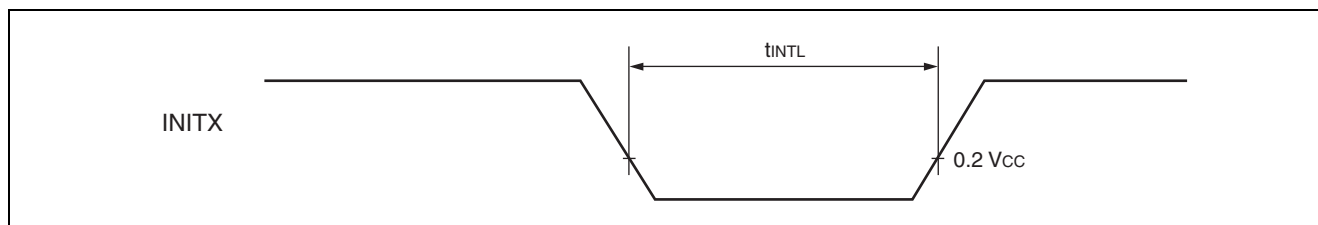
(3) Reset Input Ratings

($V_{CC} = 2.7 \text{ V}$ to 5.5 V , $V_{SS} = AVSS10 = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
INITX input time (at power-on)	t_{INTL}	INITX	—	$t_{PON} + t_{STBL} +$ Oscillation time of oscillator + $t_c \times 2^{13}$	—	ns
INITX input time (at STOP)				Oscillation time of oscillator + $t_c \times 10$	—	ns
INITX input time (other than the above)				$t_c \times 10$	—	ns

Notes : • For t_c (clock cycle time), refer to “(1) Clock Timing”.

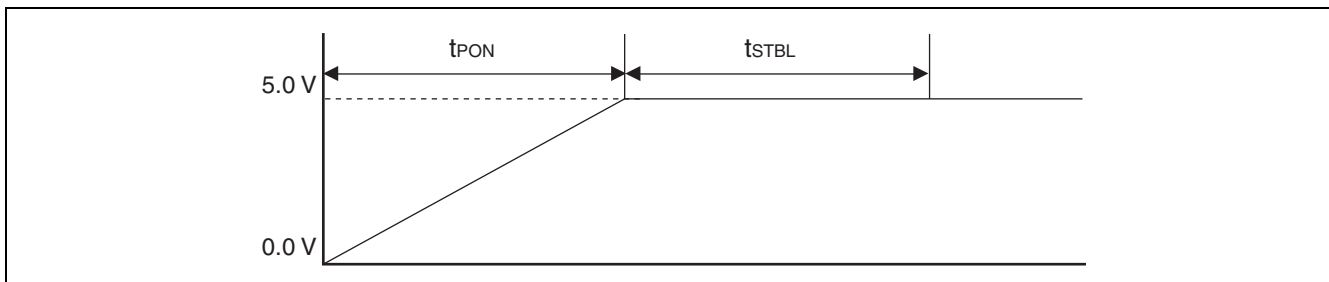
• For t_{PON} and t_{STBL} , refer to “(4) Power on Rise Time /Power-on Stabilization Time Ratings”.



(4) Power on Rise Time /Power-on Stabilization Time Ratings

($V_{SS} = AVSS10 = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
Power on rise time	t_{PON}	VCC	—	600	—	μs
power-on stabilization time	t_{STBL}			600	—	μs



(5) UART Timing

($V_{CC} = 2.7 \text{ V}$ to 5.5 V , $V_{SS} = AVSS10 = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	Internal shift clock mode	$4t_{CYCP}$	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK2 SOT0 to SOT2		− 20	+ 20	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK2 SIN0 to SIN2		30	—	ns	*1
				35	—	ns	*2
SCK ↑ → Valid SIN hold time	t_{SHIX}	SCK0 to SCK2 SIN0 to SIN2		0	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK2	External shift clock mode	$2 \times t_{CYCP} - 10$	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK2		$t_{CYCP} + 10$	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK2 SOT0 to SOT2		—	25	ns	*1
				—	35	ns	*2
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK2 SIN0 to SIN2		10	—	ns	
SCK ↑ → Valid SIN hold time	t_{SHIX}	SCK0 to SCK2 SIN0 to SIN2		20	—	ns	

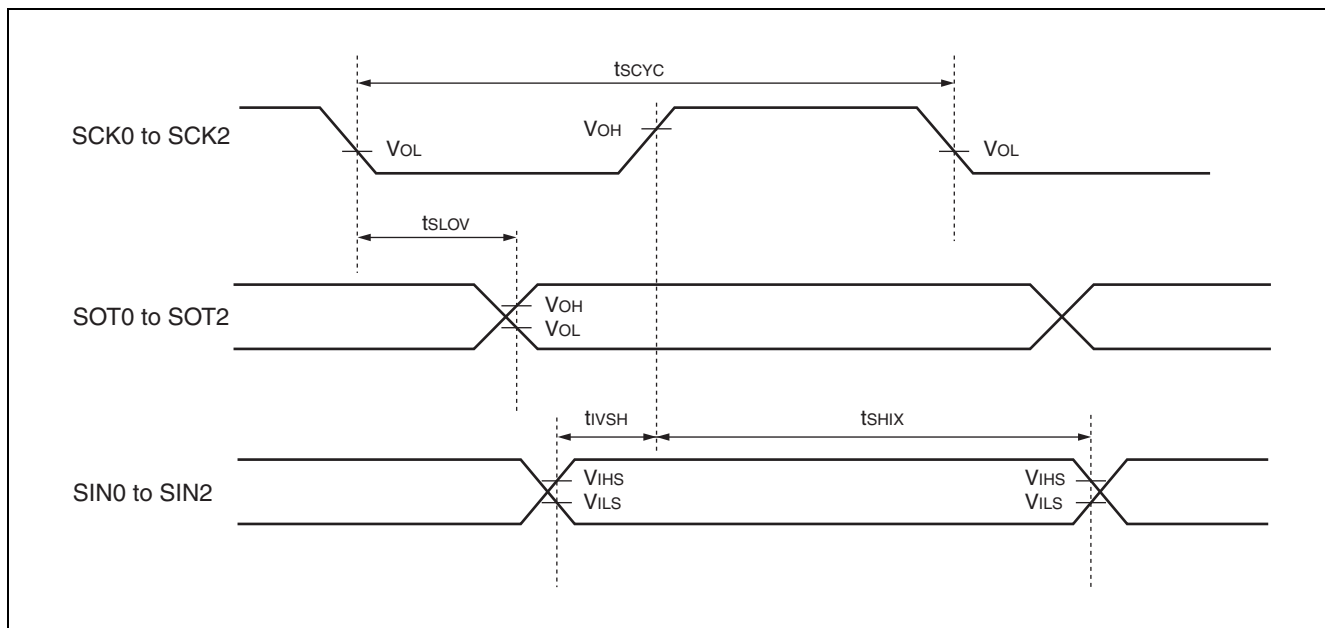
*1 : $V_{CC} = 4.0 \text{ V}$ to 5.5 V

*2 : $V_{CC} = 2.7 \text{ V}$ to 4.0 V

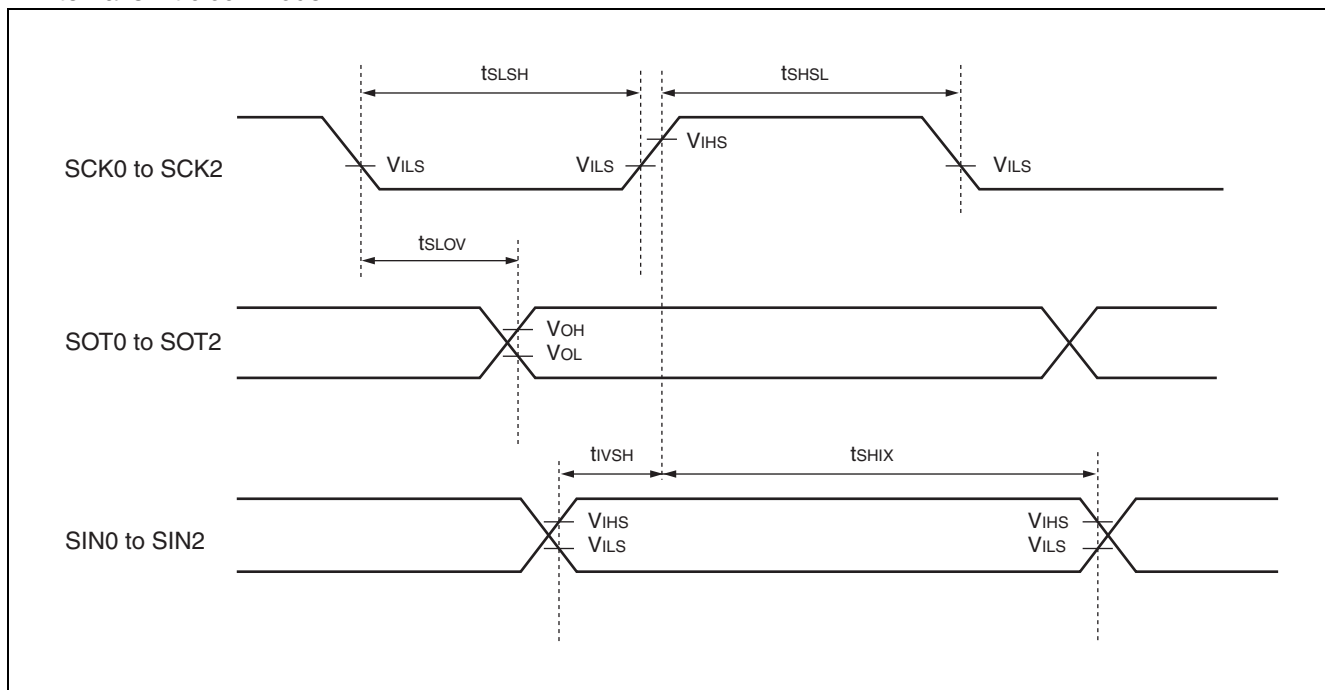
Notes : • The above ratings are the AC characteristics for CLK synchronous mode.
• t_{CYCP} indicates the peripheral clock cycle time.

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• Internal shift clock mode



• External shift clock mode



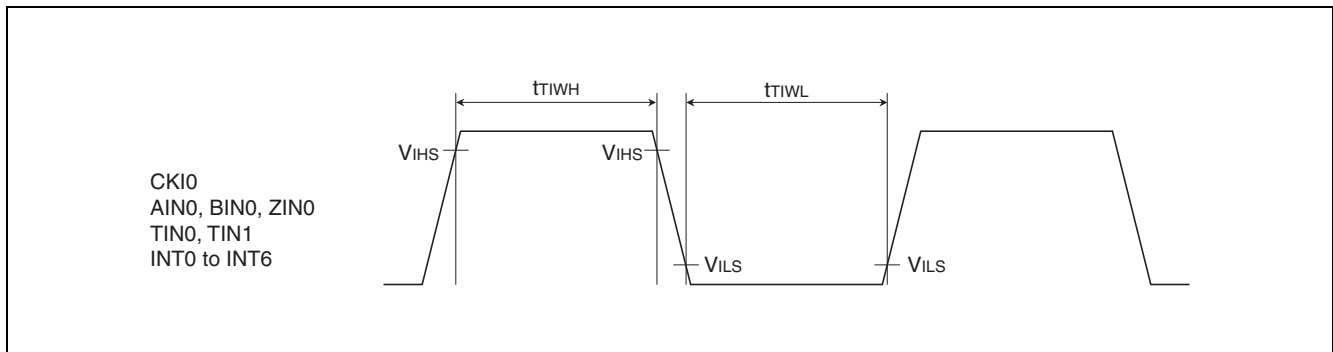
(6) Free-run Timer Clock, Up/Down Counter, Base Timer, and External Interrupt Input Timing

($V_{CC} = 2.7 \text{ V}$ to 5.5 V , $V_{SS} = AVSS10 = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
Free-run timer input clock pulse width	t_{TIWH} t_{TIWL}	CKI0	—	$4 \times t_{CYCP}$	—	ns
Up-down counter input pulse width		AIN0 BIN0 ZIN0		$4 \times t_{CYCP}$	—	ns
Base timer input pulse width		TIN0, TIN1		$4 \times t_{CYCP}$	—	ns
External interrupt input pulse width		INT0 to INT6		$4 \times t_{CYCP}$	—	ns
				1.0*	—	μs

* : In stop mode

Note : t_{CYCP} indicates the peripheral clock cycle time.



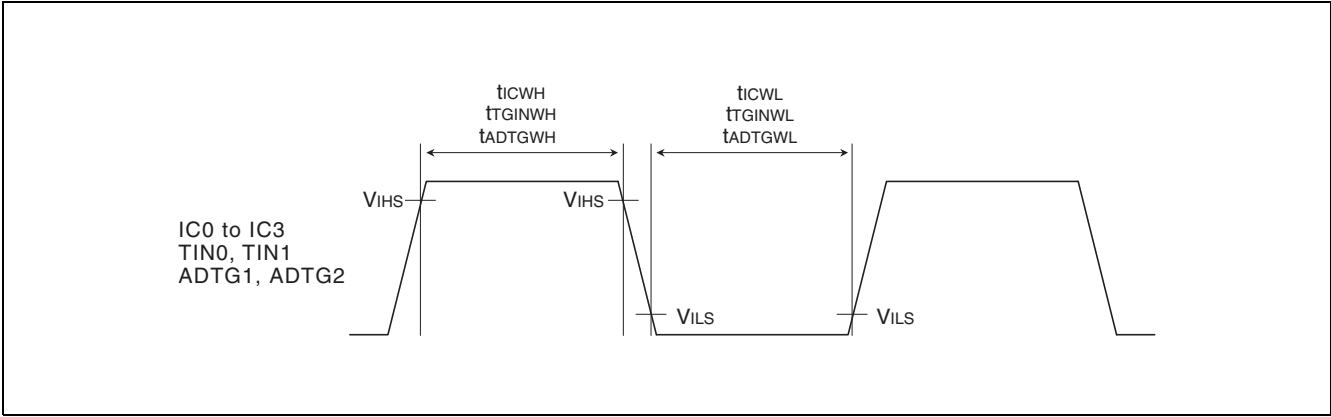
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(7) Trigger Input Timing

($V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $V_{SS} = AVSS10 = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
Input Capture trigger input	t_{ICWH} t_{ICWL}	IC0 to IC3	—	$5 \times t_{CYCP}$	—	ns
Base timer trigger input	t_{TGINWH} t_{TGINWL}	TIN0, TIN1		$4 \times t_{CYCP}$	—	ns
A/D activation trigger input	t_{ADTGWH} t_{ADTGWL}	ADTG1, ADTG2		$5 \times t_{CYCP}$	—	ns

Note : t_{CYCP} indicates the peripheral clock cycle time.



(8) I²C Timing

a. Master Mode

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = AVSS10 = 0.0 V, T_A = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Standard Mode		Fast Mode*3		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f _{SCL}	SDAn, SCLn	R=1 kΩ, C=50 pF*4	0	100	0	400	kHz	
"L" width of the SCL clock	t _{LOW}			4.7	—	1.3	—	μs	
"H" width of the SCL clock	t _{HIGH}			4.0	—	0.6	—	μs	
Bus free time between STOP and START conditions	t _{BUS}			4.7	—	1.3	—	μs	
SCL↓→SDA output delay time	t _{DL DAT}			—	5 × t _{CYCP} *1	—	5 × t _{CYCP} *1	ns	
Setup time for a repeated START condition SCL↑→SDA↓	t _{SUSTA}			4.7	—	0.6	—	μs	
Hold time for a repeated START condition SDA↓→SCL↓	t _{HDSTA}			4.0	—	0.6	—	μs	The first clock pulse is generated after this.
Setup time for STOP condition SCL↑→SDA↑	t _{SUSTO}			4.0	—	0.6	—	μs	
SDA Data input hold time (vs. SCL↓)	t _{HDDAT}			2 × t _{CYCP} *1	—	2 × t _{CYCP} *1	—	μs	
SDA Data input setup time (vs. SCL↑)	t _{SUDAT}			250	—	100 *2	—	ns	

*1 : t_{CYCP} indicates the peripheral clock cycle time.

*2 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement

t_{SUDAT} ≥ 250 ns must then be met.

If a device does not extend the "L" period of the SCL signal, it is necessary to output the next piece of data to the SDA line 1250 ns (SDA and SCL rising Max time + t_{SUDAT}) before the SCL line is released.

*3 : For use at over 100 kHz, set the peripheral clock to at least 6 MHz.

*4 : R and C are the pull-up resistance and load capacitance of the SCL and SDA lines.

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b. Slave Mode

($V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $V_{SS} = AVSS10 = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Standard Mode		Fast Mode*3		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SDAn, SCLn	$R=1 \text{ k}\Omega$, $C=50 \text{ pF}^{*4}$	0	100	0	400	kHz	
“L” width of the SCL clock	t_{LOW}			4.7	—	1.3	—	μs	
“H” width of the SCL clock	t_{HIGH}			4.0	—	0.6	—	μs	
Bus free time between STOP and START conditions	t_{BUS}			4.7	—	1.3	—	μs	
SCL $\downarrow \rightarrow$ SDA output delay time	t_{DLAT}			—	$5 \times t_{CYCP}^{*1}$	—	$5 \times t_{CYCP}^{*1}$	ns	
Setup time for a repeated START condition SCL $\uparrow \rightarrow$ SDA $\downarrow$	t_{SUSTA}			4.7	—	0.6	—	μs	
Hold time for a repeated START condition SDA $\downarrow \rightarrow$ SCL $\downarrow$	t_{HDSTA}			4.0	—	0.6	—	μs	The first clock pulse is generated after this.
Setup time for STOP condition SCL $\uparrow \rightarrow$ SDA $\uparrow$	t_{SUSTO}			4.0	—	0.6	—	μs	
SDA Data input hold time (vs. SCL $\downarrow$)	t_{HDDAT}			$2 \times t_{CYCP}^{*1}$	—	$2 \times t_{CYCP}^{*1}$	—	μs	
SDA Data input setup time (vs. SCL $\uparrow$)	t_{SUDAT}			250	—	100 ^{*2}	—	ns	

*1 : t_{CYCP} indicates the peripheral clock cycle time.

*2 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SUDAT} \geq 250 \text{ ns}$ must then be met.

If a device does not extend the “L” period of the SCL signal, it is necessary to output the next piece of data to the SDA line 1250 ns (SDA and SCL rising Max time + t_{SUDAT}) before the SCL line is released.

*3 : For use at over 100 kHz, set the peripheral clock to at least 6 MHz.

*4 : R and C are pull-up resistance and load capacitance of the SCL and SDA lines.

6. Electrical Characteristics for the A/D Converter

(1) 8/10-bit A/D Converter

($V_{CC} = 4.0 \text{ V to } 5.5 \text{ V}$, $AVRH2 = 4.0 \text{ V to } 5.5 \text{ V}$, $V_{SS} = AVSS10 = 0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	− 4	—	+ 4	LSB	When $AVRH2 = 5.0 \text{ V}$
Linearity error	—	—	− 3.5	—	+ 3.5	LSB	
Differential linearity error	—	—	− 3	—	+ 3	LSB	
Zero transition voltage	V_{OT}	AN1-0 to AN1-3 AN2-0 to AN2-7	$AVSS10-3.5$	$AVSS10+0.5$	$AVSS10+4.5$	LSB	
Full-scale transition voltage	V_{FST}	AN1-0 to AN1-3 AN2-0 to AN2-7	$AVRH2-5.5$	$AVRH2-1.5$	$AVRH2+2.5$	LSB	
Conversion time*1	—	—	1.2	—	—	μs	
Analog port input current	I_{AIN}	AN1-0 to AN1-3 AN2-0 to AN2-7	—	—	10	μA	
Analog input voltage	V_{AIN}	AN1-0 to AN1-3 AN2-0 to AN2-7	$AVSS10$	—	$AVRH2$	V	
Reference voltage	—	$AVRH2$	$AVSS10$	—	$AVCC10$	V	
Power supply current (Analog + digital)	I_A	$AVCC10$	—	2	5	mA	For each 1 unit
	I_{AH}^{*2}	$AVCC10$	—	—	5	μA	
Reference voltage supply current (between $AVRH2$ and $AVSS$)	I_R	$AVRH2$	—	1	2.5	mA	For each 1 unit, at $AVRH2 = 5.0 \text{ V}$ $AVSS10 = 0 \text{ V}$
	I_{RH}^{*2}	$AVRH2$	—	—	5	μA	For each 1 unit, at stop mode
Analog input capacitance	—	—	—	—	12.5	pF	
Interchannel disparity	—	AN1-0 to AN1-3 AN2-0 to AN2-7	—	—	4	LSB	

*1 : When $V_{CC} = AVCC10 = 5.0 \text{ V}$ and peripheral clock = 33 MHz

*2 : The current when the CPU is in stop mode and the A/D converter is not operating (at $V_{CC} = AVCC10 = AVRH2 = 5.0 \text{ V}$) .

Notes : • The above figures do not guarantee the accuracy between each unit.

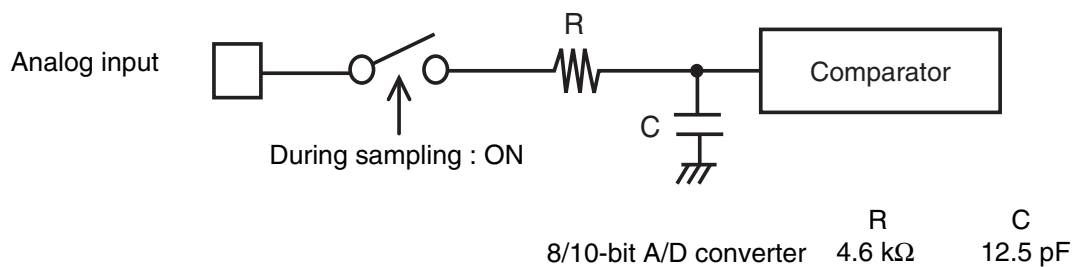
• Output impedance of the external circuit $\leq 2 \text{ k}\Omega$.

• The result of 8/10 bit A/D conversion is not guaranteed at the voltage of $V_{CC} = 2.7 \text{ V to } 4.0 \text{ V}$.

• External impedance and sampling time of analog inputs

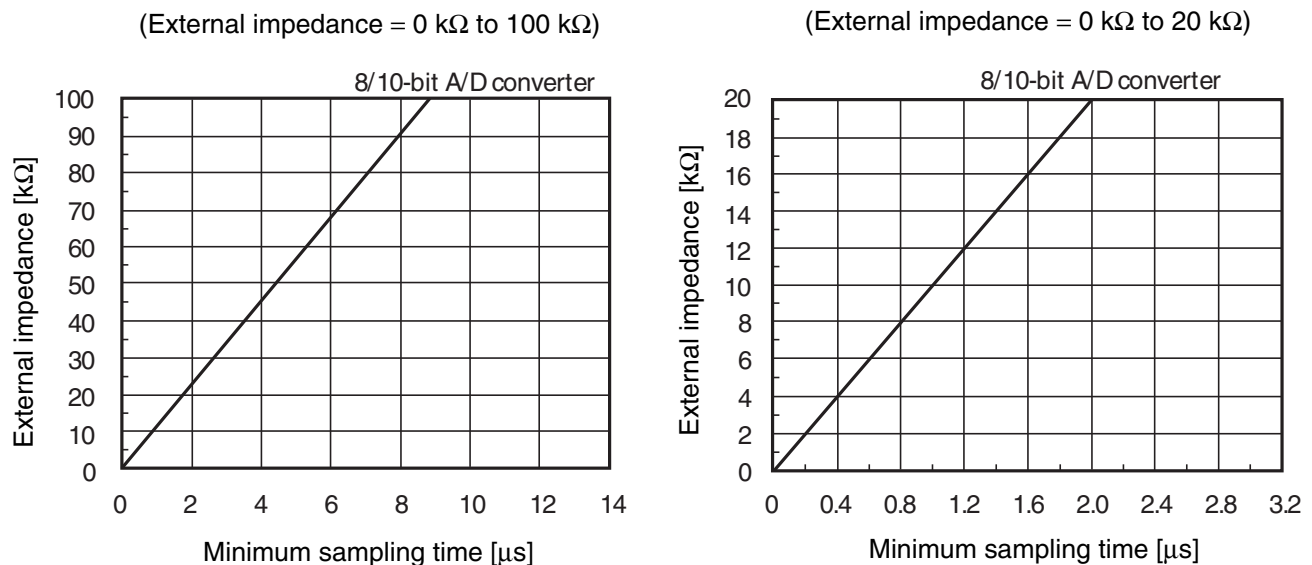
- The A/D converter is fitted with a sample and hold circuit. If the external impedance is so high that there is not sufficient time for sampling, the internal sample and hold capacitor will not fully charge to the analog voltage, and the precision of the A/D conversion will be adversely affected. Therefore, in order to satisfy the A/D conversion precision specifications, either adjust the register values and operating frequency or reduce the external impedance so that the sampling time is greater than the minimum value as given by the relationship between external impedance and minimum sampling time. If you are still unable to hold enough sampling time, connect a capacitor of about 0.1 μF to the analog input pin.

• Analog input circuit schematic



Note : The values are reference values.

• The relationship between the external impedance and minimum sampling time

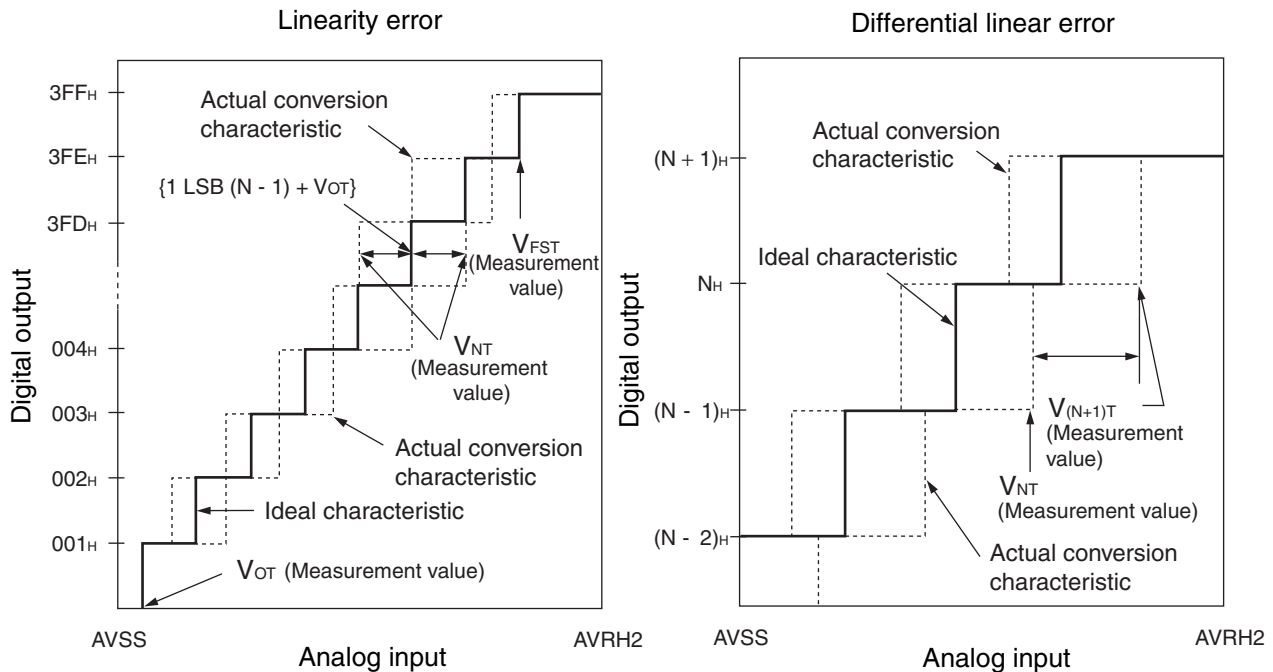


• About errors

- The relative error increases as the value of $|\text{AVRH2} - \text{AVSS}|$ decreases.

• Definition of 8/10-bit A/D Converter Terms

- Resolution : Analog variation that is recognized by the A/D converter.
- Linearity error : Deviation between the line connecting zero transition point (0000000000←→0000000001) and full-scale transition point (1111111110←→1111111111) and actual conversion characteristics.
- Differential linear error : Deviation from the ideal value of input voltage necessary to change the output code by 1LSB.
- Total Error : This error is the difference between actual and ideal values, including the zero transition error/full-scale transition error/linearity error.



$$\text{Linear error in digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$\text{Differential linear error in digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \text{ [LSB]}$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022}$$

N : A/D converter digital output value

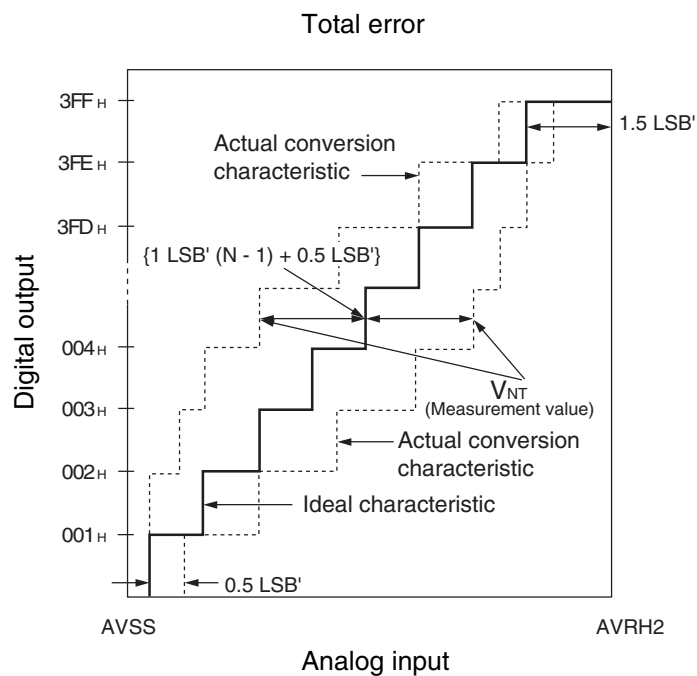
V_{OT} : Voltage at which digital output changes from 000_H to 001_H.

V_{FST} : Voltage at which digital output changes from 3FE_H to 3FF_H.

V_{NT} : Voltage at which digital output changes from (N - 1)_H to N_H.

(Continued)

(Continued)



$$1 \text{ LSB}' (\text{ideal value}) = \frac{\text{AVRH2} - \text{AVSS}}{1024} [\text{V}]$$

$$\text{Total error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB}' \times (N - 1) + 0.5 \text{ LSB}'\}}{1 \text{ LSB}'}$$

N : A/D converter digital output value

V_{NT} : Voltage at which digital output changes from $(N + 1)_H$ to N_H .

V_{OT}' (ideal value) = $\text{AVSS} + 0.5 \text{ LSB}'$ [V]

V_{FST}' (ideal value) = $\text{AVRH2} - 1.5 \text{ LSB}'$ [V]

7. Low Voltage Detection Interrupt / Reset Electrical Characteristics

a. Low Voltage Detection Interrupt

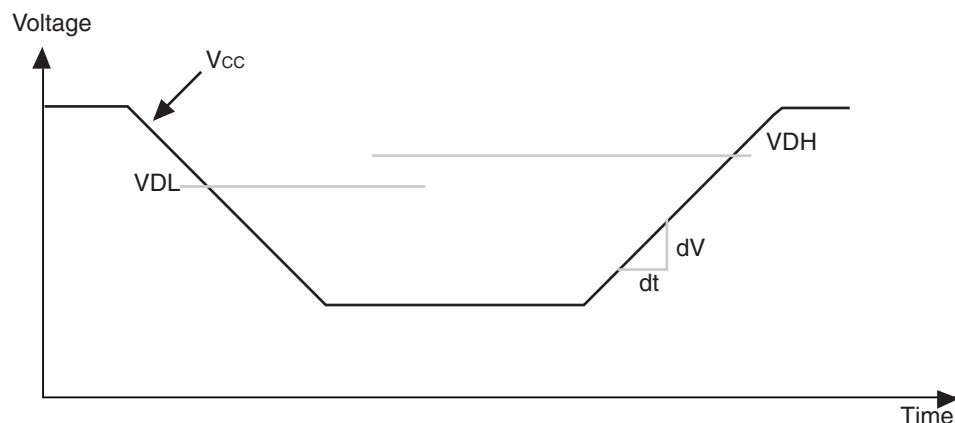
($T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Detect voltage	VDL	VCC	3.40	3.70	4.00	V	When voltage drops
Release voltage	VDH	VCC	3.45	3.75	4.05	V	When voltage rises
Power supply voltage changing rate	$ dV/dt $	VCC	—	—	0.004	V/ μs	Value which detect voltage (VDL) and release voltage (VDH) are guaranteed within each spec.

b. Low Voltage Detection Reset

($T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Detect voltage	VDL	VCC	2.76	3.00	3.24	V	When voltage drops
Release voltage	VDH	VCC	2.81	3.05	3.29	V	When voltage rises
Power supply voltage changing rate	$ dV/dt $	VCC	—	—	0.004	V/ μs	Value which detect voltage (VDL) and release voltage (VDH) are guaranteed within each spec.

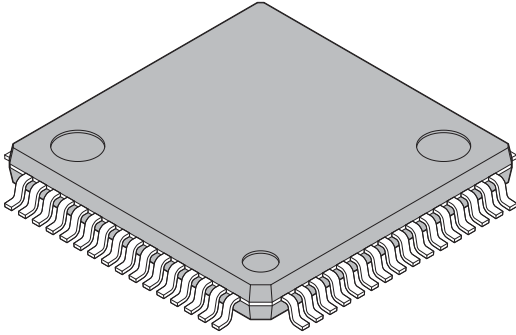


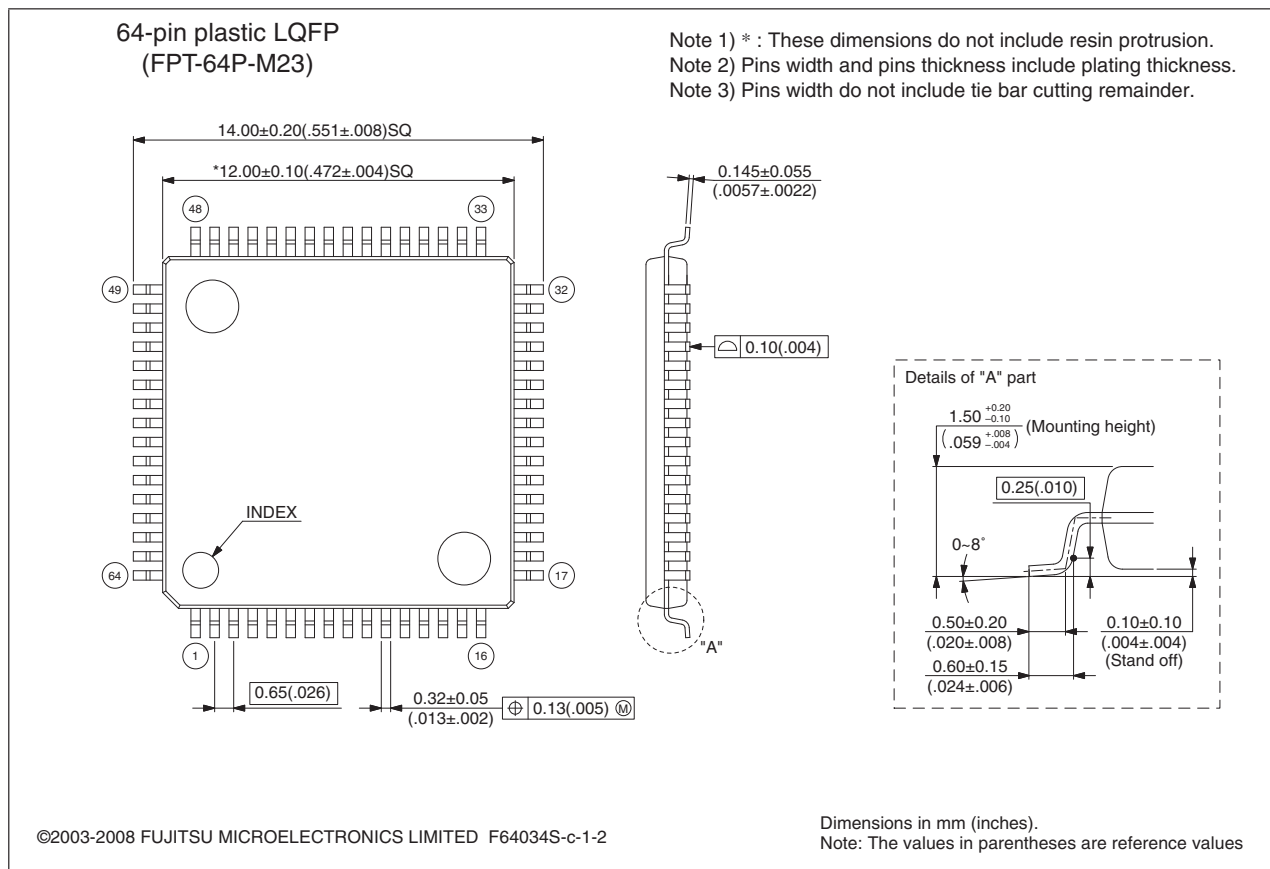
MB91490 Series

■ ORDERING INFORMATION

Part No.	Package
MB91F492PMC-GE1	64-pin plastic LQFP (FPT-64P-M23)
MB91F492PMC1-GE1	64-pin plastic LQFP (FPT-64P-M24)

■ PACKAGE DIMENSIONS

64-pin plastic LQFP  (FPT-64P-M23)	Lead pitch	0.65 mm
	Package width × package length	12.0 × 12.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Code (Reference)	P-LFQFP64-12×12-0.65

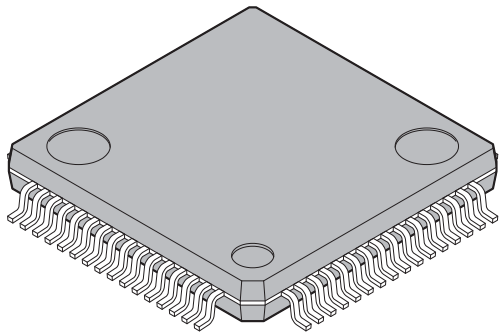


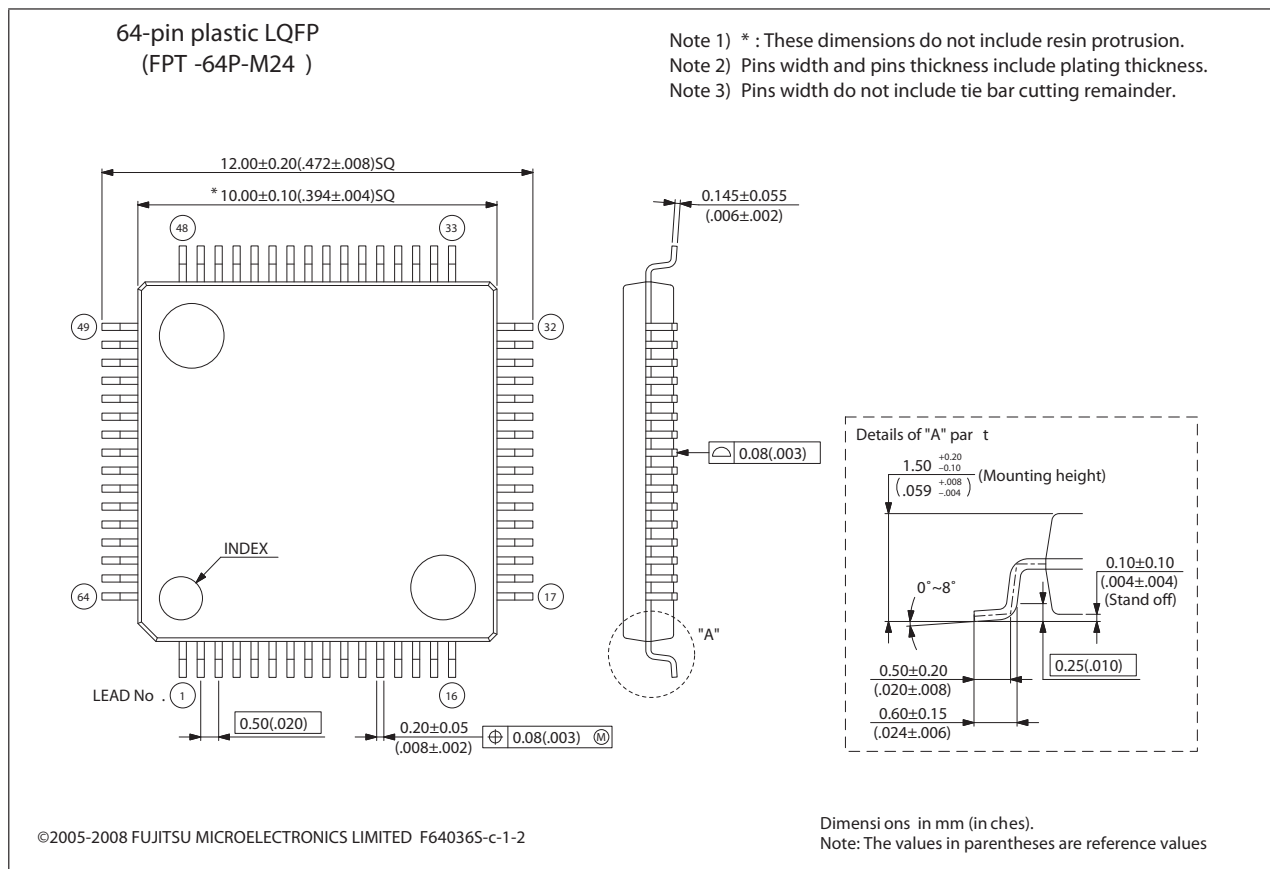
Please check the latest package dimension at the following URL.
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MB91490 Series

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64-pin plastic LQFP  (FPT -64P-M24)	Lead pitch	0.50 mm
	Package width × package length	10.0 × 10.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32 g
	Code (Reference)	P-LFQFP64-10×10-0.50



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MEMO

MB91490 Series

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