Intel® GW80314 I/O Companion Chip

Datasheet

Product Features

- Companion chip for the Intel® 80200 processor based on Intel XScale® microarchitecture (ARM* architecture compliant—no integrated core)
- Internal non-blocking, high-speed switch fabric
- Two embedded PCI-X ports
- Intel® 80200 processor interface supporting up to two processors with low-latency path to the SDRAM.
- Two 10/100/1000 Mbit Ethernet controllers providing descriptor-based access to or from any internal port including SDRAM
- SDR/DDR SDRAM controller with data queueing to allow the increased performance of DDR memory
- OpenPIC-based multi-function interrupt controller (MPIC)
- Peripheral Bus Interface providing a generic parallel port, access to flash, and access to other types of external memory
- Two 16550-compatible UARTs with 16-byte transmit and receive FIFOs
- I^2C two-wire interface for initial configuration or saving vital product data
- 1 MB of internal high-speed static RAM for higher-speed access.

Order Number: 273757-003US
November 2004

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Revision History

Date	Revision	Description
November 2004	003	Changed maximum operation temperature from 105° to 85° in Section 3.2 Removed Thermal Parameters 1 and 3 from Section 3.2.1 Removed a portion of Environmental Conditions information and Thermal Data information from Table 22. Removed Section 3.2.2, Ambient Temperature. Removed Section 3.2.4, Thermal Resistance. Updated Case Temperature Maximum Rating in Table 26. Removed Ambient Temperature information from Table 27.
June 2004	002	Updated for B1 stepping.
September 2003	001	Initial document.

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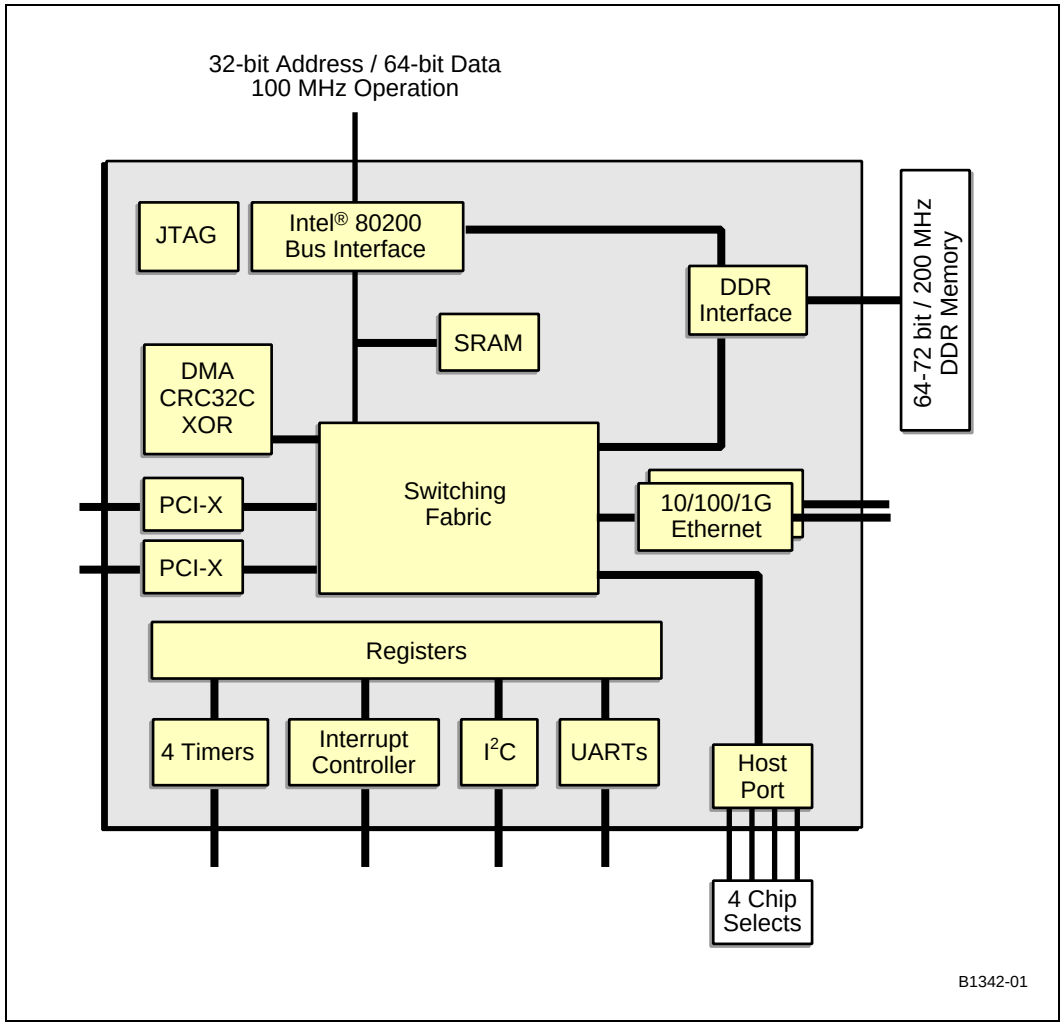
1.0 Introduction

This is the *Intel® GW80314 I/O Processor Datasheet*. This document contains a functional overview, package signal locations, targeted electrical specifications, and bus functional waveforms. Detailed functional descriptions other than parametric performance are published in the *Intel® GW80314 I/O Processor Developer Manual*.

Figure 1 shows a block diagram.

Figure 1. Intel® GW80314 I/O Processor Block Diagram



This bridge is designed as a fabric centric, any-port-to-any-port bridge. All transactions are placed into fabric packets and routed via address-based port selection to another fabric port. The bridge is based on the “store and forward” concept, where transactions are buffered at the incoming port. When a packet is complete, the incoming port knows the size of the packet, and it can be burst across the fabric to the outgoing port. As the timing of the packet is deterministic at the outgoing port, the transaction can be started at the outgoing port as soon as the header arrives. All outgoing

ports can buffer incoming packets to allow for delayed access to the external bus. To limit the latency and to provide a certain quality of service, the internal packets are limited to 256 bytes in size. Larger PCI transactions are broken into 256-byte transactions at the PCI port.

1.1 Terminology

The following terms are used in this document.

Table 1. Terms and Acronyms

Term/Acronym	Description
BAR	PCI-X Base Address Register
DMA	Direct Memory Address
Embedded	Configuration causing the PCI-X block to provide BARs and address translation mechanism to PCI-X
G/MII	Gigabit Media Independent Interface
LVTTL	Low-Voltage Transistor-Transistor Logic
MAC	Media Access Controller
MIB	Management Information Base
PCI	Transfers, interfaces or logic that are *PCI Local Bus Specification,* Revision 2.3 compatible
PCI/X	Used to signify either/or PCI or PCI-X designation.
PCI-X	Transfers, interfaces or logic that may be either *PCI Local Bus Specification,* Revision 2.3 or *PCI-X Addendum to the PCI Local Bus Specification,* Revision 1.0a compatible
PHY	Physical connection device
PMA	Physical Media Attachment
PMD	Physical Media Device
Primary	A device with the PCI port attached to the processor bus side in a homogeneous, transparent system.
RMON	Remote Monitoring
RX	Receiver
Secondary	A device with the PCI port not attached to the host processor in a homogeneous, transparent system.
SNMP	Simple Network Management Protocol
STTL	Schottky Transistor-Transistor Logic
TBI	Ten-Bit Interface
Transparent	Configuration causing the PCI/X block to use base and limit registers for PCI-X side addressing.
TX	Transmitter
VLAN	Virtual Local Area Network

1.2 Other Relevant Documents

Table 2. Related Documentation

Document Title	Document# / Contact
Intel® 80312 I/O Companion Chip Developer's Manual	273410
Intel® 80312 I/O Companion Chip Specification Update	273416
Intel® 80200 Processor based on Intel XScale® Microarchitecture Developer's Manual	273411
Intel® 80310 I/O Processor Chipset with Intel XScale® Microarchitecture Design Guide	273354
Intel® 80200 Processor based on Intel XScale® Microarchitecture Datasheet	273414
Intel® 80200 Processor based on Intel XScale® Microarchitecture Specification Update	273415
PCI Local Bus Specification, Revision 2.2	PCI Special Interest Group 1-800-433-5177 http://www.pcisig.com/home
PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a	
PCI-to-PCI Bridge Architecture Specification, Revision 1.1	
PCI System Design Guide, Revision 1.0	
PCI Hot-Plug Specification, Revision 1.0	
PCI Bus Power Management Interface Specification, Revision 1.1	
OpenPIC Specification Revision 1.2	
I^2C Peripherals for Microcontrollers	Philips Semiconductors http://www.semiconductors.philips.com/buses/i2c/
Advanced Configuration and Power Interface Specification, Revision 1.0 (ACPI)	http://www.acpi.info/spec10b.htm

NOTE: Also see the Intel® product website at http://developer.intel.com/design/iio/.

2.0 Features

The Intel® GW80314 I/O Processor (GW80314) is an I/O companion chip for the Intel® 80200 processor (80200) with an intelligent PCI-X bridge and Gigabit Ethernet access.

2.1 Switch Fabric Unit

The purpose of the Switch Fabric Network (SFN) is to provide an interconnect fabric that is useful for on-chip communications between the blocks within the GW80314.

The Switch Fabric Unit includes the following features:

- High-performance interconnect fabric for communication between GW80314 blocks
- Consistent port definition that is independent of the fabric implementation
- Protocol independent of fabric pipeline depth
- Three transaction flows using four priority levels
- 64-bit local address
- Four or six deep 256-byte transaction queues (1 K for PCI-X and SDRAM) (mode dependent)
- Port addressing supports up to 16 SFN ports

2.2 PCI-X Interface

The PCI/X block provides an interface to the SFN (internal switch fabric). It is able to convey transactions from the internal SFN fabric to a PCI/X bus and transactions from a PCI/X bus to the internal switch fabric. The PCI/X block also has the capability to tunnel through the SFN fabric to the other PCI/X block on the fabric providing a pseudo-transparent PCI-to-PCI bridge. This capability is available in the GW80314 as two separate PCI/X blocks are integrated.

The PCI-X block provides the following functions:

- 64-bit capable PCI/X interface
- Secondary PCI arbiter
- CompactPCI Hot Swap controller
- Control and status registers

2.3 CIU Interface

The Intel® 80200 processor (80200) bus Core Interface Unit (CIU) provides a bridge between the 80200 bus and the Switch Fabric, an SDRAM controller, and 1 MB of on chip SRAM. It has a queuing mechanism to store requests from up to two 80200s. The requests from a given 80200 are completed on the 80200 bus in the order in which they are received. The CIU has the following features:

- Up to two 80200 on the processor bus
- Up to four read or write requests from each processor
- Strict ordering rules for each processor
- Optional ECC for Processor Bus Data
- Up to four base address registers for the switch fabric
- Configurable software reset for the CIU and 80200 processors on startup
- Configurable with and without 1 Mbyte embedded SRAM
- Reset output for 80200 processors
- One base address register for the 1 MB on-chip SRAM
- Switch fabric access to SRAM
- 64-bit aligned data words
- 32-bit address decode
- 80200 external bus ECC protection
- Two-cycle wait states for write transactions to the SRAM from the processor bus
- Three-cycle wait states for read transactions to the SRAM from the processor bus

The CIU does not have the following features:

- Locked transactions
- Strict ordering rules between processors

2.4 SDRAM Controller

The SDRAM Controller Core provides an interface to single and double data rate SDRAM. The SDRAM Controller Core has the following features

- Synchronous SDRAM interface for PC100, PC200, and PC1600
- Two-port (64-bit data, 36-bit address) concurrent access to memory
- Internal arbiter with programmable priority for each port
- One-port (32-bit data, 18-bit address) access to registers
- Supports up to four physical (eight logical) banks
- Supports up to 32 bank interleaving (i.e., 32 pages open simultaneously)
- Flexible row and column address
- Optional ECC (single-bit error correction, multi-bit error detection)
- I/O interface compatible with DDR SDRAM
- I^2C master only interface for DIMM detection
- Digital DLL for automatic DQS timing recovery

2.5 DMA/XOR Engine

The DMA/XOR engine has four identical channels operating independently. Each channel can function as a DMA engine or as an XOR engine. As a DMA engine, it can transfer data from any port to any port and provide CRC calculation on the transferred data. As an XOR engine, it can perform XOR operations on multiple blocks of data, memory fill operation, and parity checking operation. For the DMA data transfer and XOR operation, a channel can be configured to operate in Direct Mode (single operation) or Linked-List mode (multiple operations by stepping through a linked series of Command Packets in external memory).

This DMA/XOR engine supports unaligned data transfers. The alignment or unalignment of data is the responsibility of the DMA/XOR engine. The DMA/XOR registers specify the source, destination, command packet address, mode of operation, the type of mapping to achieve the proper byte alignment, and the byte count for a transaction. Note that the maximum byte count is 16 Mbytes. All DMA operations are assumed to be to prefetchable memory.

The DMA/XOR Engine has the following features:

- Four-channel support. Each channel operates independently.
- Data transfer to and from any port as a DMA engine
- XOR operation, memory fill, and parity checking as an XOR engine
- Scatter gather (or Linked-List) and direct modes
- XOR operation of up to 16 blocks of data
- Directly fill the store queue with the first block of XOR data (optional)
- Interrupt on completed segment, chain, and error
- Mode-selectable byte alignment on transferred data
- Calculate CRC on the DMA transferred data based on the CRC-32C algorithm required by the *iSCSI Specification*
- Pipeline read requests or read and write requests for better performance
- Go/stop/halt control of data transfer operation

2.6 Gigabit Ethernet (GigE) Interface

The Ethernet block is made up of four major sub-blocks. It includes two Gigabit Ethernet interfaces, E0 and E1. There is a single management interface to manage the two PHY devices. Each Ethernet interface has its own statistics monitor that tracks and reports key interface statistics. Each ethernet interface supports a 256-entry hash table for address filtering. Each Ethernet interface is bridged to the SFN interface domain through a 2K byte transmit FIFO and a 4K byte Receive FIFO. There are four independent DMA engines to support transmit and receive data flows for both Ethernet interfaces. The DMA engines rely on descriptors set up in memory, the memory map of the device, and are accessed through the SFN interface. The DMA arbiter handles arbitration for the SFN interface. A register bus interface is provided for the register access and status monitor control.

The GigE interface has the following features:

- Full support for 10/100/1000 Mbits/s Ethernet standards IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac
- Full/half-duplex support at 10/100 Mbits/s, full-duplex only Gigabit Ethernet support
- MAC Control Sublayer w/PAUSE, extended OPCODE support
- MII Management with suppressed preamble, sequential cycle, variable clock features
- 8-bit MAC engine optimized for size, reduced latency
- Optional half-duplex back-pressure (10/100 Mbits/s only)
- Hash table support for packet filtering
- VLAN packet filtering support
- Standard register read/write interface
- 2K/4K transmit/receive FIFOs for data flow synchronization
- Two independent DMA channels per Ethernet port: one transmit and one receive
- Four transmit priority descriptor queues controlled via transmit priority tagging
- Four receive priority descriptor queues controlled by receive packet filtering priority
- Collisions detect and retransmit error handling
- PHY management interface
- Statistics monitoring and logging: support for RMON MIB group 1, RMON MIB group 2 if table counters, RMON MIB group3, RMON MIB group 9, RMON MIB 2, and the dot 3 Ethernet MIB

2.7 Interrupt Controller

The interrupt controller is a programmable, register based, and multiple port design that meets *OpenPIC Specification,* Revision 1.2.

The interrupt controller has the following features:

- Support for two Intel® 80200 processors
- Sixteen interrupt priority levels (0 to 15)
- Level/edge sensibility programmable for 24 IRQ inputs
- Level/edge sensibility programmable for four output pins
- Up to 24 input interrupt pins
- Up to four output interrupt pins
- Four doorbell registers for additional interrupts
- Four general-purpose mailbox registers
- Four global precision timers
- All registers are read/write 32 bits based
- Multiple delivery modes are supported:
  - Directed-single destination
  - Directed-multicast
  - Distributed-multiple destination
- Nesting of interrupt events
- Spurious vector generation capable
- Soft set override for all input sources (maximum 24)
- Processor initialization registers
- All registers are at “Known Reset State” on power-up

2.8 General Purpose I/O (GPIO) Block

The GPIO block contains the general purpose I/O functions available in the GW80314. They include:

- Two 16450-compatible UARTs with 16-byte incoming and 16-byte outgoing FIFOs
- One general-purpose I^2C interface port used for initialization and storing of PCI VPD data
- One 8-bit general-purpose parallel I/O port (shared with UART pins)
- One configurable 8-, 16-, or 32-bit Peripheral Bus Interface for interfacing to external SRAM/ROM

All the interfaces are configurable via the internal configuration bus.

3.0 Package Information

3.1 Package Introduction

The GW80314 is offered in a 1025-lead HSBGA (Heat Slug Ball Grid Array) thermally enhanced package. This is a perimeter array package with 904 ball connections in the outer area of the package and a square 11x11 grid of ball connections in the middle area of the package. See Figure 2 “1025-Lead HSBGA Package Drawing” on page 41.

3.1.1 Functional Signal Definitions

Signals are classified according to the types defined in Table 3.

Table 3. Signal Type Definitions

Signal Type	Definition
I	Standard input only signal.
IO	Standard tristate input/output
I(PD)	Standard input only signal with internal Pull Down.
I(PU)	Standard input only signal with internal Pull Up.
AI	Analog Input Signal
O	Standard output only signal.
OD	Open drain output that allows multiple devices to share as a wire-OR
TO	Standard tristate output only signal.
TIO	Standard tristate input/output signal.
IO(OD)	Open drain input/output that allows multiple devices to share as a wire-OR when it is used as output.
S	Supply Pin, either a V_{CC} or V_{SS}.

3.1.2 Intel XScale® Microprocessor Bus Signals

This section describes the GW80314 Intel XScale® microprocessor signals which are 3.3 V LVTTL compatible.

Table 4. Intel XScale® Microprocessor Bus Signals

Pin Name	Count	Pin Type	Description
XS_A[15:0]	16	I	Address: During the first cycle of the issue phase, it carries the upper 16 bits of the address for the access. During the second cycle of the issues phase, it carries the lower 16 bits of the address.
XS_ABORT	1	O	Transaction Abort: Indicates the next transaction on the data bus is aborted.
XS_BE[7:0]	8	IO	Processor Bus Byte Enables.
XS_CLK	1	IO	Intel XScale® microprocessor bus clock: Output clock for Intel XScale® microprocessor interface and SDRAM controller. This pin acts as an input in Scan Mode.
XS_CWF/ DBuswidth	1	O	Critical word first: Indicates the order in which the current 32-byte read burst is returning. Also when the Intel XScale® microprocessor bus is in reset this signal is driven low to indicated data bus width is 64-bit.
XS_DQ[63:0]	64	IO	Data bus.
XS_DVALID[1:0]	2	O	Data Valid: One for each Intel XScale® microprocessor on the bus. When asserted high, it indicates that two cycles later, data is valid on XS_DQ, XS_BE, and XS_ECC.
XS_HOLD[1:0]	2	O	Signal to Intel XScale® microprocessor to request Intel XScale® microprocessor to release the Intel XScale® microprocessor bus.
XS_HLDA[1:0][1]	2	I	Signal from Intel XScale® microprocessor to acknowledge the release of the Intel XScale® microprocessor bus in response to the assertion of the corresponding XS_HOLD signal.
XS_ECC[7:0]	8	IO	Data Check Bits for Intel XScale® microprocessor ECC Bus Protect.
XS_FIQ[1]/PWRUP_SD_BYP (Configuration Pin)	1	IO	Interrupt: indicates a fast interrupt to processor 1. During power-up, this pin is latched at the rising edge of reset and used to enable the SDRAM PLL bypass mode when latched high.
XS_FIQ[0]	1	O	Interrupt: indicates a fast interrupt to processor 0.
XS_IRQ[1]/ PWRUP_XS_BYP (Configuration Pin)	1	IO	Interrupt: indicates a interrupt to processor 1. During power-up, this pin is latched at the rising edge of reset and is used to enable the Intel XScale® microprocessor PLL bypass mode when latched high.
XS_IRQ[0]/ PWRUP_FADJ Configuration Pin	1	IO	Interrupt: indicates a interrupt to processor 0. During power-up, this pin is used to program Intel XScale® microprocessor PLL frequency adjust logic. • PWRUP_FADJ = 0, Intel XScale® PLL Frequency = 3/4 * SFN_CLK. • PWRUP_FADJ = 1, Intel XScale® PLL Frequency = SFN_CLK.
XS_LEN[2:0]	3	I	Control and length access: During the first cycle of the issue phase: • XS_LEN[2] (ADS#) the start of a bus request. • XS_LEN[0] (W/R#) indicates whether the current request is a read (XS_LEN[0] = 0) or a write (XS_LEN[0] =1). During the second cycle of the issue phase: • XS_LEN[2:0] indicates the length of the request.
XS_RESET#	1	O	Reset pin: When output is low the Intel XScale® microprocessor bus is reset and Intel XScale® microprocessor interface is in reset.
Intel XScale® microprocessor Pin Count	113		

NOTES:
1. For single processor configuration, XS_HLDA[0] should be tied low and XS_HLDA[1] should be tied high.

3.1.3 SDRAM Controller Signals

This section describes signals for the GW80314 SDRAM controller. Signals in this group are SSTL compatible.

Table 5. SDRAM Signals

Pin Name	Count	Pin Type	Description
SD_A[13:0]	14	TO	Address: Address and command bus
SD_BA[1:0]	2	TO	Bank Address**:** Indicates to which bank an Active, Read, Write, or Precharge command is being applied.
SD_CAS#	1	TO	Column Address Strobe**:** SD_CAS#, SD_RAS#, and SD_WE# identify the command being sent to the DRAM devices.
SD_CLK[3:0]	4	TO	Clock Out: Clock outputs for SDRAM DIMMs. All address and control signals are valid on the positive edge of SD_CLK.
SD_CLK#[3:0]	4	TO	Clock Out Inverted: Clock outputs for SDRAM DIMMs
SD_CLKEN	1	TO	Clock Enable
SD_CKFBI	1	I	DDR SDRAM system flight time removal feedback input.
SD_CKFBO	1	TO	DDR SDRAM system flight time removal feedback output.
SD_CS#[7:0]	8	TO	Chip Select: Enable indicating the command on SD_CAS#, SD_RAS#, and SD_WE# is valid.
SD_DQ[63:0]	64	IO	Data Bus: Output with write to RAM, and input with read from RAM.
SD_DQS/DM[17:9]	9	IO	High Data Strobe/Data Mask: Output with write to RAM, and input with read from RAM. Edge-aligned with read data, and center-aligned with write data. Used as Data Mask bits in 8-bit/16-bit wide RAM DDR systems that require only 9 strobes.
SD_DQS[8]	1	IO	Low ECC Data Strobe: Output with write to RAM, and input with read from RAM. Edge-aligned with read data, and center-aligned with write data.
SD_DQS[7:0]	8	IO	Low Data Strobe: Output with write to RAM, and input with read from RAM. Edge-aligned with read data, and center-aligned with write data.
SD_ECC/DM[7:0]	8	IO	ECC: Indicates which bytes on a write are to be updated or the error detection and correction bits.
SD_I2C_CLK	1	OD	Serial Clock: EEPROM Serial clock for serial DIMM recognition. Internally pulled high.
SD_I2C_SDA	1	IO(OD)	Serial Data: EEPROM Serial data line serial DIMM recognition. Internally pulled high.
SD_RAS#	1	TO	Row Address Strobe**:** SD_CAS#, SD_RAS,# and SD_WE# identify the command being sent to the DRAM devices.
SD_VREF	1	AI	Input threshold reference for the interface used on the DDR interface.
SD_WE#	1	TO	Write Enable: SD_CAS#, SD_RAS#, and SD_WE# identify the command being sent to the DRAM devices.
SD_PWRDELAY	1	I	Indicates healthy power supply. When high during chip reset, the memory controller executes a power failure sequence.
DDR Pin Count	132		

3.1.4 Dual-Gigabit Ethernet (GigE) Interface Signals

This section describes signals for the GW80314 dual-ethernet controller. Signals in this group are 3.3 V LVTTL compatible.

Table 6. GigE Signals (Sheet 1 of 3)

Pin Name	Count	Pin Type	Description
Port 0			
E0_TCG[3:0]	4	TO	All modes: Transmit Code Group Lower Nibble.
E0_TCG[7:4]	4	TO	GMII mode: Transmit Code Group Upper Nibble. TBI mode: Transmit Code Group Upper Nibble.
E0_TCG[8]	1	TO	MII mode: Transmit Enable. This signal is synchronous to E0_TX_CLK and provides precise framing for data carried on E0_TCG[3:0] for the external PMA. It is asserted when E0_TCG[3:0] contains valid data to be transmitted. G/MII mode: Transmit Enable. This signal is synchronous to GTX_CLK and provides precise framing for data carried on E0_TCG[7:0] for the external PMA. It is asserted when E0_TCG[7:0] contains valid data to be transmitted. TBI mode: Transmit Code Group bit 8. Synchronous to GTX_CLK.
E0_TCG[9]	1	TO	MII mode: Transmit Error. This signal is synchronous to E0_TX_CLK and provides error indications. G/MII mode: Transmit Error. This signal is synchronous to GTX_CLK and provides error indications. TBI mode: Transmit Code Group bit 9. Synchronous to GTX_CLK.
E0_RCG[3:0]	4	I	All modes: Receive Code Group Lower Nibble. This is a group of four signals, sourced from an external PMA, that contains data aligned on nibble boundaries and are driven synchronous to the E0_CLK. E0_RCG[3] is the most significant bit and E0_RCG[0] is the least significant bit.
E0_RCG[7:4]	4	I	G/MII mode: Receive Code Group Upper Nibble This is a group of four signals, sourced from an external PMA, that contains data aligned on byte boundaries and are driven synchronous to the E0_CLK. E0_RCG[7] is most significant bit. TBI mode: Receive Code Group Upper Nibble.
E0_RCG[8]	1	I	G/MII modes: Receive Data Valid. This indicates that the external PMA is presenting recovered and decoded nibbles on the E0_RCG signals, and that E0_CLK is synchronous to the recovered data in 100 Mb/s and 1000 Mb/s operation. This signal encompasses the frame, starting with the Start-of-Frame delimiter (JK) and excluding any End-of-Frame delimiter (TR). TBI Mode: Transmit Code Group bit 8.
E0_RCG[9]	1	I	G/MII modes: Receive Error. This signal is synchronous to E0_CLK/E0_PMA_CLK0 and provides media error indications. TBI mode: Transmit Code Group bit 9.
E0_PCRS_SDET	1	I	G/MII modes: PHY Carrier Sense indication. TBI mode: Indicates signals detected.
E0_PCOL_RBCM	1	IO	G/MII modes: PHY Collision Input. TBI mode: Receive Byte Clock mode output. When low the E0_PMA_CLK0 and E0_PMA_CLK1 are active as half rate clocks. When high the E0_PMA_CLK0 is active as a 125MHz clock input.
E0_ECMDT	1	TO	TBI mode: Enable Comma Detect. Enables SERDES to perform code group alignment upon detection of comma.
E0_EWRAP	1	TO	TBI mode: Enable Wrap. Enables SERDES to loop transmit signals to receive (Loopback).
E0_PRBSEN	1	TO	TBI mode: PRBS Enable. Used to enable PRBS test mode inside TBI SERDES devices.
E0_PRBS_PASS	1	I	TBI mode: PRBS Pass indicator input (high = pass).

Table 6. GigE Signals (Sheet 2 of 3)

Pin Name	Count	Pin Type	Description
E0_RXCLK/ E0_PMA_CLK0	1	I	G/MII modes: Receive Clock from PMA. TBI mode: PMA Receive Clock 0 or 125 MHz Receive Clock depending on state of RBCMODE.
E0_TXCLK/ E0_PMA_CLK1	1	I	G/MII mode: 2.5 MHz or 25 MHz Transmit Clock. TBI mode: PMA Receive Clock 1.
Port 1			
E1_TCG[3:0]	4	TO	All modes: Transmit Code Group Lower Nibble.
E1_TCG[7:4]	4	TO	G/MII mode: Transmit Code Group Upper Nibble. TBI mode: Transmit Code Group Upper Nibble.
E1_TCG[8]	1	TO	MII mode: Transmit Enable. This signal is synchronous to E1_TX_CLK and provides precise framing for data carried on E1_TCG[3:0] for the external PMA. It is asserted when E1_TCG[3:0] contains valid data to be transmitted. G/MII mode: Transmit Enable. This signal is synchronous to GTX_CLK and provides precise framing for data carried on E1_TCG[7:0] for the external PMA. It is asserted when E1_TCG[7:0] contains valid data to be transmitted. TBI mode: Transmit Code Group bit 8. Synchronous to GTX_CLK.
E1_TCG[9]	1	TO	MII mode: Transmit Error. This signal is synchronous to E1_TX_CLK and provides error indications. G/MII mode: Transmit Error. This signal is synchronous to GTX_CLK and provides error indications. TBI mode: Transmit Code Group bit 9. Synchronous to GTX_CLK.
E1_RCG[3:0]	4	I	All modes: Receive Code Group Lower Nibble. This is a group of 4 signals, sourced from an external PMA, that contains data aligned on nibble boundaries and are driven synchronous to the E1_CLK. E1_RCG[3] is the most significant bit and E1_RCG[0] is the least significant bit.
E1_RCG[7:4]	4	I	G/MII mode: Receive Code Group Upper Nibble This is a group of 4 signals, sourced from an external PMA, that contains data aligned on byte boundaries and are driven synchronous to the E1_CLK. E1_RCG[7] is most significant bit. TBI mode: Receive Code Group Upper Nibble.
E1_RCG[8]	1	I	G/MII modes: Receive Data Valid. This indicates that the external PMA is presenting recovered and decoded nibbles on the E1_RCG signals, and that E1_CLK is synchronous to the recovered data in 100 Mb/s and 1000 Mb/s operation. This signal encompasses the frame, starting with the Start-of-Frame delimiter (JK) and excluding any End-of-Frame delimiter (TR). TBI Mode: Transmit Code Group bit 8.
E1_RCG[9]	1	I	G/MII modes: Receive Error. This signal is synchronous to E1_CLK/E1_PMA_CLK0 and provides media error indications. TBI mode: Transmit Code Group bit 9.
E1_PCRS_SDET	1	I	G/MII modes: PHY Carrier Sense indication. TBI mode: Indicates signals detected.
E1_PCOL_RBCM	1	IO	G/MII modes: PHY Collision Input. TBI mode: Receive Byte Clock mode output. When low the E1_PMA_CLK0 and E1_PMA_CLK1 are active as half rate clocks. When high the E1_PMA_CLK0 is active as a 125 MHz clock input.
E1_ECMDT	1	TO	TBI mode: Enable Comma Detect. Enables SERDES to perform code group alignment upon detection of comma.
E1_EWRAP	1	TO	TBI mode: Enable Wrap. Enables SERDES to loop transmit signals to receive (Loopback).
E1_PRBSEN	1	TO	TBI mode: PRBS Enable. Used to enable PRBS test mode inside TBI SERDES devices.
E1_PRBS_PASS	1	I	TBI mode: PRBS Pass indicator input (high = pass).

Table 6. GigE Signals (Sheet 3 of 3)

Pin Name	Count	Pin Type	Description
E1_RXCLK/ E1_PMA_CLK0	1	I	G/MII modes: Receive Clock from PMA. TBI mode: PMA Receive Clock 0 or 125 MHz Receive Clock depending on state of RBCMODE.
E1_TXCLK/ E1_PMA_CLK1	1	I	G/MII mode: 2.5 MHz or 25 MHz Transmit Clock. TBI mode: PMA Receive Clock 1.
Management interface			
MDC	1	O	Management Data Clock (2.5 MHz by 802.3 Specification.)
MDIO	1	IO	Management Data I/O Bidirectional Pin.
Gigabit Clocks			
REF125M	1	I	All Modes: 125 MHz reference clock input.
GTX_CLK	1	O	All Modes: 125 MHz transmit clock output.
GigE Pin Count	60		

3.1.5 Peripheral Bus Interface Signals

This section describes signals for the GW80314 Peripheral Bus. Signals in this group are 3.3 V LVTTL compatible.

Table 7. Peripheral Bus Interface Signals

Pin Name	Count	Pin Type	Description
PBI_AD[31:0]	32	IO	Address/Data Bus.
PBI_OE#	1	O	Output Enable.
PBI_CS#[3:0]	4	O	Chip Selects: Active low signal indicating that an external device has been selected for access.
PBI_LE	1	IO	Latch Enable: Address latch signal to indicate when addresses are valid on the PBI_AD bus.
PBI_RDY#	1	I	Ready Input: In handshake mode, indicates that external device is ready to commence transfer.
PBI_RW	1	O	Read/Write Enable: Low indicates a write access is underway.
PBI Pin Count	40		

3.1.6 P1 PCI/X Signals

This section describes the GW80314 PCI/X signals on the P1 PCI/X bus.

Table 8. P1 PCI/X Signals (Sheet 1 of 2)

Pin Name	Count	Pin Type	Description
P1_ACK64#	1	IO	Acknowledge 64-bit transaction: Active low signal asserted by a target to indicate its willingness to participate in a 64-bit transaction. Driven by the target; sampled by the master. Rescinded by the target at the end of the transaction.
P1_AD[63:0]	64	IO	Address/Data Bus: Address and data are multiplexed over these pins providing a 64-bit address/data bus.
P1_CBE#[7:0]	8	IO	Bus Command and Byte Enable Lines: Command and byte enable information is multiplexed over all eight CBE lines.
P1_CLK_IN	1	I	PCI Input Clock: Clock In for the PCI/X Port 1 interface used to generate fixed timing parameters. P1_CLK_IN can operate between 25 and 133 MHz
P1_CLK_OUT	1	O	PCI Output Clock: Clock out for the PCI/X Port 1 interface. This is a valid clock output only when this interface is used as the controlling resource.
P1_DEVSEL#	1	IO	Device Select: An active low indication from an agent that is the target of the current transaction. Driven by the target; sampled by the master. Rescinded by the target at the end of the transaction.
P1_FRAME#	1	IO	Cycle Frame for PCI/X Bus: An active low indication from the current bus master of the beginning and end of a transaction. Driven by the bus master; sampled by the selected target. Rescinded by the bus master at the end of the transaction.
P1_GNT#[1]	1	IO	Grant: This is an input when an external arbiter is used and an output when the internal arbiter is used. As an input it is used by the external arbiter to grant the bus to the GW80314. As an output it is used by the internal arbiter to grant the bus to an external master.
P1_GNT#[7:2]	6	TO	Grant: These are used by the internal arbiter to grant the bus to an external master
P1_IDSEL	1	I	Initialization Device Select: Used as a chip select during Configuration 0 read and write transactions
P1_INTA#	1	IO(OD)	Interrupt A: An active low level sensitive indication of an interrupt.
P1_INTB#	1	IO(OD)	Interrupt B: An active low level sensitive indication of an interrupt.
P1_INTC#	1	IO(OD)	Interrupt C: An active low level sensitive indication of an interrupt.
P1_INTD#	1	IO(OD)	Interrupt B: An active low level sensitive indication of an interrupt.
P1_IRDY#	1	IO	Initiator Ready: An active low indication of the current bus master's ability to complete the current data phase. Driven by the master; sampled by the selected target.
P1_M66EN	1	I	PCI 66 MHz Enable: Controls the 33/66 MHz clock generation when in PCI mode. When pulled low, it configures the PCI Port 1 PLL clock output for 33 MHz. When pulled high, it configures the PCI Port 1 PLL for 66 MHz operation.
P1_PAR	1	IO	Parity: Carries even parity across P1_AD[31:0] and P1_C/BE[3:0]. Driven by the master for the address and write data phases. Driven by the target for read data phases.
P1_PAR64	1	IO	Parity upper dword: Carries even parity across P1_AD[63:32] and P1_CBE[7:4]. Driven by the master for address and write data phases. Driven by the target for read data phases.
P1_PCIXCAP[1:0]	2	I	PCI/X Capability pin: Indicates the speed and mode of PCI/X interface when configured as the control resource (P1_RSTDIR = 1).
P1_PERR#	1	IO	Parity Error: An active low indication of a data parity error. Driven by the target receiving data. Rescinded by that agent at the end of the transaction.

Table 8. P1 PCI/X Signals (Sheet 2 of 2)

Pin Name	Count	Pin Type	Description
P1_PME#	1	IO(OD)	Power Management (optional interrupt pin)
P1_REQ#[1]	1	IO	Bus Request: This is an output when an external arbiter is used and an input when the internal arbiter is used. As an input it is used by an external master to request the bus. As an output it is used by the GW80314 to request the bus.
P1_REQ#[7:2]	6	I	Bus Request: These signals are used by external masters to request the PCI/X bus.
P1_REQ64#	1	IO	Request 64-bit transfer: An active low indication from the current master of its choice to perform 64-bit transactions. Rescinded by the bus master at the end of the transaction.
P1_RST#	1	IO	Reset: Asynchronous active low reset for PCI/X interface. When the interface is the secondary side in a transparent bridge, this pin is configured as an output.
P1_RSTDIR	1	I	Reset Direction: 0 = P1_RST# is input and P1_CLK_OUT is driven to 0. 1 = P1_RST# is output and P1_CLK_OUT is generated (PCI Port 1 is controlling resource).
P1_SERR#	1	OD	System Error: An active low indication of address parity error.
P1_STOP#	1	IO	Stop: An active low indication from the target of its desire to stop the current transition. Sampled by the master; rescinded by the target at the end of the transaction
P1_TRDY#	1	IO	Target Ready: An active low indication of the current target's ability to complete the data phase. Driven by the target; sampled by the current bus master. Rescinded by the target at the end of the transaction.
P1 PCI/X Pin Count	110		

3.1.7 P2 PCI/X Signals

This section describes the GW80314 PCI/X signals on P2 PCI/X bus.

Table 9. P2 PCI/X Signals (Sheet 1 of 2)

Pin Name	Count	Pin Type	Description
P2_ACK64#	1	IO	Acknowledge 64-bit transaction: Active low signal asserted by a target to indicate its willingness to participate in a 64-bit transaction. Driven by the target; sampled by the master. Rescinded by the target at the end of the transaction.
P2_AD[63:0]	64	IO	Address/Data Bus: Address and data are multiplexed over these pins providing a 64-bit address/data bus.
P2_CBE#[7:0]	8	IO	Bus Command and Byte Enable Lines: Command and byte enable information is multiplexed over all eight CBE lines.
P2_CLK_IN	1	I	PCI Input Clock: Clock input for the PCI/X Port 1 interface used to generate fixed timing parameters. P2_CLK_IN can operate between 25 and 133 MHz.
P2_CLK_OUT	1	O	PCI Output Clock: Clock out for the PCI/X Port 2 interface. This is a valid clock output only when this interface is used as the controlling resource.
P2_DEVSEL#	1	IO	Device Select: An active low indication from an agent that is the target of the current transaction. Driven by the target; sampled by the master. Rescinded by the target at the end of the transaction.
P2_FRAME#	1	IO	Cycle Frame for PCI/X Bus: An active low indication from the current bus master of the beginning and end of a transaction. Driven by the bus master; sampled by the selected target. Rescinded by the bus master at the end of the transaction.
P2_GNT#[1]	1	IO	Grant: This is an input when an external arbiter is used and an output when the internal arbiter is used. As an input it is used by the external arbiter to grant the bus to the GW80314. As an output it is used by the internal arbiter to grant the bus to an external master.
P2_GNT#[7:2]	6	TO	Grant: These are used by the internal arbiter to grant the bus to an external master.
P2_IDSEL	1	I	Initialization Device Select: Used as a chip select during Configuration read and write transactions.
P2_INTA#	1	IO(OD)	Interrupt A: An active low level sensitive indication of an interrupt.
P2_INTB#	1	IO(OD)	Interrupt B: An active low level sensitive indication of an interrupt.
P2_INTC#	1	IO(OD)	Interrupt C: An active low level sensitive indication of an interrupt.
P2_INTD#	1	IO(OD)	Interrupt D: An active low level sensitive indication of an interrupt.
P2_IRDY#	1	IO	Initiator Ready: An active low indication of the current bus master's ability to complete the current data phase. Driven by the master; sampled by the selected target.
P2_M66EN	1	I	PCI 66 MHz Enable: Controls 33/66 MHz clock generation when in PCI mode. When pulled low, it configures the PCI Port 2 PLL clock output for 33MHz operation. When pulled high, it configures the PCI Port 2 PLL clock output for 66MHz operation.
P2_PAR	1	IO	Parity: Carries even parity across P2_AD[31:0] and P2_C/BE[3:0]. Driven by the master for the address and write data phases. Driven by the target for read data phases.
P2_PAR64	1	IO	Parity upper dword: Carries even parity across P2_AD[63:32] and P2_CBE[7:4]. Driven by the master for address and write data phases. Driven by the target for read data phases.
P2_PCIXCAP[1:0]	2	I	PCI/X Capability pin: Indicates the speed and mode of PCI/X interface when configured as the control resource (P2_RSTDIR = 1).
P2_PERR#	1	IO	Parity Error: An active low indication of a data parity error. Driven by the target receiving data. Rescinded by that agent at the end of the transaction.

Table 9. P2 PCI/X Signals (Sheet 2 of 2)

Pin Name	Count	Pin Type	Description
P2_PME#	1	IO(OD)	Power Management (optional interrupt pin).
P2_REQ#[1]	1	IO	Bus Request: This is an output when an external arbiter is used and an input when the internal arbiter is used. As an input it is used by an external master to request the bus. As an output it is used by the GW80314 to request the bus.
P2_REQ#[7:2]	6	I	Bus Request: These signals are used by external masters to request the PCI/X bus.
P2_REQ64#	1	IO	Request 64-bit transfer: An active low indication from the current master of its choice to perform 64-bit transactions. Rescinded by the bus master at the end of the transaction.
P2_RST#	1	IO	Reset: Asynchronous active low reset for PCI/X interface
P2_RSTDIR	1	I	Reset Direction: 0 = P2_RST# is input and P2_CLK_OUT is driven to 0. 1 = P2_RST# is output and P2_CLK_OUT is generated (PCI Port 2 is controlling resource).
P2_SERR#	1	O(OD)	System Error: An active low indication of address parity error.
P2_STOP#	1	IO	Stop: An active low indication from the target of its desire to stop the current transition. Sampled by the master; rescinded by the target at the end of the transaction
P2_TRDY#	1	IO	Target Ready: An active low indication of the current target's ability to complete the data phase. Driven by the target; sampled by the current bus master. Rescinded by the target at the end of the transaction.
P2 PCI/X Pin Count	110		

3.1.8 P1 Hot Swap Signals

This section describes the GW80314 PCI Port 1 Hot Swap signals.

Table 10. P1 Hot Swap Signals

Pin Name	Count	Pin Type	Description
P1_ENUM#	1	IO(OD)	System Enumeration: Used to notify system host that a board has been freshly inserted or extracted from the system.
P1_ES	1	I	Ejector Switch: Indicates the status of Hot Swap board ejector switch.
P1_HEALTHY#	1	I	Board healthy - In a CPCI Hot Swap environment, indicates the board is ready to be released from reset and become an active agent on the PCI bus. Negation of P1_HEALTHY# resets all GW80314 resources, including PLLs. Additionally, all GW80314 outputs are tristated when this pin is negated; some inputs and bidirectionals are inhibited.
P1_HS_64EN#	1	I	PCI/X 64-bit Enable: An active low indication that a CompactPCI Hot Swap board is in a 64-bit slot.
P1_LED#	1	OD	LED: Controls the Hot Swap status LED.
P1 Hot Swap Pin Count	5		

3.1.9 P2 Hot Swap Signals

This section describes the GW80314 PCI Port 2 Hot Swap signals.

Table 11. P2 Hot Swap Signals

Pin Name	Count	Pin Type	Description
P2_ENUM#	1	IO(OD)	System Enumeration: Used to notify system host that a board has been freshly inserted or extracted from the system.
P2_ES	1	I	Ejector Switch: Indicates the status of Hot Swap board ejector switch.
P2_HEALTHY#	1	I	Board healthy - In a CPCI Hot Swap environment, indicates the board is ready to be released from reset and become an active agent on the PCI bus. Negation of P1_HEALTHY# resets all GW80314 resources, including PLLs. Additionally, all GW80314 outputs are tristated when this pin is negated; some inputs and bidirectionals are inhibited.
P2_HS_64EN#	1	I	PCI/X 64-bit Enable: An active low indication that a CompactPCI Hot Swap board is in a 64-bit slot.
P2_LED#	1	O	LED: Controls the Hot Swap status LED.
P2 Hot Swap Pin Count	5		

3.1.10 Interrupt Controller Signals

This section describes signals for the GW80314 interrupt controller. Signals in this group are 3.3 V LVTTL compatible.

Table 12. Interrupt Controller Signals

Pin Name	Count	Pin Type	Description
INT[15:8]	8	IO	Inputs representing external, incoming interrupts.
INT[7:0]	8	I	Inputs representing external, incoming interrupts.
Interrupt Total	16		

3.1.11 Dual UART Signals

This section describes signals for the GW80314 dual UARTs. Signals in this group are 3.3 V LVTTL compatible. On reset, GPIO[7:0] are GW80314 outputs driven to the value 0x88h and remain driven until firmware configures.

Table 13. UART Signals

Pin Name	Count	Pin Type	Description
UART0			
U0_RX	1	I	Data In: Serial input data
U0_TX	1	O	Data Out: Serial output data
U0_CTS#	1	I	Clear to Send: When low, this indicates that the MODEM or data set is ready to exchange data.
U0_RTS#	1	O	Request to Send: When low, this informs the MODEM or data set that the UART is ready to exchange data.
U0_DSR#/ GPIO[6]	1	IO	Data Set Ready Output: When low, this indicates that the MODEM or data set is ready to establish the communications link with the UART. This pin is multiplexed with GPIO[6].
U0_DTR#/ GPIO[7]	1	IO	Data Terminal Ready Output: When low, this informs the MODEM or data set that the UART is ready to establish a communications link. This pin is multiplexed with GPIO[7].
U0_DCD#/ GPIO[4]	1	IO	Data Carrier Detect Output: When low, this indicates that the data carrier has been detected by the MODEM or data set. This pin is multiplexed with GPIO[4].
U0_RI#/ GPIO[5]	1	IO	Ring Indicator Output: When low, this indicates that a telephone ringing signal has been received by the MODEM or data set. This pin is multiplexed with GPIO[5].
UART1			
U1_RX	1	I	Data In: Serial input data
U1_TX	1	O	Data Out: Serial output data
U1_CTS#	1	I	Clear to Send: When low, this indicates that the MODEM or data set is ready to exchange data.
U1_RTS#	1	O	Request to Send: When low, this informs the MODEM or data set that the UART is ready to exchange data.
U1_DSR#/ GPIO[2]	1	IO	Data Set Ready Output: When low, this indicates that the MODEM or data set is ready to establish the communications link with the UART. This pin is multiplexed with GPIO[2].
U1_DTR#/ GPIO[3]	1	IO	Data Terminal Ready Output: When low, this informs the MODEM or data set that the UART is ready to establish a communications link. This pin is multiplexed with GPIO[3].
U1_DCD#/ GPIO[0]	1	IO	Data Carrier Detect Output: When low, this indicates that the data carrier has been detected by the MODEM or data set. This pin is multiplexed with GPIO[0].
U1_RI#/ GPIO[1]	1	IO	Ring Indicator Output: When low, this indicates that a telephone ringing signal has been received by the MODEM or data set. This pin is multiplexed with GPIO[1].
UART Pin Count	16		

3.1.12 I²C Signals

This section describes the GW80314 I²C signals, which are 3.3 V LVTTL compatible.

Table 14. I²C Signals

Pin Name	Count	Pin Type	Description
I2C_SCLK	1	OD	I²C Serial Clock Output - EEPROM Serial clock. Internally Pulled High.
I2C_SDA	1	IO(OD)	Serial data - EEPROM Serial data line. This signal is internally Pulled High.
I2C Pin Count	2		

3.1.13 Miscellaneous Signals

This section describes the GW80314 miscellaneous signals which are 3.3 V LVTTL compatible.

Table 15. Miscellaneous Signals

Pin Name	Count	Pin Type	Description
PWRUP_PBI_BSWP (Configuration Pin)	1	I	Used during power-up to determine whether the PBI interface is operating in Intel XScale® microprocessor Byte Swap Mode (1 - Enable Byte Swap Mode).
PWRUP_P1_ARB (Configuration Pin)	1	I	Used during power-up to determine whether the PCI1 interface uses the internal GW80314 PCI1 Arbiter (1 - Internal Arbiter Selected).
PWRUP_P1_PRIM	1	I	Transparent Mode: Always strap low - 0. Embedded Mode: Used in conjunction with P1_RSTDIR to determine the source of chip reset.
PWRUP_P2_ARB (Configuration Pin)	1	I	Used during power-up to determine whether the PCI2 interface uses the internal GW80314 PCI2 Arbiter (1 - Internal Arbiter Selected).
PWRUP_P2_PRIM	1	I	Transparent Mode: Always strap low - 0. Embedded Mode: Used in conjunction with P2_RSTDIR to determine the source of chip reset.
PWRUP_TRANS (Configuration Pin)	1	I	Used during power-up to determine whether the P2P bridge is operating in embedded or transparent mode. 0 = Embedded Mode Operation 1 = Transparent Mode Operation
PWRUP_XS_SWRST (Configuration Pin)	1	I	Controls state of Software Reset inside Intel XScale® microprocessor CIU block (1 - Intel XScale® interface held in reset until cleared by processor).
PWRUP_P1_SWRST (Configuration Pin)	1	I	Controls state of Software Reset inside P1 PCI/X block (1 - PCI1 interface held in reset until cleared by processor).
PWRUP_P2_SWRST (Configuration Pin)	1	I	Controls state of Software Reset inside P2 PCI/X block (1 - PCI2 interface held in reset until cleared by processor).
PWRUP_P1_BYP (Configuration Pin)	1	I	Used during power up to enable P1PCI PLL bypass mode (1 - PCI1 PLL is bypassed).
PWRUP_P2_BYP (Configuration Pin)	1	I	Used during power up to enable P2 PCI PLL bypass mode (1 - PCI2 PLL is bypassed).
SFN_CLK	1	I	Fabric Clock input.
SFN_RST#	1	I	Fabric Gasket Reset and General Chip Reset.
SRAM_SKU	1	I	The SRAM_SKU pin (AW33) is an input-only pin with an internal pull-up. When this pin is tied low, the SDRAM inside the Intel® GW80314 I/O Companion Chip is inaccessible. “No SRAM” skew parts must tie this pin low. When this pin is left floating, the device ID incorrectly indicates that SDRAM is usable.
NC_(Location)	5		No Connect Pins (NC_J35, NC_K34, NC_L6, NC_M33, NC_N6)
Misc. Pin Count	19		

3.1.14 Test Signals

This section describes the GW80314 signals used to support silicon or board-level testing. Signals in this section are 3.3 V LVTTL compatible.

Table 16. Test Signals

Pin Name	Count	Pin Type	Description
TCK	1	I	Test Clock (JTAG): Used to clock state information and data into and out of the device during boundary scan
TMS	1	I(PU)	Test Mode Select (JTAG): Used to control the state of the TAP controller. Internally Pulled High.
TDI	1	I(PU)	Test Data Input (JTAG): Used to shift data and instruction into boundary scan. Internally Pulled High.
TDO	1	TO	Test Data Output (JTAG): Used to shift data and instruction out of boundary scan
TRST#	1	I(PU)	Test Reset (JTAG): Asynchronous reset for the JTAG controller. This pin must be asserted low during the power-up reset sequence to ensure that the Boundary Scan Register elements are configured for normal system operation. Customers must assert TRST# concurrently with SF_RST or P1_RST or P2_RST (depending on power-up configurations) as part of the power-up reset sequence. Internally pulled high. Pull-down resistor when JTAG is not used.
Test Pin Count	5		

3.1.15 PLL Power Signals

This section describes the GW80314 signals used to support on board PLLs for the various interfaces. Each AVCC pin supplies 3.3 V (typical) to each interface.

Table 17. PLL Power Signals

Pin Name	Count	Pin Type	Description
XS_PLL_AVCC (V_{CC33})	1	S	Analog Power pin for Intel XScale® microprocessor Interface PLL.
XS_PLL_AVSS	1	S	Analog Ground pin for Intel XScale® microprocessor Interface PLL.
SD_PLL_AVCC (V_{CC33})	1	S	Analog Power pin for DDR SDRAM Interface PLL.
SD_PLL_AVSS	1	S	Analog Ground pin for DDR SDRAM Interface PLL.
P1_PLL_AVCC (V_{CC33})	1	S	Analog Power pin for PCI1 Interface PLL.
P1_PLL_AVSS	1	S	Analog Ground pin for PCI1 Interface PLL.
P2_PLL_AVCC (V_{CC33})	1	S	Analog Power pin for PCI2 Interface PLL.
P2_PLL_AVSS	1	S	Analog Ground pin for PCI2 Interface PLL.
PLL Supply Count	8		

3.1.16 Power Supplies

This section describes the GW80314 power supplies used to support both I/O interfaces and Core elements.

Table 18. Power Supplies

Pin Name	Pin Type / Count	Description
VCC_CORE (V_{CC12})	S / 75	Core Power Supply for the GW80314.
VCC_PC (V_{CC33})	S / 56	I/O Power Supply for PCI Interface.
VCC_SD (V_{CC25})	S / 26	I/O Power Supply for DDR SDRAM Interface.
VCC_XS (V_{CC33})	S / 28	I/O Power Supply for Intel XScale® microprocessor Interface.
VSS_CORE	S / 73	Core Ground Supply for the GW80314.
VSS_IO	S / 119	I/O Ground Supply.
VCC Pin Count Total	185	
VSS Pin Count Total	192	

3.1.17 Signal Pin Mode Behavior

This section describes the GW80314 signal pin mode behavior during reset, normal operation, 32-bit PCI mode, and error correction mode.

Table 19. Signal Pin Mode Behavior (Sheet 1 of 7)

Pin Name	Reset	Norm	Hold	32-Bit PCI	32-Bit Mem	ECC Off
XS_A[15:0]	VI	VI	–	–	–	–
XS_ABORT	0	VO	–	–	–	–
XS_BE[7:0]	0	VB	–	–	–	–
XS_CLK	0	VB	–	–	–	–
XS_CWF / DBuswidth	0	VO	–	–	–	–
XS_DQ[63:0]	0	VB	–	–	–	–
XS_DVALID[1:0]	0	VO	–	–	–	–
XS_HOLD[1:0]	0	VO	–	–	–	–
XS_HLDA[1:0]	VI	VI	–	–	–	–
XS_ECC[7:0]	0	VB	–	–	–	–
XS_FIQ[1] / PWRUP_SD_BYP	L	VO	1	–	–	–
XS_FIQ[0]	0	VO	–	–	–	–
XS_IRQ[1]/PWRUP_XS_BYP	L	VO	1	–	–	–
XS_IRQ[0]/PWRUP_FADJ	L	VO	1	–	–	–
XS_LEN[2:0]	VI	VI	–	–	–	–
XS_RESET#	0	VO	–	–	–	–
SD_A[13:0]	0*	VO	–	–	–	–
SD_BA[1:0]	0*	VO	–	–	–	–
SD_CAS#	1*	VO	–	–	–	–
SD_CLK[3:0]	VO	VO	–	–	–	–
SD_CLK#[3:0]	VO	VO	–	–	–	–
SD_CLKEN	0*	VO	–	–	–	–
SD_CKFBI	VI	VI	–	–	–	–
SD_CKFBO	VO	VO	–	–	–	–
SD_CS#[7:0]	1*	VO	–	–	–	–
SD_DQ[63:32]	Z*	VB	–	–	ID	–

NOTES:
1. 1 = driven to V_{CC}
2. Z = output disabled (floats)
3. 0 = driven to V_{SS}
4. VB = acts like a valid bidirectional pin
5. ID = input is disabled
6. VO = a valid output level is driven
7. VO_M = a valid output level is driven (PCI Master)
8. VO_T = a valid output level is driven (PCI Target)
9. H = pulled up to V_{CC}
10. L = pulled down to V_{SS}
11. VI = need to drive a valid input level
12. VI_M = need to drive a valid input level (PCI Master)
13. VI_T = need to drive a valid input level (PCI Target)
14. PD = pull-up disabled
15. * = after power fail sequence completes

Table 19. Signal Pin Mode Behavior (Sheet 2 of 7)

Pin Name	Reset	Norm	Hold	32-Bit PCI	32-Bit Mem	ECC Off
SD_DQ[31:0]	Z*	VB	–	–	–	–
SD_DQS[17]	Z*	VB	–	–	–	ID
SD_DQS/DM[16:9]	Z*	VB	–	–	ID	–
SD_DQS[8]	Z*	VB	–	–	–	ID
SD_DQS[7:0]	Z*	VB	–	–	–	–
SD_ECC	Z*	VB	–	–	–	ID
SD_I2C_CLK	H	VO	–	–	–	–
SD_I2C_SDA	H	VB	–	–	–	–
SD_RAS#	1*	VO	–	–	–	–
SD_WE#	1*	VO	–	–	–	–
SD_PWRDELAY	VI	VI	–	–	–	–
E0_TCG[9:0]	VO	VO	–	–	–	–
E0_RCG[9:0]	VI	VI	–	–	–	–
E0_PCRS_SDET	VI	VI	–	–	–	–
E0_PCOL_RBCM	Z	VB	–	–	–	–
E0_ECMDT	Z	VO	–	–	–	–
E0_EWRAP	Z	VO	–	–	–	–
E0_PRBSEN	Z	VO	–	–	–	–
E0_PRBS_PASS	VI	VI	–	–	–	–
E0_RXCLK/E0_PMA_CLK0	VI	VI	–	–	–	–
E0_TXCLK/E0_PMA_CLK1	VI	VI	–	–	–	–
E1_TCG[9:0]	VO	VO	–	–	–	–
E1_RCG[9:0]	VI	VI	–	–	–	–
E1_PCRS_SDET	VI	VI	–	–	–	–
E1_PCOL_RBCM	Z	VB	–	–	–	–
E1_ECMDT	Z	VO	–	–	–	–
E1_EWRAP	Z	VO	–	–	–	–
E1_PRBSEN	Z	VO	–	–	–	–
E1_PRBS_PASS	VI	VI	–	–	–	–
E1_RXCLK/E1_PMA_CLK0	VI	VI	–	–	–	–

NOTES:
1. 1 = driven to V_{CC}
2. Z = output disabled (floats)
3. 0 = driven to V_{SS}
4. VB = acts like a valid bidirectional pin
5. ID = input is disabled
6. VO = a valid output level is driven
7. VO_M = a valid output level is driven (PCI Master)
8. VO_T = a valid output level is driven (PCI Target)
9. H = pulled up to V_{CC}
10. L = pulled down to V_{SS}
11. VI = need to drive a valid input level
12. VI_M = need to drive a valid input level (PCI Master)
13. VI_T = need to drive a valid input level (PCI Target)
14. PD = pull-up disabled
15. * = after power fail sequence completes

Table 19. Signal Pin Mode Behavior (Sheet 3 of 7)

Pin Name	Reset	Norm	Hold	32-Bit PCI	32-Bit Mem	ECC Off
E1_TXCLK/E1_PMA_CLK1	VI	VI	–	–	–	–
MDC	0	VO	–	–	–	–
MDIO	Z	VB	–	–	–	–
REF125M	VI	VI	–	–	–	–
GTX_CLK	0	VO	–	–	–	–
PBI_AD[31:0]	0	VB	Z	–	–	–
PBI_OE#	1	VO	–	–	–	–
PBI_CS#[3:0]	1	VO	–	–	–	–
PBI_LE	0	VO	Z	–	–	–
PBI_RDY#	VI	VI	–	–	–	–
PBI_RW	0	VO	Z	–	–	–
P1_ACK64#	Z	VB	–	–	–	–
P1_AD[63:32]	Z	VB	–	H	–	–
P1_AD[31:0]	Z	VB	–	–	–	–
P1_CBE#[7:4]	Z	VB	–	H	–	–
P1_CBE#[3:0]	Z	VB	–	–	–	–
P1_CLK_IN	VI	VI	–	–	–	–
P1_CLK_OUT	0	VO	–	–	–	–
P1_DEVSEL#	Z	VB	–	–	–	–
P1_FRAME#	Z	VB	–	–	–	–
P1_GNT#[1]	Z	VB	–	–	–	–
P1_GNT#[7:2]	Z	VO	–	–	–	–
P1_IDSEL	VI	VI	–	–	–	–
P1_INTA#	Z	VO	–	–	–	–
P1_INTB#	Z	VO	–	–	–	–
P1_INTC#	Z	VO	–	–	–	–
P1_INTD#	Z	VO	–	–	–	–
P1_IRDY#	Z	VB	–	–	–	–
P1_M66EN	VI	VI	–	–	–	–
P1_PAR	Z	VB	–	–	–	–

NOTES:
1. 1 = driven to V_{CC}
2. Z = output disabled (floats)
3. 0 = driven to V_{SS}
4. VB = acts like a valid bidirectional pin
5. ID = input is disabled
6. VO = a valid output level is driven
7. VO_M = a valid output level is driven (PCI Master)
8. VO_T = a valid output level is driven (PCI Target)
9. H = pulled up to V_{CC}
10. L = pulled down to V_{SS}
11. VI = need to drive a valid input level
12. VI_M = need to drive a valid input level (PCI Master)
13. VI_T = need to drive a valid input level (PCI Target)
14. PD = pull-up disabled
15. * = after power fail sequence completes

Table 19. Signal Pin Mode Behavior (Sheet 4 of 7)

Pin Name	Reset	Norm	Hold	32-Bit PCI	32-Bit Mem	ECC Off
P1_PAR64	Z	VB	–	H	–	–
P1_PCIXCAP[1:0]	VI	VI	–	–	–	–
P1_PERR#	Z	VB	–	–	–	–
P1_PME#	Z	VB	–	–	–	–
P1_REQ#[1]	Z	VB	–	–	–	–
P1_REQ#[7:2]	VI	VI	–	–	–	–
P1_REQ64#	VO_M/VI_T	VO_M/VI_T	–	–	–	–
P1_RST#	VB	VB	–	–	–	–
P1_RSTDIR	VI	VI	–	–	–	–
P1_SERR#	Z	VB	–	–	–	–
P1_STOP#	VO_T/VI_M	VO_T/VI_M	–	–	–	–
P1_TRDY#	VO_T/VI_M	VO_T/VI_M	–	–	–	–
P2_ACK64#	Z	VB	–	–	–	–
P2_AD[63:32]	Z	VB	–	H	–	–
P2_AD[31:0]	Z	VB	–	–	–	–
P2_CBE#[7:4]	Z	VB	–	H	–	–
P2_CBE#[3:0	Z	VB	–	–	–	–
P2_CLK_IN	VI	VI	–	–	–	–
P2_CLK_OUT	0	VO	–	–	–	–
P2_DEVSEL#	Z	VB	–	–	–	–
P2_FRAME#	Z	VB	–	–	–	–
P2_GNT#[1]	Z	VB	–	–	–	–
P2_GNT#[7:2]	Z	VO	–	–	–	–
P2_IDSEL	VI	VI	–	–	–	–
P2_INTA#	Z	VO	–	–	–	–
P2_INTB#	Z	VO	–	–	–	–
P2_INTC#	Z	VO	–	–	–	–
P2_INTD#	Z	VO	–	–	–	–
P2_IRDY#	Z	VB	–	–	–	–
P2_M66EN	VI	VI	–	–	–	–

NOTES:
1. 1 = driven to V_{CC}
2. Z = output disabled (floats)
3. 0 = driven to V_{SS}
4. VB = acts like a valid bidirectional pin
5. ID = input is disabled
6. VO = a valid output level is driven
7. VO_M = a valid output level is driven (PCI Master)
8. VO_T = a valid output level is driven (PCI Target)
9. H = pulled up to V_{CC}
10. L = pulled down to V_{SS}
11. VI = need to drive a valid input level
12. VI_M = need to drive a valid input level (PCI Master)
13. VI_T = need to drive a valid input level (PCI Target)
14. PD = pull-up disabled
15. * = after power fail sequence completes

Table 19. Signal Pin Mode Behavior (Sheet 5 of 7)

Pin Name	Reset	Norm	Hold	32-Bit PCI	32-Bit Mem	ECC Off
P2_PAR	Z	VB	–	–	–	–
P2_PAR64	Z	VB	–	H	–	–
P2_PCIXCAP[1:0]	VI	VI	–	–	–	–
P2_PERR#	Z	VB	–	–	–	–
P2_PME#	Z	VB	–	–	–	–
P2_REQ#[1]	Z	VB	–	–	–	–
P2_REQ#[7:2]	VI	VI	–	–	–	–
P2_REQ64#	VO_M/VI_T	VO_M/VI_T	–	–	–	–
P2_RST#	VB	VB	–	–	–	–
P2_RSTDIR	VI	VI	–	–	–	–
P2_SERR#	Z	VB	–	–	–	–
P2_STOP#	VO_T/VI_M	VO_T/VI_M	–	–	–	–
P2_TRDY#	VO_T/VI_M	VO_T/VI_M	–	–	–	–
P1_ENUM#	Z	VB	–	–	–	–
P1_ES	VI	VI	–	–	–	–
P1_HEALTHY#	VI	VI	–	–	–	–
P1_HS_64EN#	VI	VI	–	–	–	–
P1_LED#	Z	VO	–	–	–	–
P2_ENUM#	Z	VO	–	–	–	–
P2_ES	VI	VI	–	–	–	–
P2_HEALTHY#	VI	VI	–	–	–	–
P2_HS_64EN#	VI	VI	–	–	–	–
P2_LED#	Z	VO	–	–	–	–
INT[15:8]/TM_MON[7:0]	VI	VB	–	–	–	–
INT[7:0]	VI	VI	–	–	–	–
U0_RX	VI	VI	–	–	–	–
U0_TX	0	VO	–	–	–	–
U0_CTS#	VI	VI	–	–	–	–
U0_RTS#	1	VI	–	–	–	–
U0_DSR#/GPIO[0]	VI	VB	–	–	–	–

NOTES:
1. 1 = driven to V_{CC}
2. Z = output disabled (floats)
3. 0 = driven to V_{SS}
4. VB = acts like a valid bidirectional pin
5. ID = input is disabled
6. VO = a valid output level is driven
7. VO_M = a valid output level is driven (PCI Master)
8. VO_T = a valid output level is driven (PCI Target)
9. H = pulled up to V_{CC}
10. L = pulled down to V_{SS}
11. VI = need to drive a valid input level
12. VI_M = need to drive a valid input level (PCI Master)
13. VI_T = need to drive a valid input level (PCI Target)
14. PD = pull-up disabled
15. * = after power fail sequence completes

Table 19. Signal Pin Mode Behavior (Sheet 6 of 7)

Pin Name	Reset	Norm	Hold	32-Bit PCI	32-Bit Mem	ECC Off
U0_DTR#/GPIO[1]	VI	VB	–	–	–	–
U0_DCD#/GPIO[2]	VI	VB	–	–	–	–
U0_RI#/GPIO[3]	VI	VB	–	–	–	–
U1_RX	VI	VI	–	–	–	–
U1_TX	0	VO	–	–	–	–
U1_CTS#	VI	VI	–	–	–	–
U1_RTS#	1	VI	–	–	–	–
U1_DSR#/GPIO[4]	VI	VB	–	–	–	–
U1_DTR#/GPIO[5]	VI	VB	–	–	–	–
U1_DCD#/GPIO[6]	VI	VB	–	–	–	–
U1_RI#/GPIO[7]	VI	VB	–	–	–	–
I2C_SCLK	H	VO	–	–	–	–
I2C_SDA	H	VB	–	–	–	–
PWRUP_PBI_BSWP	VI	VI	–	–	–	–
PWRUP_P1_ARB	VI	VI	–	–	–	–
PWRUP_P1_PRIM	VI	VI	–	–	–	–
PWRUP_P2_ARB	VI	VI	–	–	–	–
PWRUP_P2_PRIM	VI	VI	–	–	–	–
PWRUP_TRANS	VI	VI	–	–	–	–
PWRUP_XS_SWRST	VI	VI	–	–	–	–
PWRUP_P1_SWRST	VI	VI	–	–	–	–
PWRUP_P2_SWRST	VI	VI	–	–	–	–
PWRUP_P1_BYP	VI	VI	–	–	–	–
PWRUP_P2_BYP	VI	VI	–	–	–	–
SF_CLK	VI	VI	–	–	–	–

NOTES:
1. 1 = driven to V_{CC}
2. Z = output disabled (floats)
3. 0 = driven to V_{SS}
4. VB = acts like a valid bidirectional pin
5. ID = input is disabled
6. VO = a valid output level is driven
7. VO_M = a valid output level is driven (PCI Master)
8. VO_T = a valid output level is driven (PCI Target)
9. H = pulled up to V_{CC}
10. L = pulled down to V_{SS}
11. VI = need to drive a valid input level
12. VI_M = need to drive a valid input level (PCI Master)
13. VI_T = need to drive a valid input level (PCI Target)
14. PD = pull-up disabled
15. * = after power fail sequence completes

Table 19. Signal Pin Mode Behavior (Sheet 7 of 7)

Pin Name	Reset	Norm	Hold	32-Bit PCI	32-Bit Mem	ECC Off
SF_RST#	VI	VI	–	–	–	–
TCK	VI	VI	–	–	–	–
TMS	H	H	–	–	–	–
TDI	H	H	–	–	–	–
TDO	Z	VO	–	–	–	–
TRST#	H	H	–	–	–	–

NOTES:
1. 1 = driven to V_{CC}
2. Z = output disabled (floats)
3. 0 = driven to V_{SS}
4. VB = acts like a valid bidirectional pin
5. ID = input is disabled
6. VO = a valid output level is driven
7. VO_M = a valid output level is driven (PCI Master)
8. VO_T = a valid output level is driven (PCI Target)
9. H = pulled up to V_{CC}
10. L = pulled down to V_{SS}
11. VI = need to drive a valid input level
12. VI_M = need to drive a valid input level (PCI Master)
13. VI_T = need to drive a valid input level (PCI Target)
14. PD = pull-up disabled
15. * = after power fail sequence completes

3.1.18 1025-Lead HSBGA (Heat Slug Ball Grid Array) Package

Figure 2 shows the drawings for the 1025-lead HSBGA thermally enhanced package being used for the GW80314 device.

Figure 2. 1025-Lead HSBGA Package Drawing

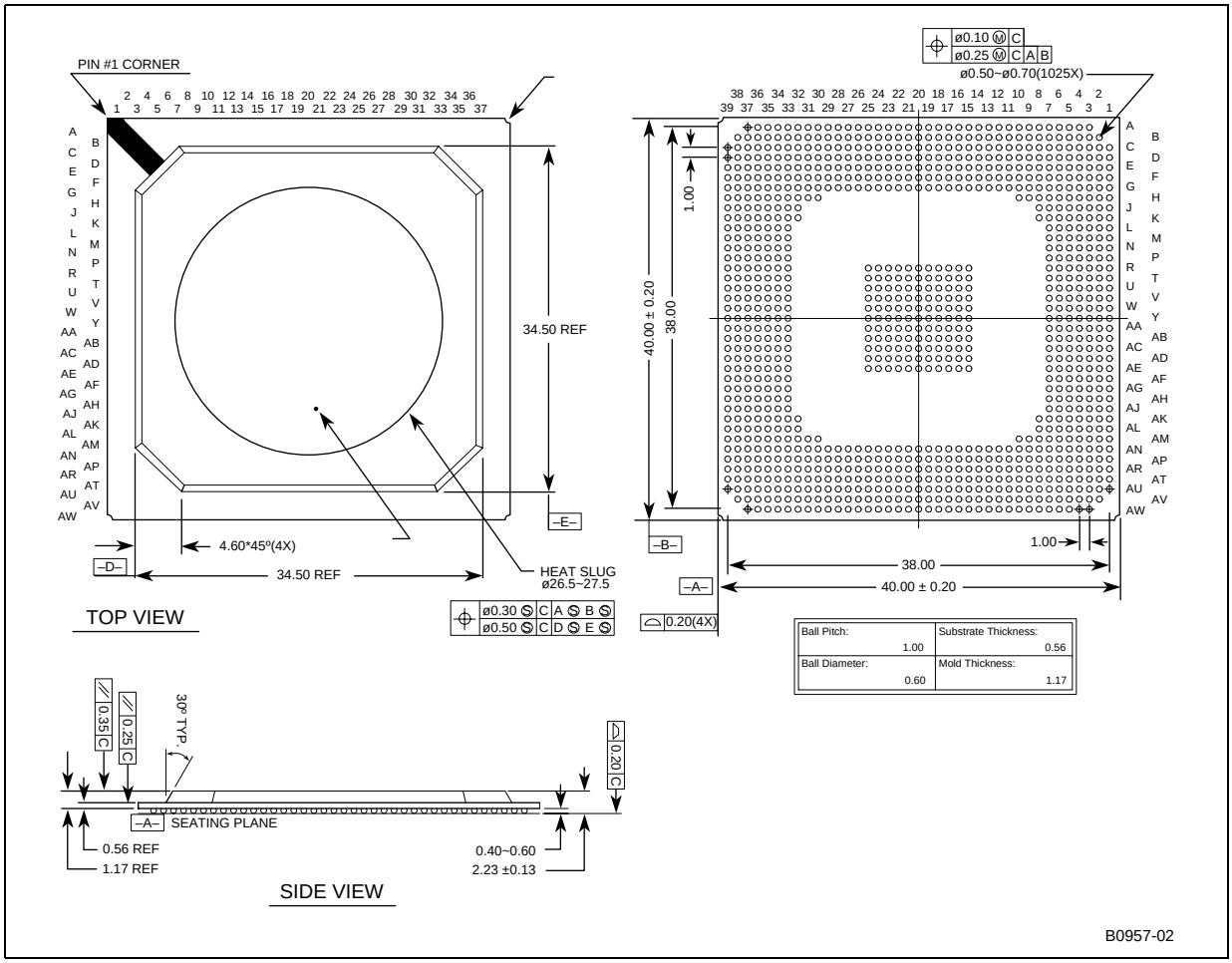


Figure 3. Ball Map - Left Side - Top View

Top View (Left Side)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	NB	NB	E0_ ECMDT	E0_ TCG[5]	E0_ TCG[3]	SD_ DQ[63]	SD_ DQS[6]	SD_ VREF	SD_ DQS[7]	SD_ DQ[57]	SD_ DQ[60]	SD_ DQ[46]	SD_ CAS#	SD_ CS#[0]	SD_ CS#[2]	SD_ WE#	SD_ BA[0]	SD_ CLK[3]	SD_ BA[1]	SD_A[0]	A
B	NB	VSS_IO	VSS_IO	E0_ TCG[1]	MDIO	E0_ TCG[9]	VSS_IO	SD_ DQ[62]	SD_ CLKEN	VSS_IO	SD_ DQ[56]	SD_ DQ[43]	VSS_IO	SD_ CS#[1]	SD_ CS#[3]	VSS_IO	SD_ RAS#	SD_ CLK#[3]	VSS_IO	SD_A[10]	B
C	E0_ RCG[3]	VSS_IO	VSS_IO	E0_PMA_ CLK1	MDC	E0_ PRBSEN	SD_ DQS[15]	SD_ DQ[58]	SD_ DQ[53]	SD_ DQ[49]	SD_ DQ[48]	SD_ DQ[35]	SD_ DQ[38]	SD_ DQS[14]	SD_ DQS[4]	SD_ DQ[37]	SD_ DQ[32]	SD_ECC [3]	SD_ECC [2]	SD_ DQS[8]	C
D	E0_PCOL _RBCM	E0_T CG[7]	E0_PCRS _SDET	VSS_IO	E0_ PRBS_ PASS	E0_ TCG[2]	E0_ TCG[8]	SD_ DQ[52]	SD_ DQ[54]	SD_ DQ[55]	SD_ DQ[50]	SD_ DQ[51]	SD_ DQ[39]	VSS_IO	SD_ DQS[13]	SD_ DQ[33]	VSS_IO	SD_ECC [6]	SD_ DQ[27]	VSS_IO	D
E	E0_ RCG[1]	E0_ EWRAP	E0_ TCG[4]	E0_ TCG[0]	E0_ RCG[0]	VSS_IO	E1_PCOL _RBCM	VSS_IO	SD_ DQ[59]	SD_ DQS[16]	VSS_IO	SD_ DQ[47]	SD_ DQS[5]	SD_ DQ[34]	SD_ DQ[45]	SD_ DQ[44]	SD_ECC [7]	SD_ DQ[31]	SD_ DQS[17]	SD_ ECC[1]	E
F	E0_ RCG[4]	E0_ RCG[5]	E1_ TCG[5]	E0_ RCG[6]	E0_ RCG[2]	VCC_PC	VCC_ CORE	E0_ TCG[6]	VCC_SD	VCC_SD	VCC_SD	SD_ DQ[61]	SD_ DQ[42]	SD_ DQ[41]	VSS_IO	SD_ DQ[40]	SD_ DQ[36]	VSS_IO	SD_ DQ[30]	SD_ DQS[3]	F
G	E0_ RCG[8]	E0_ RCG[9]	VSS_IO	E1_ TCG[9]	E0_PMA_ CLK0	VCC_PC	VCC_ CORE	VCC_ CORE	VCC_SD	VCC_SD	VCC_SD	VCC_SD	VCC_SD	VCC_SD	VCC_SD	VCC_SD	VCC_SD	VCC_SD	VCC_SD	VCC_SD	G
H	E0_ RCG[7]	E1_ TCG[3	E1_ TCG[4]	E1_ TCG[1]	E1_ TCG[7]	VCC_PC	VCC_PC	VCC_ CORE	VCC_ CORE	VCC_ CORE	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	H
J	E1_ TCG[2]	E1_PMA_ CLK1	E1_ RCG[2	E1_ TCG[8]	E1_ TCG[0]	VCC_PC	VCC_ CORE	VCC_ CORE	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	J
K	E1_ TCG[6]	E1_ EWRAP	VSS_IO	REF 125M	E1_ RCG[5]	VCC_PC	VCC_ CORE	VCC_ CORE	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	K
L	P2_ INTD#	E1_ RCG[1]	E1_ RCG[0]	GTX _CLK	E1_ PRBSEN	NC_L6	VCC_ CORE	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	L
M	P2_ GNT#[1]	P2_ REQ#[1]	E1_PMA_ CLK0	E1_ RCG[4]	E1_ RCG[7]	VSS_IO	VCC_PC	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	M
N	P2_ INTB#	VSS_IO	E1_ PCRS_ SDET	E1_ RCG[3]	E1_ PRBS_ PASS	NC_N6	VCC_PC	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	N
P	P2_ AD[31	P2_ RST#	P2_ INTA#	E1_ ECMDT	E1_ RCG[8]	E1_ RCG[6]	VCC_PC	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	P
R	P2_ AD[26]	P2_ HEALTHY #	P2_ IDSEL	P2_ AD[30]	VSS_IO	E1_ RCG[9]	VCC_PC	NB	NB	NB	NB	NB	NB	NB	VSS_ CORE	VCC_ CORE	VSS_ CORE	VCC_ CORE	VSS_ CORE	VCC_ CORE	R
T	P2_ PME#	P2_ AD[27]	P2_ AD[28]	P2_ AD[24]	P2_ CLK_IN	P2_PLL _AVSS	VCC_PC	NB	NB	NB	NB	NB	NB	NB	VCC_ CORE	VSS_ CORE	VCC_ CORE	VSS_ CORE	VCC_ CORE	VSS_ CORE	T
U	P2_ AD[21]	VSS_IO	P2_ INTC#	P2_ IRDY#	VSS_IO	P2_ CLK_OUT	VCC_PC	NB	NB	NB	NB	NB	NB	NB	VSS_ CORE	VCC_ CORE	VSS_ CORE	VCC_ CORE	VSS_ CORE	VCC_ CORE	U
V	P2_ CBE#[3]	P2_ CBE#[1]	P2_ AD[25]	P2_ AD[29]	P2_ AD[23]	P2_PLL_ AVCC	VCC_PC	NB	NB	NB	NB	NB	NB	NB	VCC_ CORE	VSS_ CORE	VCC_ CORE	VSS_ CORE	VSS_ CORE	VSS_ CORE	V
W	P2_ AD[22]	P2_ SERR#	P2_ AD[20]	P2_ AD[18]	VSS_IO	P2_ DEVSEL #	VCC_PC	NB	NB	NB	NB	NB	NB	NB	VSS_ CORE	VCC_ CORE	VSS_ CORE	VSS_ CORE	VSS_ CORE	VSS_ CORE	W
Y	P2_ CBE#[2]	VSS_IO	P2_ AD[19]	P2_ FRAME#	P2_ AD[15]	P2_ TRDY#	VCC_PC	NB	NB	NB	NB	NB	NB	NB	VCC_ CORE	VSS_ CORE	VCC_ CORE	VSS_ CORE	VSS_ CORE	VSS_ CORE	Y
AA	P2_ AD[16]	P2_ AD[17]	P2_ PEER#	P2_PAR	P2_ RSTDIR	P2_ STOP#	VCC_PC	NB	NB	NB	NB	NB	NB	NB	VSS_ CORE	VCC_ CORE	VSS_ CORE	VSS_ CORE	VSS_ CORE	VSS_ CORE	AA
AB	P2_ ACK64#	P2_ AD[12]	P2_ AD[13]	P2_ AD[9]	VSS_IO	P2_ AD[14]	VCC_PC	NB	NB	NB	NB	NB	NB	NB	VCC_ CORE	VSS_ CORE	VCC_ CORE	VSS_ CORE	VSS_ CORE	VSS_ CORE	AB
AC	P2_ AD[10]	VSS_IO	P2_CBE_ [0]#	P2_AD[3]	P2_AD[8]	P2_ AD[11]	VCC_PC	NB	NB	NB	NB	NB	NB	NB	VSS_ CORE	VCC_ CORE	VSS_ CORE	VCC_ CORE	VSS_ CORE	VCC_ CORE	AC
AD	P2_AD[5]	P2_ M66EN	P2_AD[6]	P2_AD[4]	P2_CBE_ [7]#	P2_AD[7]	VCC_PC	NB	NB	NB	NB	NB	NB	NB	VCC_ CORE	VSS_ CORE	VCC_ CORE	VSS_ CORE	VCC_ CORE	VSS_ CORE	AD
AE	P2_ CBE#[6]	P2_AD[1]	P2_AD[0]	P2_REQ_ [3]#	VSS_IO	P2_AD[2]	VCC_PC	NB	NB	NB	NB	NB	NB	NB	VSS_ CORE	VCC_ CORE	VSS_ CORE	VCC_ CORE	VSS_ CORE	VCC_ CORE	AE
AF	P2_ REQ#[4]	VSS_IO	P2_GNT_ [2]#	P2_ REQ#[5]	P2_GNT_ [4]#	P2_ ENUM#	VCC_PC	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	AF
AG	P2_ CBE#[4]	P2_ GNT#[5]	P2_GNT_ [3]#	P2_ AD[61]	VSS_IO	P2_ REQ#[2]	VCC_PC	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	AG
AH	P2_ AD[59]	VSS_IO	P2_ AD[63]	P2_ AD[62]	P2_ AD[58]	P2_ PAR64	VCC_PC	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	AH
AJ	P2_ AD[55]	P2_ AD[60]	P2_ AD[56]	P2_ AD[53]	VSS_IO	P2_ CBE#[5]	VCC_PC	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	AJ
AK	P2_ AD[50]	VSS_IO	P2_ REQ64#	P2_ AD[54]	P2_ AD[49]	P2_ AD[57]	VCC_PC	VCC_ CORE	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	AK
AL	P2_ AD[46]	P2_ AD[51]	P2_ AD[44]	P2_ AD[43]	VSS_IO	P2_ AD[52]	VCC_PC	VCC_ CORE	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	AL
AM	P2_ AD[45]	VSS_IO	P2_ AD[47]	P2_ AD[40]	P2_ AD[39]	P2_ AD[48]	VCC_PC	VCC_ CORE	VCC_ CORE	VCC_ CORE	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	AM
AN	P2_ AD[37]	P2_ AD[41]	P2_ AD[35]	P2_ LED#	VSS_IO	P2_ AD[42]	VSS_IO	VCC-PC	VCC-PC	VCC-PC	VCC-PC	VCC-PC	VCC-PC	VCC-PC	VCC-PC	VCC-PC	VCC-PC	VCC-PC	VCC-PC	VCC-PC	AN
AP	P2_ AD[34]	VSS_IO	P2_ AD[38]	P2_ AD[32]	P2_ AD[33]	P2_ AD[36]	P1_PLL_ AVSS	P1_ CLK_OUT	P1_PLL_ AVCC	P1_ TRDY#	P1_ STOP#	P1_ AD[14]	P1_ AD[11]	P1_ AD[7]	P1_AD[2]	P1_ ENUM#	P1_ REQ#[4]	P1_ PAR64	P1_ CBE#[5]	P1_ AD[57]	AP
AR	P2_ GNT#[6]	P2_ REQ#[7]	P2_REQ_ [6]#	P2_ GNT#[7]	VSS_IO	P1_ AD[29]	P1_CLK _IN	P1_ AD[23]	P1_ DEVSEL#	VSS_IO	P1_ FRAME#	VSS_IO	P1_ RSTDIR	VSS_IO	P1_AD[3]	VSS_IO	P1_ GNT#[4]	VSS_IO	P1_ AD[61]	VSS_IO	AR
AT	P2_ HS_64EN #	P2_ PCIXCAP [1]	P2_ PCIXCAP [0]	VSS_IO	P1_RST #	P1_ GNT#[1]	P1_ AD[30]	P1_ AD[24]	P1_ IRDY#	P1_ AD[18]	P1_PAR	P1_ AD[15]	P1_AD[9]	P1_AD[8]	P1_AD[4]	P1_ REQ#[2]	P1_ REQ#[5]	P1_ CBE#[7]	P1_ AD[62]	P1_ AD[58]	AT
AU	P2_ES	VSS_IO	VSS_IO	P1_IDSEL	P1_ AD[28]	P1_ HEALTHY #	P1_ INTC#	P1_ AD[25]	P1_ AD[20]	P1_ AD[19]	P1_ AD[12]	P1_ AD[13]	P1_AD[6]	P1_ CBE#[0]	P1_ GNT#[5]	P1_AD[0]	P1_ AD[63]	P1_ GNT#[3]	P1_ CBE#[4]	P1_ AD[56]	AU
AV	NB	VSS_IO	VSS_IO	P1_ INTD#	P1_ AD[27]	VSS_IO	P1_CBE_ [1]#	P1_ SERR#	VSS_IO	P1_ AD[17]	VSS_IO	P1_ M66EN	VSS_IO	P1_AD[1]	VSS_IO	P1_ GNT#[2]	VSS_IO	P1_ AD[60]	VSS_IO	P1_ AD[51]	AV
AW	NB	NB	P1_ REQ#[1]	P1_ INTA#	P1_ INTB#	P1_ AD[21]	P1_ AD[31]	P1_ AD[26]	P1_ PME#	P1_ PERR#	P1_ CBE#[3]	P1_ AD[22]	P1_ CBE#[2]	P1_ AD[16]	P1_ ACK64#	P1_ AD[10]	P1_AD[5]	P1_ REQ#[3]	P1_ CBE#[6]	P1_ REQ64#	AW
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

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Figure 4. Ball Map - Right Side - Top View

Top View (Right Side)

	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	
A	SD_CLK[0]	SD_A[1]	SD_CLK[1]	SD_CLK[2]	SD_A[2]	SD_A[4]	SD_A[5]	SD_A[8]	SD_A[9]	SD_A[12]	SD_DQ[1]	SD_I2C_SDA	SD_DQ[8]	SD_CKFBI	SD_CS[4]#	SD_CS[7]#	SD_CS[6]#	NB	NB	A
B	SD_CLK[0]#	VSS_IO	SD_CLK[1]#	SD_CLK[2]#	VSS_IO	SD_A[3]	SD_A[6]	VSS_IO	SD_A[7]	SD_A[11]	VSS_IO	SD_A[13]#	SD_CS[5]#	VSS_IO	SD_CKFBO	PBI_AD[29]	VSS_IO	VSS_IO	NB	B
C	SD_DQ[26]	SD_DQ[28]	SD_DQ[25]	SD_DQ[11]	SD_DQ[18]	SD_DQS[2]	SD_DQ[21]	SD_DQ[20]	SD_DQ[2]	SD_DQ[6]	SD_DQS[9]	SD_I2C_CLK	SD_PWR DELAY	SD_DQ[4]	PBI_AD[31]	PBI_AD[27]	VSS_IO	VSS_IO	PBI_AD[24]	C
D	SD_DQS[12]	SD_DQ[29]	VSS_IO	SD_DQ[24]	SD_DQ[10]	VSS_IO	SD_DQS[10]	SD_DQ[13]	VSS_IO	SD_DQ[9]	SD_DQ[0]	SD_PLL_AVSS	PBI_AD[4]	PBI CS[3]#	PBI_AD[28]	VSS_IO	PBI_AD[23]	PBI_AD[25]	PBI_AD[19]	D
E	SD_ECC[5]	SD_ECC[4]	SD_DQ [19]	SD_DQ[22]	SD_DQ[15]	SD_DQ[14]	SD_DQ[16]	SD_DQ[3]	SD_DQS[0]	SD_DQ[7]	SD_DQ[5]	VSS_IO	PBI_AD[26]	PBI_AD[21]	VSS_IO	PBI_AD[22]	PBI_AD[18]	PBI_AD[20]	VSS_IO	E
F	VSS_IO	SD_ECC[0]	SD_DQ[23]	VSS_IO	SD_DQS[11]	SD_DQ[17]	VSS_IO	SD_DQS[1]	SD_DQ[12]	VSS_IO	VCC_SD	PBI_AD[30]	VCC_XS	VCC_XS	PBI_CS [0]#	PBI_AD[15]	PBI_CS [1]#	PBI_RW	PBI_AD[17]	F
G	VCC_SD	VCC_SD	VCC_SD	VCC_SD	VCC_SD	VCC_SD	VCC_SD	VCC_SD	VCC_SD	SD_PLL_AVCC	VCC_SD	PBI_LE	VCC_XS	VCC_XS	PBI_CS[2]#	PBI_AD[14]	VSS_IO	PBI_AD16	PBI_AD[13]	G
H	NB	NB	NB	NB	NB	NB	NB	NB	NB	VCC_CORE	VCC_CORE	VCC_CORE	VCC_XS	VCC_XS	PBI_AD[9]	PBI_AD[10]	PBI_AD[5]	PBI_AD[12]	PBI_AD[11]	H
J	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	VCC_CORE	VCC_XS	VCC_XS	NC_J35	PBI_OE#	PBI_AD[8]	XS_DQ[48]	VSS_IO	J
K	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	VCC_CORE	VCC_XS	NC_K34	PBI_RDY#	PBI_AD[0]	XS_DQ[49]	XS_CLK	XS_DQ[51]	K
L	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	XS_PLL_AVCC	PBI_AD[2]	VSS_IO	XS_DQ[50]	XS_DQ[52]	XS_DQ[20]	XS_DQ[53]	L
M	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NC_M33	XS_PLL_AVSS	PBI_AD[3]	XS_DQ[55]	XS_DQ[54]	VSS_IO	XS_DQ[23]	M
N	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	VCC_XS	PBI_AD[6]	VSS_IO	XS_DQ[19]	XS_DQ[18]	XS_DQ[16]	XS_DQ[22]	N
P	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	VCC_XS	PBI_AD[7]	PBI_AD[1]	XS_DQ[17]	XS_DQ[21]	VSS_IO	XS_DQ[47]	P
R	VSS_CORE	VCC_CORE	VSS_CORE	VCC_CORE	VSS_CORE	NB	NB	NB	NB	NB	NB	NB	VCC_XS	XS_DQ[45]	VSS_IO	XS_DQ[43]	XS_DQ[46]	XS_DQ[40]	XS_DQ[44]	R
T	VCC_CORE	VSS_CORE	VCC_CORE	VSS_CORE	VCC_CORE	NB	NB	NB	NB	NB	NB	NB	VCC_XS	XS_DQ[41]	XS_DQ[10]	XS_DQ[42]	XS_DQ[14]	VSS_IO	XS_DQ[15]	T
U	VSS_CORE	VCC_CORE	VSS_CORE	VCC_CORE	VSS_CORE	NB	NB	NB	NB	NB	NB	NB	VCC_XS	XS_DQ[13]	VSS_IO	XS_DQ[11]	XS_DQ[9]	XS_DQ[39]	XS_DQ[12]	U
V	VSS_CORE	VSS_CORE	VCC_CORE	VSS_CORE	VCC_CORE	NB	NB	NB	NB	NB	NB	NB	VCC_XS	XS_DQ[8]	XS_DQ[38]	XS_DQ[34]	XS_DQ[33]	VSS_IO	XS_DQ[36]	V
W	VSS_CORE	VSS_CORE	VSS_CORE	VCC_CORE	VSS_CORE	NB	NB	NB	NB	NB	NB	NB	VCC_XS	XS_DQ[37]	VSS_IO	XS_DQ[35]	XS_DQ[7]	XS_DQ[3]	XS_DQ[32]	W
Y	VSS_CORE	VSS_CORE	VCC_CORE	VSS_CORE	VCC_CORE	NB	NB	NB	NB	NB	NB	NB	VCC_XS	XS_DQ[6]	XS_DQ[0]	XS_DQ[2]	XS_DQ[1]	VSS_IO	XS_DQ[4]	Y
AA	VSS_CORE	VSS_CORE	VSS_CORE	VCC_CORE	VSS_CORE	NB	NB	NB	NB	NB	NB	NB	VCC_XS	XS_DQ[5]	VSS_IO	XS_DVALID[0]	XS_ECC[2]	XS_ECC[0]	XS_ECC[1]	AA
AB	VSS_CORE	VSS_CORE	VCC_CORE	VSS_CORE	VCC_CORE	NB	NB	NB	NB	NB	NB	NB	VCC_XS	XS_DVALID[1]	XS_ECC[3]	XS_ECC[5]	XS_ECC[7]	VSS_IO	XS_ECC[6]	AB
AC	VSS_CORE	VCC_CORE	VSS_CORE	VCC_CORE	VSS_CORE	NB	NB	NB	NB	NB	NB	NB	VCC_XS	XS_ECC[4]#	VSS_IO	XS_BE[0]	XS_BE[2]	XS_BE[5]	XS_BE[3]	AC
AD	VCC_CORE	VSS_CORE	VCC_CORE	VSS_CORE	VCC_CORE	NB	NB	NB	NB	NB	NB	NB	VCC_XS	XS_BE[1]	XS_LEN[2]	XS_LEN[0]	XS_LEN[1]	VSS_IO	XS_BE[4]	AD
AE	VSS_CORE	VCC_CORE	VSS_CORE	VCC_CORE	VSS_CORE	NB	NB	NB	NB	NB	NB	NB	VCC_XS	XS_BE[6]	VSS_IO	XS_BE[7]	XS_CWF	XS_HLDA[1]	XS_HOLD[0]	AE
AF	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	VCC_XS	XS_ABORT	XS_A[13]	XS_A[4]	XS_A[8]	VSS_IO	XS_HOLD[1]	AF
AG	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	VCC_XS	XS_HLDA[0]	VSS_IO	XS_A[12]	XS_A[3]	XS_A[1]	XS_A[2]	AG
AH	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	VCC_XS	XS_A[0]	XS_A[11]	XS_A[14]	XS_A[6]	VSS_IO	XS_A[7]	AH
AJ	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	VCC_XS	XS_A[5]	VSS_IO	XS_A[10]	XS_DQ[56]	XS_DQ[59]	XS_A[15]	AJ
AK	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	VCC_CORE	VCC_XS	XS_A[9]	XS_DQ[60]	XS_DQ[57]	XS_DQ[61]	VSS_IO	XS_DQ[62]	AK
AL	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	VCC_CORE	VCC_PC	U1_DTR	VSS_IO	XS_DQ[58]	XS_DQ[30]	XS_DQ[27]	XS_DQ[29]	AL
AM	NB	NB	NB	NB	NB	NB	NB	NB	NB	VCC_CORE	VCC_CORE	VCC_CORE	VCC_PC	U0_DCD#	U0_DTR#	XS_DQ[63]	XS_DQ[31]	VSS_IO	XS_DQ[28]	AM
AN	VCC_PC	VCC_PC	VCC_PC	VCC_PC	VCC_PC	VCC_PC	VCC_PC	VCC_PC	VCC_CORE	VCC_PC	VCC_PC	VCC_PC	VCC_PC	U1_DSR#	VSS_IO	U0_DSR#	XS_DQ[25]	XS_DQ[24]	XS_DQ[26]	AN
AP	P1_AD[52]	P1_AD[48]	P1_AD[42]	P1_REQ[7]#	SF_RST#	PWRUP_P1_ARB	PWRUP_TRANS	TDO	VCC_PC	VCC_PC	VCC_PC	INT[5]	VSS_IO	VSS_IO	U0_RX	U1_RX	U1_CTS#	XS_IRQ[1]	XS_IRQ[0]	AP
AR	P1_AD[53]	VSS_IO	P1_AD[43]	VSS_IO	PWRUP_P1_PRIM	PWRUP_P1_SWRST	TRST#	VSS_IO	NC	INT[1]	NC	INT[11]	NC	I2C_SDA	U0_TX	U0_CTS#	U0_RTS#	XS_C_FIQ[1]	XS_C_FIQ[0]	AR
AT	P1_AD[54]	P1_AD[49]	P1_AD[44]	P1_GNT[7]#	P1_GNT[6]#	P1_LED#	P1_HS_64EN#	TMS	TCK	NC	NC	NC	INT[7]	INT[14]	I2C_SCLK	VSS_IO	U1_RTS#	U0_RI#	XS_RESET#	AT
AU	P1_AD[46]	P1_AD[47]	P1_AD[38]	P1_AD[40]	P1_AD[34]	P1_AD[35]	P1_ES	P1_AD[32]	PWRUP_P2_PRIM	TDI	INT[2]	VSS_IO	INT[6]	INT[13]	INT[15]	PWRUP_P2_BYP	VSS_IO	VSS_IO	U1_DCD#	AU
AV	VSS_IO	P1_AD[41]	VSS_IO	P1_REQ[6]#	VSS_IO	P1_PCIXCAP [0]	P1_AD[33]	P1_AD[39]	VSS_IO	INT[0]	INT[3]	PWRUP_P1_BYP	INT[10]	INT[8]	INT[12]	U1_TX	VSS_IO	VSS_IO	NB	AV
AW	P1_AD[59]	P1_AD[55]	P1_AD[50]	P1_AD[45]	P1_AD[37]	PWRUP_P2_SWRST	P1_PCIXCAP [1]	PWRUP_XS_SWRST	PWRUP_PBI_BSWP	P1_AD[36]	SF_CLK	INT[9]	NC	PWRUP_P2_ARB	NC	INT[4]	U1_RI	NB	NB	AW
	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	

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Table 20. 1025-Lead HSBGA Package — Alphabetical Ball Listing

Table 20 1025-Lead HSBGA Package — Alphabetical Ball Listing (Sheet 1 of 30)	
Ball	**Signal Name**
A3	E0_ECMDT
A4	E0_TCG[5]
A5	E0_TCG[3]
A6	SD_DQ[63]
A7	SD_DQS[6]
A8	SD_VREF
A9	SD_DQS[7]
A10	SD_DQ[57]
A11	SD_DQ[60]
A12	SD_DQ[46]
A13	SD_CAS#
A14	SD_CS#[0]
A15	SD_CS#[2]
A16	SD_WE#
A17	SD_BA[0]
A18	SD_CLK[3]
A19	SD_BA[1]
A20	SD_A[0]
A21	SD_CLK[0]
A22	SD_A[1]
A23	SD_CLK[1]
A24	SD_CLK[2]
A25	SD_A[2]
A26	SD_A[4]
A27	SD_A[5]
A28	SD_A[8]
A29	SD_A[9]
A30	SD_A[12]
A31	SD_DQ[1]
A32	SD_I2C_SDA
A33	SD_DQ[8]
A34	SD_CKFBI
A35	SD_CS#[4]
A36	SD_CS#[7]

Table 20 1025-Lead HSBGA Package — Alphabetical Ball Listing (Sheet 2 of 30)	
Ball	**Signal Name**
A37	SD_CS#[6]
B2	VSS_IO
B3	VSS_IO
B4	E0_TCG[1]
B5	MDIO
B6	E0_TCG[9]
B7	VSS_IO
B8	SD_DQ[62]
B9	SD_CLKEN
B10	VSS_IO
B11	SD_DQ[56]
B12	SD_DQ[43]
B13	VSS_IO
B14	SD_CS#[1]
B15	SD_CS#[3]
B16	VSS_IO
B17	SD_RAS#
B18	SD_CLK#[3]
B19	VSS_IO
B20	SD_A[10]
B21	SD_CLK#[0]
B22	VSS_IO
B23	SD_CLK#[1]
B24	SD_CLK#[2]
B25	VSS_IO
B26	SD_A[3]
B27	SD_A[6]
B28	VSS_IO
B29	SD_A[7]
B30	SD_A[11]
B31	VSS_IO
B32	SD_A[13]
B33	SD_CS#[5]
B34	VSS_IO

Table 20 1025-Lead HSBGA Package — Alphabetical Ball Listing (Sheet 3 of 30)	
Ball	**Signal Name**
B35	SD_CKFBO
B36	PBI_AD[29]
B37	VSS_IO
B38	VSS_IO
C1	E0_RCG[3]
C2	VSS_IO
C3	VSS_IO
C4	E0_PMA_CLK1
C5	MDC
C6	E0_PRBSEN
C7	SD_DQS[15]
C8	SD_DQ[58]
C9	SD_DQ[53]
C10	SD_DQ[49]
C11	SD_DQ[48]
C12	SD_DQ[35]
C13	SD_DQ[38]
C14	SD_DQS[14]
C15	SD_DQS[4]
C16	SD_DQ[37]
C17	SD_DQ[32]
C18	SD_ECC[3]
C19	SD_ECC[2]
C20	SD_DQS[8]
C21	SD_DQ[26]
C22	SD_DQ[28]
C23	SD_DQ[25]
C24	SD_DQ[11]
C25	SD_DQ[18]
C26	SD_DQS[2]
C27	SD_DQ[21]
C28	SD_DQ[20]
C29	SD_DQ[2]
C30	SD_DQ[6]

Table 20 1025-Lead HSBGA Package — Alphabetical Ball Listing (Sheet 4 of 30)	
Ball	**Signal Name**
C31	SD_DQS[9]
C32	SD_I2C_CLK
C33	SD_PWRDELAY
C34	SD_DQ[4]
C35	PBI_AD[31]
C36	PBI_AD[27]
C37	VSS_IO
C38	VSS_IO
C39	PBI_AD[24]
D1	E0_PCOL_RBCM
D2	E0_TCG[7]
D3	E0_PCRS_SDET
D4	VSS_IO
D5	E0_PRBS_PASS
D6	E0_TCG[2]
D7	E0_TCG[8]
D8	SD_DQ[52]
D9	SD_DQ[54]
D10	SD_DQ[55]
D11	SD_DQ[50]
D12	SD_DQ[51]
D13	SD_DQ[39]
D14	VSS_IO
D15	SD_DQS[13]
D16	SD_DQ[33]
D17	VSS_IO
D18	SD_ECC[6]
D19	SD_DQ[27]
D20	VSS_IO
D21	SD_DQS[12]
D22	SD_DQ[29]
D23	VSS_IO
D24	SD_DQ[24]
D25	SD_DQ[10]
D26	VSS_IO

Table 20 1025-Lead HSBGA Package — Alphabetical Ball Listing (Sheet 5 of 30)	
Ball	**Signal Name**
D27	SD_DQS[10]
D28	SD_DQ[13]
D29	VSS_IO
D30	SD_DQ[9]
D31	SD_DQ[0]
D32	SD_PLL_AVSS
D33	PBI_AD[4]
D34	PBI_CS#[3]
D35	PBI_AD[28]
D36	VSS_IO
D37	PBI_AD[23]
D38	PBI_AD[25]
D39	PBI_AD[19]
E1	E0_RCG[1]
E2	E0_EWRAP
E3	E0_TCG[4]
E4	E0_TCG[0]
E5	E0_RCG[0]
E6	VSS_IO
E7	E1_PCOL_RBCM
E8	VSS_IO
E9	SD_DQ[59]
E10	SD_DQS[16]
E11	VSS_IO
E12	SD_DQ[47]
E13	SD_DQS[5]
E14	SD_DQ[34]
E15	SD_DQ[45]
E16	SD_DQ[44]
E17	SD_ECC[7]
E18	SD_DQ[31]
E19	SD_DQS[17]
E20	SD_ECC[1]
E21	SD_ECC[5]
E22	SD_ECC[4]

Table 20 1025-Lead HSBGA Package — Alphabetical Ball Listing (Sheet 6 of 30)	
Ball	**Signal Name**
E23	SD_DQ[19]
E24	SD_DQ[22]
E25	SD_DQ[15]
E26	SD_DQ[14]
E27	SD_DQ[16]
E28	SD_DQ[3]
E29	SD_DQS[0]
E30	SD_DQ[7]
E31	SD_DQ[5]
E32	VSS_IO
E33	PBI_AD[26]
E34	PBI_AD[21]
E35	VSS_IO
E36	PBI_AD[22]
E37	PBI_AD[18]
E38	PBI_AD[20]
E39	VSS_IO
F1	E0_RCG[4]
F2	E0_RCG[5]
F3	E1_TCG[5]
F4	E0_RCG[6]
F5	E0_RCG[2]
F6	VCC_PC
F7	VCC_CORE
F8	E0_TCG[6]
F9	VCC_SD
F10	VCC_SD
F11	VCC_SD
F12	SD_DQ[61]
F13	SD_DQ[42]
F14	SD_DQ[41]
F15	VSS_IO
F16	SD_DQ[40]
F17	SD_DQ[36]
F18	VSS_IO

Table 20
1025-Lead HSBGA Package — Alphabetical Ball Listing
(Sheet 7 of 30)

Ball	Signal Name
F19	SD_DQ[30]
F20	SD_DQS[3]
F21	VSS_IO
F22	SD_ECC[0]
F23	SD_DQ[23]
F24	VSS_IO
F25	SD_DQS[11]
F26	SD_DQ[17]
F27	VSS_IO
F28	SD_DQS[1]
F29	SD_DQ[12]
F30	VSS_IO
F31	VCC_SD
F32	PBI_AD[30]
F33	VCC_XS
F34	VCC_XS
F35	PBI_CS#[0]
F36	PBI_AD[15]
F37	PBI_CS#[1]
F38	PBI_RW
F39	PBI_AD[17]
G1	E0_RCG[8]
G2	E0_RCG[9]
G3	VSS_IO
G4	E1_TCG[9]
G5	E0_PMA_CLK0
G6	VCC_PC
G7	VCC_CORE
G8	VCC_CORE
G9	VCC_SD
G10	VCC_SD
G11	VCC_SD
G12	VCC_SD
G13	VCC_SD
G14	VCC_SD

Table 20
1025-Lead HSBGA Package — Alphabetical Ball Listing
(Sheet 8 of 30)

Ball	Signal Name
G15	VCC_SD
G16	VCC_SD
G17	VCC_SD
G18	VCC_SD
G19	VCC_SD
G20	VCC_SD
G21	VCC_SD
G22	VCC_SD
G23	VCC_SD
G24	VCC_SD
G25	VCC_SD
G26	VCC_SD
G27	VCC_SD
G28	VCC_SD
G29	VCC_SD
G30	SD_PLL_AVCC
G31	VCC_SD
G32	PBI_LE
G33	VCC_XS
G34	VCC_XS
G35	PBI_CS#[2]
G36	PBI_AD[14]
G37	VSS_IO
G38	PBI_AD[16]
G39	PBI_AD[13]
H1	E0_RCG[7]
H2	E1_TCG[3]
H3	E1_TCG[4]
H4	E1_TCG[1]
H5	E1_TCG[7]
H6	VCC_PC
H7	VCC_PC
H8	VCC_CORE
H9	VCC_CORE
H10	VCC_CORE

Table 20
1025-Lead HSBGA Package — Alphabetical Ball Listing
(Sheet 9 of 30)

Ball	Signal Name
H30	VCC_CORE
H31	VCC_CORE
H32	VCC_CORE
H33	VCC_XS
H34	VCC_XS
H35	PBI_AD[9]
H36	PBI_AD[10]
H37	PBI_AD[5]
H38	PBI_AD[12]
H39	PBI_AD[11]
J1	E1_TCG[2]
J2	E1_PMA_CLK1
J3	E1_RCG[2]
J4	E1_TCG[8]
J5	E1_TCG[0]
J6	VCC_PC
J7	VCC_CORE
J8	VCC_CORE
J32	VCC_CORE
J33	VCC_XS
J34	VCC_XS
J35	NC_J35
J36	PBI_OE#
J37	PBI_AD[8]
J38	XS_DQ[48]
J39	VSS_IO
K1	E1_TCG[6]
K2	E1_EWRAP
K3	VSS_IO
K4	REF125M
K5	E1_RCG[5]
K6	VCC_PC
K7	VCC_CORE
K8	VCC_CORE
K32	VCC_CORE

Table 20 1025-Lead HSBGA Package — Alphabetical Ball Listing (Sheet 10 of 30)	
Ball	**Signal Name**
K33	VCC_XS
k34	NC_K34
K35	PBI_RDY#
K36	PBI_AD[0]
K37	XS_DQ[49]
K38	XS_CLK
K39	XS_DQ[51]
L1	P2_INTD#
L2	E1_RCG[1]
L3	E1_RCG[0]
L4	GTX_CLK
L5	E1_PRBSEN
L6	NC_L6
L7	VCC_CORE
L33	XS_PLL_AVCC
L34	PBI_AD[2]
L35	VSS_IO
L36	XS_DQ[50]
L37	XS_DQ[52]
L38	XS_DQ[20]
L39	XS_DQ[53]
M1	P2_GNT#[1]
M2	P2_REQ#[1]
M3	E1_PMA_CLK0
M4	E1_RCG[4]
M5	E1_RCG[7]
M6	VSS_IO
M7	VCC_PC
M33	NC_M33
M34	XS_PLL_AVSS
M35	PBI_AD[3]
M36	XS_DQ[55]
M37	XS_DQ[54]
M38	VSS_IO
M39	XS_DQ[23]

Table 20 1025-Lead HSBGA Package — Alphabetical Ball Listing (Sheet 11 of 30)	
Ball	**Signal Name**
N1	P2_INTB#
N2	VSS_IO
N3	E1_PCRS_SDET
N4	E1_RCG[3]
N5	E1_PRBS_PASS
N6	NC_N6
N7	VCC_PC
N33	VCC_XS
N34	PBI_AD[6]
N35	VSS_IO
N36	XS_DQ[19]
N37	XS_DQ[18]
N38	XS_DQ[16]
N39	XS_DQ[22]
P1	P2_AD[31]
P2	P2_RST#
P3	P2_INTA#
P4	E1_ECMDT
P5	E1_RCG[8]
P6	E1_RCG[6]
P7	VCC_PC
P33	VCC_XS
P34	PBI_AD[7]
P35	PBI_AD[1]
P36	XS_DQ[17]
P37	XS_DQ[21]
P38	VSS_IO
P39	XS_DQ[47]
R1	P2_AD[26]
R2	P2_HEALTHY#
R3	P2_IDSEL
R4	P2_AD[30]
R5	VSS_IO
R6	E1_RCG[9]
R7	VCC_PC

Table 20 1025-Lead HSBGA Package — Alphabetical Ball Listing (Sheet 12 of 30)	
Ball	**Signal Name**
R15	VSS_CORE
R16	VCC_CORE
R17	VSS_CORE
R18	VCC_CORE
R19	VSS_CORE
R20	VCC_CORE
R21	VSS_CORE
R22	VCC_CORE
R23	VSS_CORE
R24	VCC_CORE
R25	VSS_CORE
R33	VCC_XS
R34	XS_DQ[45]
R35	VSS_IO
R36	XS_DQ[43]
R37	XS_DQ[46]
R38	XS_DQ[40]
R39	XS_DQ[44]
T1	P2_PME#
T2	P2_AD[27]
T3	P2_AD[28]
T4	P2_AD[24]
T5	P2_CLK_IN
T6	P2_PLL_AVSS
T7	VCC_PC
T15	VCC_CORE
T16	VSS_CORE
T17	VCC_CORE
T18	VSS_CORE
T19	VCC_CORE
T20	VSS_CORE
T21	VCC_CORE
T22	VSS_CORE
T23	VCC_CORE
T24	VSS_CORE

Table 20
1025-Lead HSBGA Package — Alphabetical Ball Listing
(Sheet 13 of 30)

Ball	Signal Name
T25	VCC_CORE
T33	VCC_XS
T34	XS_DQ[41]
T35	XS_DQ[10]
T36	XS_DQ[42]
T37	XS_DQ[14]
T38	VSS_IO
T39	XS_DQ[15]
U1	P2_AD[21]
U2	VSS_IO
U3	P2_INTC#
U4	P2_IRDY#
U5	VSS_IO
U6	P2_CLK_OUT
U7	VCC_PC
U15	VSS_CORE
U16	VCC_CORE
U17	VSS_CORE
U18	VCC_CORE
U19	VSS_CORE
U20	VCC_CORE
U21	VSS_CORE
U22	VCC_CORE
U23	VSS_CORE
U24	VCC_CORE
U25	VSS_CORE
U33	VCC_XS
U34	XS_DQ[13]
U35	VSS_IO
U36	XS_DQ[11]
U37	XS_DQ[9]
U38	XS_DQ[39]
U39	XS_DQ[12]
V1	P2_CBE#[3]
V2	P2_CBE#[1]

Table 20
1025-Lead HSBGA Package — Alphabetical Ball Listing
(Sheet 14 of 30)

Ball	Signal Name
V3	P2_AD[25]
V4	P2_AD[29]
V5	P2_AD[23]
V6	P2_PLL_AVCC
V7	VCC_PC
V15	VCC_CORE
V16	VSS_CORE
V17	VCC_CORE
V18	VSS_CORE
V19	VSS_CORE
V20	VSS_CORE
V21	VSS_CORE
V22	VSS_CORE
V23	VCC_CORE
V24	VSS_CORE
V25	VCC_CORE
V33	VCC_XS
V34	XS_DQ[8]
V35	XS_DQ[38]
V36	XS_DQ[34]
V37	XS_DQ[33]
V38	VSS_IO
V39	XS_DQ[36]
W1	P2_AD[22]
W2	P2_SERR#
W3	P2_AD[20]
W4	P2_AD[18]
W5	VSS_IO
W6	P2_DEVSEL#
W7	VCC_PC
W15	VSS_CORE
W16	VCC_CORE
W17	VSS_CORE
W18	VSS_CORE
W19	VSS_CORE

Table 20
1025-Lead HSBGA Package — Alphabetical Ball Listing
(Sheet 15 of 30)

Ball	Signal Name
W20	VSS_CORE
W21	VSS_CORE
W22	VSS_CORE
W23	VSS_CORE
W24	VCC_CORE
W25	VSS_CORE
W33	VCC_XS
W34	XS_DQ[37]
W35	VSS_IO
W36	XS_DQ[35]
W37	XS_DQ[7]
W38	XS_DQ[3]
W39	XS_DQ[32]
Y1	P2_CBE#[2]
Y2	VSS_IO
Y3	P2_AD[19]
Y4	P2_FRAME#
Y5	P2_AD[15]
Y6	P2_TRDY#
Y7	VCC_PC
Y15	VCC_CORE
Y16	VSS_CORE
Y17	VCC_CORE
Y18	VSS_CORE
Y19	VSS_CORE
Y20	VSS_CORE
Y21	VSS_CORE
Y22	VSS_CORE
Y23	VCC_CORE
Y24	VSS_CORE
Y25	VCC_CORE
Y33	VCC_XS
Y34	XS_DQ[6]
Y35	XS_DQ[0]
Y36	XS_DQ[2]

Table 20 1025-Lead HSBGA Package — Alphabetical Ball Listing (Sheet 16 of 30)	
Ball	**Signal Name**
Y37	XS_DQ[1]
Y38	VSS_IO
Y39	XS_DQ[4]
AA1	P2_AD[16]
AA2	P2_AD[17]
AA3	P2_PERR#
AA4	P2_PAR
AA5	P2_RSTDIR
AA6	P2_STOP#
AA7	VCC_PC
AA15	VSS_CORE
AA16	VCC_CORE
AA17	VSS_CORE
AA18	VSS_CORE
AA19	VSS_CORE
AA20	VSS_CORE
AA21	VSS_CORE
AA22	VSS_CORE
AA23	VSS_CORE
AA24	VCC_CORE
AA25	VSS_CORE
AA33	VCC_XS
AA34	XS_DQ[5]
AA35	VSS_IO
AA36	XS_DVALID[0]
AA37	XS_ECC[2]
AA38	XS_ECC[0]
AA39	XS_ECC[1]
AB1	P2_ACK64#
AB2	P2_AD[12]
AB3	P2_AD[13]
AB4	P2_AD[9]
AB5	VSS_IO
AB6	P2_AD[14]
AB7	VCC_PC

Table 20 1025-Lead HSBGA Package — Alphabetical Ball Listing (Sheet 17 of 30)	
Ball	**Signal Name**
AB15	VCC_CORE
AB16	VSS_CORE
AB17	VCC_CORE
AB18	VSS_CORE
AB19	VSS_CORE
AB20	VSS_CORE
AB21	VSS_CORE
AB22	VSS_CORE
AB23	VCC_CORE
AB24	VSS_CORE
AB25	VCC_CORE
AB33	VCC_XS
AB34	XS_DVALID[1]
AB35	XS_ECC[3]
AB36	XS_ECC[5]
AB37	XS_ECC[7]
AB38	VSS_IO
AB39	XS_ECC[6]
AC1	P2_AD[10]
AC2	VSS_IO
AC3	P2_CBE#[0]
AC4	P2_AD[3]
AC5	P2_AD[8]
AC6	P2_AD[11]
AC7	VCC_PC
AC15	VSS_CORE
AC16	VCC_CORE
AC17	VSS_CORE
AC18	VCC_CORE
AC19	VSS_CORE
AC20	VCC_CORE
AC21	VSS_CORE
AC22	VCC_CORE
AC23	VSS_CORE
AC24	VCC_CORE

Table 20 1025-Lead HSBGA Package — Alphabetical Ball Listing (Sheet 18 of 30)	
Ball	**Signal Name**
AC25	VSS_CORE
AC33	VCC_XS
AC34	XS_ECC[4]
AC35	VSS_IO
AC36	XS_BE[0]
AC37	XS_BE[2]
AC38	XS_BE[5]
AC39	XS_BE[3]
AD1	P2_AD[5]
AD2	P2_M66EN
AD3	P2_AD[6]
AD4	P2_AD[4]
AD5	P2_CBE#[7]
AD6	P2_AD[7]
AD7	VCC_PC
AD15	VCC_CORE
AD16	VSS_CORE
AD17	VCC_CORE
AD18	VSS_CORE
AD19	VCC_CORE
AD20	VSS_CORE
AD21	VCC_CORE
AD22	VSS_CORE
AD23	VCC_CORE
AD24	VSS_CORE
AD25	VCC_CORE
AD33	VCC_XS
AD34	XS_BE[1]
AD35	XS_LEN[2]
AD36	XS_LEN[0]
AD37	XS_LEN[1]
AD38	VSS_IO
AD39	XS_BE[4]
AE1	P2_CBE#[6]
AE2	P2_AD[1]

Table 20
1025-Lead HSBGA Package — Alphabetical Ball Listing
(Sheet 19 of 30)

Ball	Signal Name
AE3	P2_AD[0]
AE4	P2_REQ#[3]
AE5	VSS_IO
AE6	P2_AD[2]
AE7	VCC_PC
AE15	VSS_CORE
AE16	VCC_CORE
AE17	VSS_CORE
AE18	VCC_CORE
AE19	VSS_CORE
AE20	VCC_CORE
AE21	VSS_CORE
AE22	VCC_CORE
AE23	VSS_CORE
AE24	VCC_CORE
AE25	VSS_CORE
AE33	VCC_XS
AE34	XS_BE[6]
AE35	VSS_IO
AE36	XS_BE[7]
AE37	XS_CWF
AE38	XS_HLDA[1]
AE39	XS_HOLD[0]
AF1	P2_REQ#[4]
AF2	VSS_IO
AF3	P2_GNT#[2]
AF4	P2_REQ#[5]
AF5	P2_GNT#[4]
AF6	P2_ENUM#
AF7	VCC_PC
AF33	VCC_XS
AF34	XS_ABORT
AF35	XS_A[13]
AF36	XS_A[4]
AF37	XS_A[8]

Table 20
1025-Lead HSBGA Package — Alphabetical Ball Listing
(Sheet 20 of 30)

Ball	Signal Name
AF38	VSS_IO
AF39	XS_HOLD[1]
AG1	P2_CBE#[4]
AG2	P2_GNT#[5]
AG3	P2_GNT#[3]
AG4	P2_AD[61]
AG5	VSS_IO
AG6	P2_REQ#[2]
AG7	VCC_PC
AG33	VCC_XS
AG34	XS_HLDA[0]
AG35	VSS_IO
AG36	XS_A[12]
AG37	XS_A[3]
AG38	XS_A[1]
AG39	XS_A[2]
AH1	P2_AD[59]
AH2	VSS_IO
AH3	P2_AD[63]
AH4	P2_AD[62]
AH5	P2_AD[58]
AH6	P2_PAR64
AH7	VCC_PC
AH33	VCC_XS
AH34	XS_A[0]
AH35	XS_A[11]
AH36	XS_A[14]
AH37	XS_A[6]
AH38	VSS_IO
AH39	XS_A[7]
AJ1	P2_AD[55]
AJ2	P2_AD[60]
AJ3	P2_AD[56]
AJ4	P2_AD[53]
AJ5	VSS_IO

Table 20
1025-Lead HSBGA Package — Alphabetical Ball Listing
(Sheet 21 of 30)

Ball	Signal Name
AJ6	P2_CBE#[5]
AJ7	VCC_PC
AJ33	VCC_XS
AJ34	XS_A[5]
AJ35	VSS_IO
AJ36	XS_A[10]
AJ37	XS_DQ[56]
AJ38	XS_DQ[59]
AJ39	XS_A[15]
AK1	P2_AD[50]
AK2	VSS_IO
AK3	P2_REQ64#
AK4	P2_AD[54]
AK5	P2_AD[49]
AK6	P2_AD[57]
AK7	VCC_PC
AK8	VCC_CORE
AK32	VCC_CORE
AK33	VCC_XS
AK34	XS_A[9]
AK35	XS_DQ[60]
AK36	XS_DQ[57]
AK37	XS_DQ[61]
AK38	VSS_IO
AK39	XS_DQ[62]
AL1	P2_AD[46]
AL2	P2_AD[51]
AL3	P2_AD[44]
AL4	P2_AD[43]
AL5	VSS_IO
AL6	P2_AD[52]
AL7	VCC_PC
AL8	VCC_CORE
AL32	VCC_CORE
AL33	VCC_PC

Table 20 1025-Lead HSBGA Package — Alphabetical Ball Listing (Sheet 22 of 30)	
Ball	**Signal Name**
AL34	U1_DTR#
AL35	VSS_IO
AL36	XS_DQ[58]
AL37	XS_DQ[30]
AL38	XS_DQ[27]
AL39	XS_DQ[29]
AM1	P2_AD[45]
AM2	VSS_IO
AM3	P2_AD[47]
AM4	P2_AD[40]
AM5	P2_AD[39]
AM6	P2_AD[48]
AM7	VCC_PC
AM8	VCC_CORE
AM9	VCC_CORE
AM10	VCC_CORE
AM30	VCC_CORE
AM31	VCC_CORE
AM32	VCC_CORE
AM33	VCC_PC
AM34	U0_DCD#
AM35	U0_DTR#
AM36	XS_DQ[63]
AM37	XS_DQ[31]
AM38	VSS_IO
AM39	XS_DQ[28]
AN1	P2_AD[37]
AN2	P2_AD[41]
AN3	P2_AD[35]
AN4	P2_LED#
AN5	VSS_IO
AN6	P2_AD[42]
AN7	VSS_IO
AN8	VCC_PC
AN9	VCC_PC

Table 20 1025-Lead HSBGA Package — Alphabetical Ball Listing (Sheet 23 of 30)	
Ball	**Signal Name**
AN10	VCC_PC
AN11	VCC_PC
AN12	VCC_PC
AN13	VCC_PC
AN14	VCC_PC
AN15	VCC_PC
AN16	VCC_PC
AN17	VCC_PC
AN18	VCC_PC
AN19	VCC_PC
AN20	VCC_PC
AN21	VCC_PC
AN22	VCC_PC
AN23	VCC_PC
AN24	VCC_PC
AN25	VCC_PC
AN26	VCC_PC
AN27	VCC_PC
AN28	VCC_PC
AN29	VCC_CORE
AN30	VCC_PC
AN31	VCC_PC
AN32	VCC_PC
AN33	VCC_PC
AN34	U1_DSR#
AN35	VSS_IO
AN36	U0_DSR#
AN37	XS_DQ[25]
AN38	XS_DQ[24]
AN39	XS_DQ[26]
AP1	P2_AD[34]
AP2	VSS_IO
AP3	P2_AD[38]
AP4	P2_AD[32]
AP5	P2_AD[33]

Table 20 1025-Lead HSBGA Package — Alphabetical Ball Listing (Sheet 24 of 30)	
Ball	**Signal Name**
AP6	P2_AD[36]
AP7	P1_PLL_AVSS
AP8	P1_CLK_OUT
AP9	P1_PLL_AVCC
AP10	P1_TRDY#
AP11	P1_STOP#
AP12	P1_AD[14]
AP13	P1_AD[11]
AP14	P1_AD[7]
AP15	P1_AD[2]
AP16	P1_ENUM#
AP17	P1_REQ#[4]
AP18	P1_PAR64
AP19	P1_CBE#[5]
AP20	P1_AD[57]
AP21	P1_AD[52]
AP22	P1_AD[48]
AP23	P1_AD[42]
AP24	P1_REQ#[7]
AP25	SF_RST#
AP26	PWRUP_P1_ARB
AP27	PWRUP_TRANS
AP28	TDO
AP29	VCC_PC
AP30	VCC_PC
AP31	VCC_PC
AP32	INT[5]
AP33	VSS_IO
AP34	VSS_IO
AP35	U0_RX
AP36	U1_RX
AP37	U1_CTS#
AP38	XS_IRQ[1]
AP39	XS_IRQ[0]
AR1	P2_GNT#[6]

Table 20
1025-Lead HSBGA Package — Alphabetical Ball Listing
(Sheet 25 of 30)

Ball	Signal Name
AR2	P2_REQ#[7]
AR3	P2_REQ#[6]
AR4	P2_GNT#[7]
AR5	VSS_IO
AR6	P1_AD[29]
AR7	P1_CLK_IN
AR8	P1_AD[23]
AR9	P1_DEVSEL#
AR10	VSS_IO
AR11	P1_FRAME#
AR12	VSS_IO
AR13	P1_RSTDIR
AR14	VSS_IO
AR15	P1_AD[3]
AR16	VSS_IO
AR17	P1_GNT#[4]
AR18	VSS_IO
AR19	P1_AD[61]
AR20	VSS_IO
AR21	P1_AD[53]
AR22	VSS_IO
AR23	P1_AD[43]
AR24	VSS_IO
AR25	PWRUP_P1_PRIM
AR26	PWRUP_P1_SWRST
AR27	TRST#
AR28	VSS_IO
AR29	NC
AR30	INT[1]
AR31	NC
AR32	INT[11]
AR33	NC
AR34	I2C_SDA
AR35	U0_TX
AR36	U0_CTS#

Table 20
1025-Lead HSBGA Package — Alphabetical Ball Listing
(Sheet 26 of 30)

Ball	Signal Name
AR37	U0_RTS#
AR38	XS_FIQ[1]
AR39	XS_FIQ[0]
AT1	P2_HS_64EN#
AT2	P2_PCIXCAP[1]
AT3	P2_PCIXCAP[0]
AT4	VSS_IO
AT5	P1_RST#
AT6	P1_GNT#[1]
AT7	P1_AD[30]
AT8	P1_AD[24]
AT9	P1_IRDY#
AT10	P1_AD[18]
AT11	P1_PAR
AT12	P1_AD[15]
AT13	P1_AD[9]
AT14	P1_AD[8]
AT15	P1_AD[4]
AT16	P1_REQ#[2]
AT17	P1_REQ#[5]
AT18	P1_CBE#[7]
AT19	P1_AD[62]
AT20	P1_AD[58]
AT21	P1_AD[54]
AT22	P1_AD[49]
AT23	P1_AD[44]
AT24	P1_GNT#[7]
AT25	P1_GNT#[6]
AT26	P1_LED#
AT27	P1_HS_64EN#
AT28	TMS
AT29	TCK
AT30	NC
AT31	NC
AT32	NC

Table 20
1025-Lead HSBGA Package — Alphabetical Ball Listing
(Sheet 27 of 30)

Ball	Signal Name
AT33	INT[7]
AT34	INT[14]
AT35	I2C_SCLK
AT36	VSS_IO
AT37	U1_RTS#
AT38	U0_RI#
AT39	XS_RESET#
AU1	P2_ES
AU2	VSS_IO
AU3	VSS_IO
AU4	P1_IDSEL
AU5	P1_AD[28]
AU6	P1_HEALTHY#
AU7	P1_INTC#
AU8	P1_AD[25]
AU9	P1_AD[20]
AU10	P1_AD[19]
AU11	P1_AD[12]
AU12	P1_AD[13]
AU13	P1_AD[6]
AU14	P1_CBE#[0]
AU15	P1_GNT#[5]
AU16	P1_AD[0]
AU17	P1_AD[63]
AU18	P1_GNT#[3]
AU19	P1_CBE#[4]
AU20	P1_AD[56]
AU21	P1_AD[46]
AU22	P1_AD[47]
AU23	P1_AD[38]
AU24	P1_AD[40]
AU25	P1_AD[34]
AU26	P1_AD[35]
AU27	P1_ES
AU28	P1_AD[32]

Table 20 1025-Lead HSBGA Package — Alphabetical Ball Listing (Sheet 28 of 30)	
Ball	**Signal Name**
AU29	PWRUP_P2_PRIM
AU30	TDI
AU31	INT[2]
AU32	VSS_IO
AU33	INT[6]
AU34	INT[13]
AU35	INT[15]
AU36	PWRUP_P2_BYP
AU37	VSS_IO
AU38	VSS_IO
AU39	U1_DCD#
AV2	VSS_IO
AV3	VSS_IO
AV4	P1_INTD#
AV5	P1_AD[27]
AV6	VSS_IO
AV7	P1_CBE#[1]
AV8	P1_SERR#
AV9	VSS_IO
AV10	P1_AD[17]
AV11	VSS_IO
AV12	P1_M66EN
AV13	VSS_IO
AV14	P1_AD[1]
AV15	VSS_IO
AV16	P1_GNT#[2]
AV17	VSS_IO
AV18	P1_AD[60]
AV19	VSS_IO
AV20	P1_AD[51]
AV21	VSS_IO
AV22	P1_AD[41]
AV23	VSS_IO
AV24	P1_REQ#[6]
AV25	VSS_IO

Table 20 1025-Lead HSBGA Package — Alphabetical Ball Listing (Sheet 29 of 30)	
Ball	**Signal Name**
AV26	P1_PCIXCAP[0]
AV27	P1_AD[33]
AV28	P1_AD[39]
AV29	VSS_IO
AV30	INT[0]
AV31	INT[3]
AV32	PWRUP_P1_BYP
AV33	INT[10]
AV34	INT[8]
AV35	INT[12]
AV36	U1_TX
AV37	VSS_IO
AV38	VSS_IO
AW3	P1_REQ#[1]
AW4	P1_INTA#
AW5	P1_INTB#
AW6	P1_AD[21]
AW7	P1_AD[31]
AW8	P1_AD[26]
AW9	P1_PME#
AW10	P1_PERR#
AW11	P1_CBE#[3]
AW12	P1_AD[22]
AW13	P1_CBE#[2]
AW14	P1_AD[16]
AW15	P1_ACK64#
AW16	P1_AD[10]
AW17	P1_AD[5]
AW18	P1_REQ#[3]
AW19	P1_CBE#[6]
AW20	P1_REQ64#
AW21	P1_AD[59]
AW22	P1_AD[55]
AW23	P1_AD[50]
AW24	P1_AD[45]

Table 20 1025-Lead HSBGA Package — Alphabetical Ball Listing (Sheet 30 of 30)	
Ball	**Signal Name**
AW25	P1_AD[37]
AW26	PWRUP_P2_SWRST
AW27	P1_PCIXCAP[1]
AW28	PWRUP_XS_SWRST
AW29	PWRUP_PBI_BSWP
AW30	P1_AD[36]
AW31	SF_CLK
AW32	INT[9]
AW33	SRAM_SKU
AW34	PWRUP_P2_ARB
AW35	NC
AW36	INT[4]
AW37	U1_RI#

Table 21. 1025-Lead HSBGA Package — Alphabetical Signal Listing

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 1 of 30)	
Signal Name	**Ball**
E0_ECMDT	A3
E0_EWRAP	E2
E0_PCOL_RBCM	D1
E0_PCRS_SDET	D3
E0_PMA_CLK0	G5
E0_PMA_CLK1	C4
E0_PRBS_PASS	D5
E0_PRBSEN	C6
E0_RCG[0]	E5
E0_RCG[1]	E1
E0_RCG[2]	F5
E0_RCG[3]	C1
E0_RCG[4]	F1
E0_RCG[5]	F2
E0_RCG[6]	F4
E0_RCG[7]	H1
E0_RCG[8]	G1
E0_RCG[9]	G2
E0_TCG[0]	E4
E0_TCG[1]	B4
E0_TCG[2]	D6
E0_TCG[3]	A5
E0_TCG[4]	E3
E0_TCG[5]	A4
E0_TCG[6]	F8
E0_TCG[7]	D2
E0_TCG[8]	D7
E0_TCG[9]	B6
E1_ECMDT	P4
E1_EWRAP	K2
E1_PCOL_RBCM	E7
E1_PCRS_SDET	N3
E1_PMA_CLK0	M3
E1_PMA_CLK1	J2

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 2 of 30)	
Signal Name	**Ball**
E1_PRBS_PASS	N5
E1_PRBSEN	L5
E1_RCG[0]	L3
E1_RCG[1]	L2
E1_RCG[2]	J3
E1_RCG[3]	N4
E1_RCG[4]	M4
E1_RCG[5]	K5
E1_RCG[6]	P6
E1_RCG[7]	M5
E1_RCG[8]	P5
E1_RCG[9]	R6
E1_TCG[0]	J5
E1_TCG[1]	H4
E1_TCG[2]	J1
E1_TCG[3]	H2
E1_TCG[4]	H3
E1_TCG[5]	F3
E1_TCG[6]	K1
E1_TCG[7]	H5
E1_TCG[8]	J4
E1_TCG[9]	G4
GTX_CLK	L4
I2C_SCLK	AT35
I2C_SDA	AR34
INT[0]	AV30
INT[1]	AR30
INT[2]	AU31
INT[3]	AV31
INT[4]	AW36
INT[5]	AP32
INT[6]	AU33
INT[7]	AT33
INT[8]	AV34

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 3 of 30)	
Signal Name	**Ball**
INT[9]	AW32
INT[10]	AV33
INT[11]	AR32
INT[12]	AV35
INT[13]	AU34
INT[14]	AT34
INT[15]	AU35
MDC	C5
MDIO	B5
NC	AR29
NC	AR31
NC	AR33
NC	AT30
NC	AT31
NC	AT32
NC	AW35
NC_J35	J35
NC_K34	K34
NC_L6	L6
NC_M33	M33
NC_N6	N6
P1_ACK64#	AW15
P1_AD[0]	AU16
P1_AD[1]	AV14
P1_AD[2]	AP15
P1_AD[3]	AR15
P1_AD[4]	AT15
P1_AD[5]	AW17
P1_AD[6]	AU13
P1_AD[7]	AP14
P1_AD[8]	AT14
P1_AD[9]	AT13
P1_AD[10]	AW16
P1_AD[11]	AP13

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 4 of 30)	
Signal Name	**Ball**
P1_AD[12]	AU11
P1_AD[13]	AU12
P1_AD[14]	AP12
P1_AD[15]	AT12
P1_AD[16]	AW14
P1_AD[17]	AV10
P1_AD[18]	AT10
P1_AD[19]	AU10
P1_AD[20]	AU9
P1_AD[21]	AW6
P1_AD[22]	AW12
P1_AD[23]	AR8
P1_AD[24]	AT8
P1_AD[25]	AU8
P1_AD[26]	AW8
P1_AD[27]	AV5
P1_AD[28]	AU5
P1_AD[29]	AR6
P1_AD[30]	AT7
P1_AD[31]	AW7
P1_AD[32]	AU28
P1_AD[33]	AV27
P1_AD[34]	AU25
P1_AD[35]	AU26
P1_AD[36]	AW30
P1_AD[37]	AW25
P1_AD[38]	AU23
P1_AD[39]	AV28
P1_AD[40]	AU24
P1_AD[41]	AV22
P1_AD[42]	AP23
P1_AD[43]	AR23
P1_AD[44]	AT23
P1_AD[45]	AW24
P1_AD[46]	AU21

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 5 of 30)	
Signal Name	**Ball**
P1_AD[47]	AU22
P1_AD[48]	AP22
P1_AD[49]	AT22
P1_AD[50]	AW23
P1_AD[51]	AV20
P1_AD[52]	AP21
P1_AD[53]	AR21
P1_AD[54]	AT21
P1_AD[55]	AW22
P1_AD[56]	AU20
P1_AD[57]	AP20
P1_AD[58]	AT20
P1_AD[59]	AW21
P1_AD[60]	AV18
P1_AD[61]	AR19
P1_AD[62]	AT19
P1_AD[63]	AU17
P1_CBE#[0]	AU14
P1_CBE#[1]	AV7
P1_CBE#[2]	AW13
P1_CBE#[3]	AW11
P1_CBE#[4]	AU19
P1_CBE#[5]	AP19
P1_CBE#[6]	AW19
P1_CBE#[7]	AT18
P1_CLK_IN	AR7
P1_CLK_OUT	AP8
P1_DEVSEL#	AR9
P1_ENUM#	AP16
P1_ES	AU27
P1_FRAME#	AR11
P1_GNT#[1]	AT6
P1_GNT#[2]	AV16
P1_GNT#[3]	AU18
P1_GNT#[4]	AR17

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 6 of 30)	
Signal Name	**Ball**
P1_GNT#[5]	AU15
P1_GNT#[6]	AT25
P1_GNT#[7]	AT24
P1_HEALTHY#	AU6
P1_HS_64EN#	AT27
P1_IDSEL	AU4
P1_INTA#	AW4
P1_INTB#	AW5
P1_INTC#	AU7
P1_INTD#	AV4
P1_IRDY#	AT9
P1_LED#	AT26
P1_M66EN	AV12
P1_PAR	AT11
P1_PAR64	AP18
P1_PCIXCAP[0]	AV26
P1_PCIXCAP[1]	AW27
P1_PERR#	AW10
P1_PLL_AVCC	AP9
P1_PLL_AVSS	AP7
P1_PME#	AW9
P1_REQ#[1]	AW3
P1_REQ#[2]	AT16
P1_REQ#[3]	AW18
P1_REQ#[4]	AP17
P1_REQ#[5]	AT17
P1_REQ#[6]	AV24
P1_REQ#[7]	AP24
P1_REQ64#	AW20
P1_RST#	AT5
P1_RSTDIR	AR13
P1_SERR#	AV8
P1_STOP#	AP11
P1_TRDY#	AP10
P2_ACK64#	AB1

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 7 of 30)	
Signal Name	**Ball**
P2_AD[0]	AE3
P2_AD[1]	AE2
P2_AD[2]	AE6
P2_AD[3]	AC4
P2_AD[4]	AD4
P2_AD[5]	AD1
P2_AD[6]	AD3
P2_AD[7]	AD6
P2_AD[8]	AC5
P2_AD[9]	AB4
P2_AD[10]	AC1
P2_AD[11]	AC6
P2_AD[12]	AB2
P2_AD[13]	AB3
P2_AD[14]	AB6
P2_AD[15]	Y5
P2_AD[16]	AA1
P2_AD[17]	AA2
P2_AD[18]	W4
P2_AD[19]	Y3
P2_AD[20]	W3
P2_AD[21]	U1
P2_AD[22]	W1
P2_AD[23]	V5
P2_AD[24]	T4
P2_AD[25]	V3
P2_AD[26]	R1
P2_AD[27]	T2
P2_AD[28]	T3
P2_AD[29]	V4
P2_AD[30]	R4
P2_AD[31]	P1
P2_AD[32]	AP4
P2_AD[33]	AP5
P2_AD[34]	AP1

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 8 of 30)	
Signal Name	**Ball**
P2_AD[35]	AN3
P2_AD[36]	AP6
P2_AD[37]	AN1
P2_AD[38]	AP3
P2_AD[39]	AM5
P2_AD[40]	AM4
P2_AD[41]	AN2
P2_AD[42]	AN6
P2_AD[43]	AL4
P2_AD[44]	AL3
P2_AD[45]	AM1
P2_AD[46]	AL1
P2_AD[47]	AM3
P2_AD[48]	AM6
P2_AD[49]	AK5
P2_AD[50]	AK1
P2_AD[51]	AL2
P2_AD[52]	AL6
P2_AD[53]	AJ4
P2_AD[54]	AK4
P2_AD[55]	AJ1
P2_AD[56]	AJ3
P2_AD[57]	AK6
P2_AD[58]	AH5
P2_AD[59]	AH1
P2_AD[60]	AJ2
P2_AD[61]	AG4
P2_AD[62]	AH4
P2_AD[63]	AH3
P2_CBE#[0]	AC3
P2_CBE#[1]	V2
P2_CBE#[2]	Y1
P2_CBE#[3]	V1
P2_CBE#[4]	AG1
P2_CBE#[5]	AJ6

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 9 of 30)	
Signal Name	**Ball**
P2_CBE#[6]	AE1
P2_CBE#[7]	AD5
P2_CLK_IN	T5
P2_CLK_OUT	U6
P2_DEVSEL#	W6
P2_ENUM#	AF6
P2_ES	AU1
P2_FRAME#	Y4
P2_GNT#[1]	M1
P2_GNT#[2]	AF3
P2_GNT#[3]	AG3
P2_GNT#[4]	AF5
P2_GNT#[5]	AG2
P2_GNT#[6]	AR1
P2_GNT#[7]	AR4
P2_HEALTHY#	R2
P2_HS_64EN#	AT1
P2_IDSEL	R3
P2_INTA#	P3
P2_INTB#	N1
P2_INTC#	U3
P2_INTD#	L1
P2_IRDY#	U4
P2_LED#	AN4
P2_M66EN	AD2
P2_PAR	AA4
P2_PAR64	AH6
P2_PCIXCAP[0]	AT3
P2_PCIXCAP[1]	AT2
P2_PERR#	AA3
P2_PLL_AVCC	V6
P2_PLL_AVSS	T6
P2_PME#	T1
P2_REQ#[1]	M2
P2_REQ#[2]	AG6

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 10 of 30)	
Signal Name	**Ball**
P2_REQ#[3]	AE4
P2_REQ#[4]	AF1
P2_REQ#[5]	AF4
P2_REQ#[6]	AR3
P2_REQ#[7]	AR2
P2_REQ64#	AK3
P2_RST#	P2
P2_RSTDIR	AA5
P2_SERR#	W2
P2_STOP#	AA6
P2_TRDY#	Y6
PBI_AD[0]	K36
PBI_AD[1]	P35
PBI_AD[2]	L34
PBI_AD[3]	M35
PBI_AD[4]	D33
PBI_AD[5]	H37
PBI_AD[6]	N34
PBI_AD[7]	P34
PBI_AD[8]	J37
PBI_AD[9]	H35
PBI_AD[10]	H36
PBI_AD[11]	H39
PBI_AD[12]	H38
PBI_AD[13]	G39
PBI_AD[14]	G36
PBI_AD[15]	F36
PBI_AD[16]	G38
PBI_AD[17]	F39
PBI_AD[18]	E37
PBI_AD[19]	D39
PBI_AD[20]	E38
PBI_AD[21]	E34
PBI_AD[22]	E36
PBI_AD[23]	D37

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 11 of 30)	
Signal Name	**Ball**
PBI_AD[24]	C39
PBI_AD[25]	D38
PBI_AD[26]	E33
PBI_AD[27]	C36
PBI_AD[28]	D35
PBI_AD[29]	B36
PBI_AD[30]	F32
PBI_AD[31]	C35
PBI_CS#[0]	F35
PBI_CS#[1]	F37
PBI_CS#[2]	G35
PBI_CS#[3]	D34
PBI_LE	G32
PBI_OE#	J36
PBI_RDY#	K35
PBI_RW	F38
PWRUP_P1_ARB	AP26
PWRUP_P1_BYP	AV32
PWRUP_P1_PRIM	AR25
PWRUP_P1_SWRST	AR26
PWRUP_P2_ARB	AW34
PWRUP_P2_BYP	AU36
PWRUP_P2_PRIM	AU29
PWRUP_P2_SWRST	AW26
PWRUP_PBI_BSWP	AW29
PWRUP_TRANS	AP27
PWRUP_XS_SWRST	AW28
REF125M	K4
SD_A[0]	A20
SD_A[1]	A22
SD_A[2]	A25
SD_A[3]	B26
SD_A[4]	A26
SD_A[5]	A27
SD_A[6]	B27

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 12 of 30)	
Signal Name	**Ball**
SD_A[7]	B29
SD_A[8]	A28
SD_A[9]	A29
SD_A[10]	B20
SD_A[11]	B30
SD_A[12]	A30
SD_A[13]	B32
SD_BA[0]	A17
SD_BA[1]	A19
SD_CAS#	A13
SD_CKFBI	A34
SD_CKFBO	B35
SD_CLK#[0]	B21
SD_CLK#[1]	B23
SD_CLK#[2]	B24
SD_CLK#[3]	B18
SD_CLK[0]	A21
SD_CLK[1]	A23
SD_CLK[2]	A24
SD_CLK[3]	A18
SD_CLKEN	B9
SD_CS#[0]	A14
SD_CS#[1]	B14
SD_CS#[2]	A15
SD_CS#[3]	B15
SD_CS#[4]	A35
SD_CS#[5]	B33
SD_CS#[6]	A37
SD_CS#[7]	A36
SD_DQ[0]	D31
SD_DQ[1]	A31
SD_DQ[2]	C29
SD_DQ[3]	E28
SD_DQ[4]	C34
SD_DQ[5]	E31

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 13 of 30)	
Signal Name	**Ball**
SD_DQ[6]	C30
SD_DQ[7]	E30
SD_DQ[8]	A33
SD_DQ[9]	D30
SD_DQ[10]	D25
SD_DQ[11]	C24
SD_DQ[12]	F29
SD_DQ[13]	D28
SD_DQ[14]	E26
SD_DQ[15]	E25
SD_DQ[16]	E27
SD_DQ[17]	F26
SD_DQ[18]	C25
SD_DQ[19]	E23
SD_DQ[20]	C28
SD_DQ[21]	C27
SD_DQ[22]	E24
SD_DQ[23]	F23
SD_DQ[24]	D24
SD_DQ[25]	C23
SD_DQ[26]	C21
SD_DQ[27]	D19
SD_DQ[28]	C22
SD_DQ[29]	D22
SD_DQ[30]	F19
SD_DQ[31]	E18
SD_DQ[32]	C17
SD_DQ[33]	D16
SD_DQ[34]	E14
SD_DQ[35]	C12
SD_DQ[36]	F17
SD_DQ[37]	C16
SD_DQ[38]	C13
SD_DQ[39]	D13
SD_DQ[40]	F16

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 14 of 30)	
Signal Name	**Ball**
SD_DQ[41]	F14
SD_DQ[42]	F13
SD_DQ[43]	B12
SD_DQ[44]	E16
SD_DQ[45]	E15
SD_DQ[46]	A12
SD_DQ[47]	E12
SD_DQ[48]	C11
SD_DQ[49]	C10
SD_DQ[50]	D11
SD_DQ[51]	D12
SD_DQ[52]	D8
SD_DQ[53]	C9
SD_DQ[54]	D9
SD_DQ[55]	D10
SD_DQ[56]	B11
SD_DQ[57]	A10
SD_DQ[58]	C8
SD_DQ[59]	E9
SD_DQ[60]	A11
SD_DQ[61]	F12
SD_DQ[62]	B8
SD_DQ[63]	A6
SD_DQS[0]	E29
SD_DQS[1]	F28
SD_DQS[2]	C26
SD_DQS[3]	F20
SD_DQS[4]	C15
SD_DQS[5]	E13
SD_DQS[6]	A7
SD_DQS[7]	A9
SD_DQS[8]	C20
SD_DQS[9]	C31
SD_DQS[10]	D27
SD_DQS[11]	F25

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 15 of 30)	
Signal Name	**Ball**
SD_DQS[12]	D21
SD_DQS[13]	D15
SD_DQS[14]	C14
SD_DQS[15]	C7
SD_DQS[16]	E10
SD_DQS[17]	E19
SD_ECC[0]	F22
SD_ECC[1]	E20
SD_ECC[2]	C19
SD_ECC[3]	C18
SD_ECC[4]	E22
SD_ECC[5]	E21
SD_ECC[6]	D18
SD_ECC[7]	E17
SD_I2C_CLK	C32
SD_I2C_SDA	A32
SD_PLL_AVCC	G30
SD_PLL_AVSS	D32
SD_PWRDELAY	C33
SD_RAS#	B17
SD_VREF	A8
SD_WE#	A16
SF_CLK	AW31
SF_RST#	AP25
SRAM_SKU	AW33
TCK	AT29
TDI	AU30
TDO	AP28
TMS	AT28
TRST#	AR27
U0_CTS#	AR36
U0_DCD#	AM34
U0_DSR#	AN36
U0_DTR#	AM35
U0_RI#	AT38

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 16 of 30)	
Signal Name	**Ball**
U0_RTS#	AR37
U0_RX	AP35
U0_TX	AR35
U1_CTS#	AP37
U1_DCD#	AU39
U1_DSR#	AN34
U1_DTR#	AL34
U1_RI#	AW37
U1_RTS#	AT37
U1_RX	AP36
U1_TX	AV36
VCC_CORE	F7
VCC_CORE	G7
VCC_CORE	G8
VCC_CORE	H8
VCC_CORE	H9
VCC_CORE	H10
VCC_CORE	H30
VCC_CORE	H31
VCC_CORE	H32
VCC_CORE	J7
VCC_CORE	J8
VCC_CORE	J32
VCC_CORE	K7
VCC_CORE	K8
VCC_CORE	K32
VCC_CORE	L7
VCC_CORE	R16
VCC_CORE	R18
VCC_CORE	R20
VCC_CORE	R22
VCC_CORE	R24
VCC_CORE	T15
VCC_CORE	T17
VCC_CORE	T19

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 17 of 30)	
Signal Name	**Ball**
VCC_CORE	T21
VCC_CORE	T23
VCC_CORE	T25
VCC_CORE	U16
VCC_CORE	U18
VCC_CORE	U20
VCC_CORE	U22
VCC_CORE	U24
VCC_CORE	V15
VCC_CORE	V17
VCC_CORE	V23
VCC_CORE	V25
VCC_CORE	W16
VCC_CORE	W24
VCC_CORE	Y15
VCC_CORE	Y17
VCC_CORE	Y23
VCC_CORE	Y25
VCC_CORE	AA16
VCC_CORE	AA24
VCC_CORE	AB15
VCC_CORE	AB17
VCC_CORE	AB23
VCC_CORE	AB25
VCC_CORE	AC16
VCC_CORE	AC18
VCC_CORE	AC20
VCC_CORE	AC22
VCC_CORE	AC24
VCC_CORE	AD15
VCC_CORE	AD17
VCC_CORE	AD19
VCC_CORE	AD21
VCC_CORE	AD23
VCC_CORE	AD25

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 18 of 30)	
Signal Name	**Ball**
VCC_CORE	AE16
VCC_CORE	AE18
VCC_CORE	AE20
VCC_CORE	AE22
VCC_CORE	AE24
VCC_CORE	AK8
VCC_CORE	AK32
VCC_CORE	AL8
VCC_CORE	AL32
VCC_CORE	AM8
VCC_CORE	AM9
VCC_CORE	AM10
VCC_CORE	AM30
VCC_CORE	AM31
VCC_CORE	AM32
VCC_CORE	AN29
VCC_PC	F6
VCC_PC	G6
VCC_PC	H6
VCC_PC	H7
VCC_PC	J6
VCC_PC	K6
VCC_PC	M7
VCC_PC	N7
VCC_PC	P7
VCC_PC	R7
VCC_PC	T7
VCC_PC	U7
VCC_PC	V7
VCC_PC	W7
VCC_PC	Y7
VCC_PC	AA7
VCC_PC	AB7
VCC_PC	AC7
VCC_PC	AD7

Table 21
1025-Lead HSBGA Package — Alphabetical Signal Listing
(Sheet 19 of 30)

Signal Name	Ball
VCC_PC	AE7
VCC_PC	AF7
VCC_PC	AG7
VCC_PC	AH7
VCC_PC	AJ7
VCC_PC	AK7
VCC_PC	AL7
VCC_PC	AM7
VCC_PC	AM33
VCC_PC	AN8
VCC_PC	AN9
VCC_PC	AN10
VCC_PC	AN11
VCC_PC	AN12
VCC_PC	AN13
VCC_PC	AN14
VCC_PC	AN15
VCC_PC	AN16
VCC_PC	AN17
VCC_PC	AN18
VCC_PC	AN19
VCC_PC	AN20
VCC_PC	AN21
VCC_PC	AN22
VCC_PC	AN23
VCC_PC	AN24
VCC_PC	AN25
VCC_PC	AN26
VCC_PC	AN27
VCC_PC	AN28
VCC_PC	AN30
VCC_PC	AN31
VCC_PC	AN32
VCC_PC	AN33
VCC_PC	AP29

Table 21
1025-Lead HSBGA Package — Alphabetical Signal Listing
(Sheet 20 of 30)

Signal Name	Ball
VCC_PC	AP30
VCC_PC	AP31
VCC_SD	F9
VCC_SD	F10
VCC_SD	F11
VCC_SD	F31
VCC_SD	G9
VCC_SD	G10
VCC_SD	G11
VCC_SD	G12
VCC_SD	G13
VCC_SD	G14
VCC_SD	G15
VCC_SD	G16
VCC_SD	G17
VCC_SD	G18
VCC_SD	G19
VCC_SD	G20
VCC_SD	G21
VCC_SD	G22
VCC_SD	G23
VCC_SD	G24
VCC_SD	G25
VCC_SD	G26
VCC_SD	G27
VCC_SD	G28
VCC_SD	G29
VCC_SD	G31
VCC_XS	F33
VCC_XS	F34
VCC_XS	G33
VCC_XS	G34
VCC_XS	H33
VCC_XS	H34
VCC_XS	J33

Table 21
1025-Lead HSBGA Package — Alphabetical Signal Listing
(Sheet 21 of 30)

Signal Name	Ball
VCC_XS	J34
VCC_XS	K33
VCC_XS	N33
VCC_XS	P33
VCC_XS	R33
VCC_XS	T33
VCC_XS	U33
VCC_XS	V33
VCC_XS	W33
VCC_XS	Y33
VCC_XS	AA33
VCC_XS	AB33
VCC_XS	AC33
VCC_XS	AD33
VCC_XS	AE33
VCC_XS	AF33
VCC_XS	AG33
VCC_XS	AH33
VCC_XS	AJ33
VCC_XS	AK33
VCC_XS	AL33
VSS_CORE	R15
VSS_CORE	R17
VSS_CORE	R19
VSS_CORE	R21
VSS_CORE	R23
VSS_CORE	R25
VSS_CORE	T16
VSS_CORE	T18
VSS_CORE	T20
VSS_CORE	T22
VSS_CORE	T24
VSS_CORE	U15
VSS_CORE	U17
VSS_CORE	U19

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 22 of 30)	
Signal Name	**Ball**
VSS_CORE	U21
VSS_CORE	U23
VSS_CORE	U25
VSS_CORE	V16
VSS_CORE	V18
VSS_CORE	V19
VSS_CORE	V20
VSS_CORE	V21
VSS_CORE	V22
VSS_CORE	V24
VSS_CORE	W15
VSS_CORE	W17
VSS_CORE	W18
VSS_CORE	W19
VSS_CORE	W20
VSS_CORE	W21
VSS_CORE	W22
VSS_CORE	W23
VSS_CORE	W25
VSS_CORE	Y16
VSS_CORE	Y18
VSS_CORE	Y19
VSS_CORE	Y20
VSS_CORE	Y21
VSS_CORE	Y22
VSS_CORE	Y24
VSS_CORE	AA15
VSS_CORE	AA17
VSS_CORE	AA18
VSS_CORE	AA19
VSS_CORE	AA20
VSS_CORE	AA21
VSS_CORE	AA22
VSS_CORE	AA23
VSS_CORE	AA25

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 23 of 30)	
Signal Name	**Ball**
VSS_CORE	AB16
VSS_CORE	AB18
VSS_CORE	AB19
VSS_CORE	AB20
VSS_CORE	AB21
VSS_CORE	AB22
VSS_CORE	AB24
VSS_CORE	AC15
VSS_CORE	AC17
VSS_CORE	AC19
VSS_CORE	AC21
VSS_CORE	AC23
VSS_CORE	AC25
VSS_CORE	AD16
VSS_CORE	AD18
VSS_CORE	AD20
VSS_CORE	AD22
VSS_CORE	AD24
VSS_CORE	AE15
VSS_CORE	AE17
VSS_CORE	AE19
VSS_CORE	AE21
VSS_CORE	AE23
VSS_CORE	AE25
VSS_IO	B2
VSS_IO	B3
VSS_IO	B7
VSS_IO	B10
VSS_IO	B13
VSS_IO	B16
VSS_IO	B19
VSS_IO	B22
VSS_IO	B25
VSS_IO	B28
VSS_IO	B31

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 24 of 30)	
Signal Name	**Ball**
VSS_IO	B34
VSS_IO	B37
VSS_IO	B38
VSS_IO	C2
VSS_IO	C3
VSS_IO	C37
VSS_IO	C38
VSS_IO	D4
VSS_IO	D14
VSS_IO	D17
VSS_IO	D20
VSS_IO	D23
VSS_IO	D26
VSS_IO	D29
VSS_IO	D36
VSS_IO	E6
VSS_IO	E8
VSS_IO	E11
VSS_IO	E32
VSS_IO	E35
VSS_IO	E39
VSS_IO	F15
VSS_IO	F18
VSS_IO	F21
VSS_IO	F24
VSS_IO	F27
VSS_IO	F30
VSS_IO	G3
VSS_IO	G37
VSS_IO	J39
VSS_IO	K3
VSS_IO	L35
VSS_IO	M6
VSS_IO	M38
VSS_IO	N2

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 25 of 30)

Signal Name	Ball
VSS_IO	N35
VSS_IO	P38
VSS_IO	R5
VSS_IO	R35
VSS_IO	T38
VSS_IO	U2
VSS_IO	U5
VSS_IO	U35
VSS_IO	V38
VSS_IO	W5
VSS_IO	W35
VSS_IO	Y2
VSS_IO	Y38
VSS_IO	AA35
VSS_IO	AB5
VSS_IO	AB38
VSS_IO	AC2
VSS_IO	AC35
VSS_IO	AD38
VSS_IO	AE5
VSS_IO	AE35
VSS_IO	AF2
VSS_IO	AF38
VSS_IO	AG5
VSS_IO	AG35
VSS_IO	AH2
VSS_IO	AH38
VSS_IO	AJ5
VSS_IO	AJ35
VSS_IO	AK2
VSS_IO	AK38
VSS_IO	AL5
VSS_IO	AL35
VSS_IO	AM2
VSS_IO	AM38

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 26 of 30)

Signal Name	Ball
VSS_IO	AN5
VSS_IO	AN7
VSS_IO	AN35
VSS_IO	AP2
VSS_IO	AP33
VSS_IO	AP34
VSS_IO	AR5
VSS_IO	AR10
VSS_IO	AR12
VSS_IO	AR14
VSS_IO	AR16
VSS_IO	AR18
VSS_IO	AR20
VSS_IO	AR22
VSS_IO	AR24
VSS_IO	AR28
VSS_IO	AT4
VSS_IO	AT36
VSS_IO	AU2
VSS_IO	AU3
VSS_IO	AU32
VSS_IO	AU37
VSS_IO	AU38
VSS_IO	AV2
VSS_IO	AV3
VSS_IO	AV6
VSS_IO	AV9
VSS_IO	AV11
VSS_IO	AV13
VSS_IO	AV15
VSS_IO	AV17
VSS_IO	AV19
VSS_IO	AV21
VSS_IO	AV23
VSS_IO	AV25

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 27 of 30)

Signal Name	Ball
VSS_IO	AV29
VSS_IO	AV37
VSS_IO	AV38
XS_A[0]	AH34
XS_A[1]	AG38
XS_A[2]	AG39
XS_A[3]	AG37
XS_A[4]	AF36
XS_A[5]	AJ34
XS_A[6]	AH37
XS_A[7]	AH39
XS_A[8]	AF37
XS_A[9]	AK34
XS_A[10]	AJ36
XS_A[11]	AH35
XS_A[12]	AG36
XS_A[13]	AF35
XS_A[14]	AH36
XS_A[15]	AJ39
XS_ABORT	AF34
XS_BE[0]	AC36
XS_BE[1]	AD34
XS_BE[2]	AC37
XS_BE[3]	AC39
XS_BE[4]	AD39
XS_BE[5]	AC38
XS_BE[6]	AE34
XS_BE[7]	AE36
XS_CLK	K38
XS_CWF	AE37
XS_DQ[0]	Y35
XS_DQ[1]	Y37
XS_DQ[2]	Y36
XS_DQ[3]	W38
XS_DQ[4]	Y39

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 28 of 30)

Signal Name	Ball
XS_DQ[5]	AA34
XS_DQ[6]	Y34
XS_DQ[7]	W37
XS_DQ[8]	V34
XS_DQ[9]	U37
XS_DQ[10]	T35
XS_DQ[11]	U36
XS_DQ[12]	U39
XS_DQ[13]	U34
XS_DQ[14]	T37
XS_DQ[15]	T39
XS_DQ[16]	N38
XS_DQ[17]	P36
XS_DQ[18]	N37
XS_DQ[19]	N36
XS_DQ[20]	L38
XS_DQ[21]	P37
XS_DQ[22]	N39
XS_DQ[23]	M39
XS_DQ[24]	AN38
XS_DQ[25]	AN37
XS_DQ[26]	AN39
XS_DQ[27]	AL38
XS_DQ[28]	AM39
XS_DQ[29]	AL39
XS_DQ[30]	AL37
XS_DQ[31]	AM37
XS_DQ[32]	W39
XS_DQ[33]	V37
XS_DQ[34]	V36
XS_DQ[35]	W36
XS_DQ[36]	V39
XS_DQ[37]	W34
XS_DQ[38]	V35
XS_DQ[39]	U38

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 29 of 30)

Signal Name	Ball
XS_DQ[40]	R38
XS_DQ[41]	T34
XS_DQ[42]	T36
XS_DQ[43]	R36
XS_DQ[44]	R39
XS_DQ[45]	R34
XS_DQ[46]	R37
XS_DQ[47]	P39
XS_DQ[48]	J38
XS_DQ[49]	K37
XS_DQ[50]	L36
XS_DQ[51]	K39
XS_DQ[52]	L37
XS_DQ[53]	L39
XS_DQ[54]	M37
XS_DQ[55]	M36
XS_DQ[56]	AJ37
XS_DQ[57]	AK36
XS_DQ[58]	AL36
XS_DQ[59]	AJ38
XS_DQ[60]	AK35
XS_DQ[61]	AK37
XS_DQ[62]	AK39
XS_DQ[63]	AM36
XS_DVALID[0]	AA36
XS_DVALID[1]	AB34
XS_ECC[0]	AA38
XS_ECC[1]	AA39
XS_ECC[2]	AA37
XS_ECC[3]	AB35
XS_ECC[4]	AC34
XS_ECC[5]	AB36
XS_ECC[6]	AB39
XS_ECC[7]	AB37
XS_FIQ[0]	AR39

Table 21 1025-Lead HSBGA Package — Alphabetical Signal Listing (Sheet 30 of 30)

Signal Name	Ball
XS_FIQ[1]	AR38
XS_HLDA[0]	AG34
XS_HLDA[1]	AE38
XS_HOLD[0]	AE39
XS_HOLD[1]	AF39
XS_IRQ[0]	AP39
XS_IRQ[1]	AP38
XS_LEN[0]	AD36
XS_LEN[1]	AD37
XS_LEN[2]	AD35
XS_PLL_AVCC	L33
XS_PLL_AVSS	M34
XS_RESET#	AT39

3.2 Package Thermal Specifications

The device is specified for operation when T_C (case temperature) is within the range of 0 °C to 85 °C, depending on operating conditions. Case temperature may be measured in any environment to determine whether the processor is within specified operating range. Case temperature is best measured at the center of the top surface, opposite the ball pad.

3.2.1 Thermal Characteristics

Table 22 summarizes the thermal simulation data for the GW80314.

The thermal performance of the GW80314 package is represented by the following parameters:

1. ψ_{JT}, thermal characterization parameter from junction-to-top center
   $\psi_{JT} = (T_J - T_T) / P$
   where
   T_T is the temperature of the top-center of the package
   ψ_{JT} is used to estimate junction temperature by measuring T_T in an actual environment
   ψ_{JT} simulations are carried out to show the thermal performance of the GW80314.

Table 22. Thermal Simulation Data for the Intel® GW80314 I/O Processor

Package Conditions	
Package Type	**HSBGA**
Ball Count	1025
Package Size (mm)	40x40
Mold Thickness (mm)	1.17
Pitch (mm)	1
Ball Matrix (mm)	39x39
Ball Row Depth	7x7
Thermal Ball Matrix	11x11
Vias	144
Pad Size (mm)	12.5x12.5
Die Size (mm)	11.62x11.62
Substrate Layer	4
Substrate Thickness (mm)	0.56
PCB Conditions (JEDEC JESD51-9)	
PCB Layer	4
PCB Dimensions (mm)	127.0x139.5
PCB Thickness (mm)	1.6
Environment Conditions	
Maximum Junction Temperature (C)	125
Power Dissipation (W)	2.456 Typical 4.226 Max
Thermal Data	
Property V_{AIR} (m/s)	**Psi jt (C/W)**
0.00	1.8
1.00	1.8
2.00	1.8
Heat Flow Path	
Heat Dissipated from PCB (%)	66.1
(%)	15.9
Heat Dissipated from Others (%)	18.0

3.2.2 Case Temperature

When measuring case temperature, T_C, attention to detail is required to ensure accuracy. When a thermocouple is used, calibrate is before taking measurements. Errors may result when the measured surface temperature is affected by the surrounding ambient air temperature. Such errors may be due to a poor thermal contact between thermocouple junction and the surface, heat loss by radiation, or conduction through thermocouple leads.

To minimize measurement errors:

- Use a 35 gauge K-type thermocouple or equivalent.
- Attach the thermocouple bead or junction to the package top surface at a location corresponding to the center of the die. The center of the die gives a more accurate measurement and less variation as the boundary condition changes.
- Attach the thermocouple bead at a 0^o angle with respect to the package when no heat sink is attached.

3.3 Socket Information

Table 23 and Table 24 provide vendor details for socket-headers and burn-in sockets for the GW80314. This is neither an endorsement nor a warranty of the performance of any of the listed products and/or companies.

3.3.1 Socket-Header Vendor

Table 23. Socket-Header Vendor

Company	Factory Representative	Phone/Fax #	BGA 544-Pin Socket Carrier
Advanced Interconnections	TBD	TBD	Socket: FHSB1025-716GG Carrier: FHAX1025-715G
Ironwood	TBD	TBD	SG-BGA-6035

3.3.2 Burn-in Socket Vendor

Table 24. Burn-in Socket Vendor

Company	Factory Representative	Phone #	Burn-in Socket Part #
TBD	TBD	TBD	TBD

3.3.3 Shipping Tray Vendor

Table 25. Shipping Tray Vendor

Company	Factory Representative	Phone #	Shipping Tray Part #
PEAK 2136A Rutland Drive Austin, Texas 78758	TBD	512-339-4684	NXBG40402.503076REV.E

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

Table 26. Maximum Temperature and Voltage Ratings

Parameter	Maximum Rating
Storage Temperature T_{STG}	–40°C to +125°C
Case Temperature Under Bias T_C	0°C to + 85°C
Supply Voltage $\mathbf{V_{CC33}}$ with regard to $\mathbf{V_{SS}}$	–0.5 V to +4.1 V (3.3 VDC)
Supply Voltage $\mathbf{V_{CC25}}$ with regard to $\mathbf{V_{SS}}$	–0.5 V to +3.6 V (2.5 VDC)
Supply Voltage $\mathbf{V_{CC12}}$ with regard to $\mathbf{V_{SS}}$	–0.5 V to +2.0 V (1.2 VDC)

WARNING: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reli*ability.

Table 27. Operating Conditions

Symbol	Parameter	Min.	Max.	Units	Notes
Pvcc33	3.3 V Supply Power	756	1710	mW	
Pvcc25	2.5 V Supply Power	270	609	mW	
Pvcc12	1.2 V Supply Power	1430	1907	mW	
$\mathbf{V_{CC33}}$	3.3 V Supply Power	3.0	3.6	V	
$\mathbf{V_{CC25}}$	2.5 V Supply Power	2.3	2.7	V	
$\mathbf{V_{CC12}}$	1.2 V Supply Power	1.08	1.32	V	
V_{PLL}	PLL Analog Supply Voltage	3.0	3.6	V	
I_{PLL}	PLL Analog Supply Current	–	10	mA	

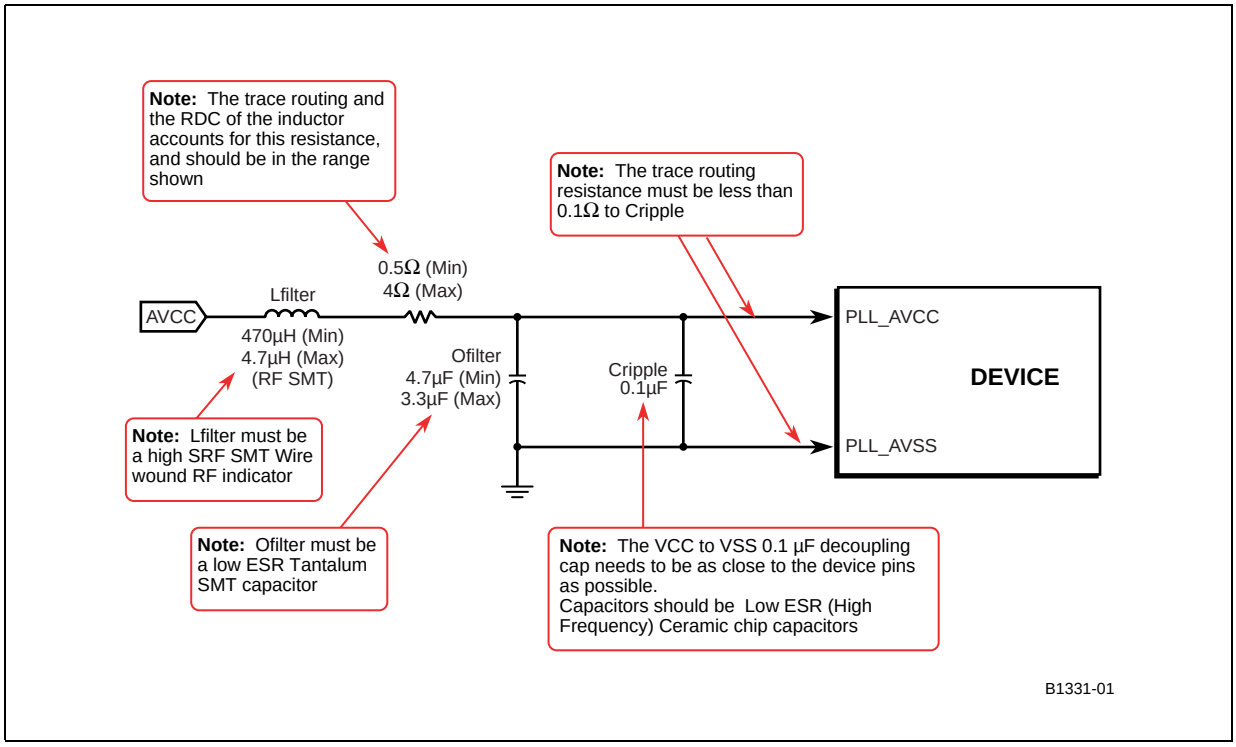
WARNING: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reli*ability.

4.2 PLL Supply Pin Requirements

Package balls of the supply pins for the four Phase Lock Loops (PLLs) used on the GW80314 should be isolated and decoupled externally in order to provide the cleanest possible supply environment. The following pins are used as PLL supplies in the GW80314: XS_PLL_AVCC, SD_PLL_AVCC, P1_PLL_AVCC, and P2_PLL_AVCC. The recommended decoupling network for these pins is shown in Figure 5.

In order to minimize the transient IR drops across the leads from the isolation network and the PLL supply device pins, the trace routes must be kept short. It is preferred that the Cripple capacitor used in Figure 5 be placed as close to the device pins as possible, on the backside of the board underneath the device, when possible.

Figure 5. Intel® GW80314 I/O Processor PLL Supply Decoupling Network



4.3 Targeted DC Specifications

Table 28. DC Characteristics

Symbol	Parameter	Minimum	Maximum	Units	Notes
V_{IL1}	SDRAM Input Low Voltage	-0.3	V_{REF} - 0.12	V	-
V_{IH1}	SDRAM Input High Voltage	V_{REF} + 0.12	V_{CC25} + 0.3	V	-
V_{IL2}	Misc. Input Low Voltage	-0.3	0.8	V	1
V_{IH2}	Misc. Input High Voltage	2.0	V_{CC33} + 0.5	V	1
V_{IL3}	GigE Input Low Voltage	-0.3	0.8	V	
V_{IH3}	GigE Input High Voltage	2.0	V_{CC33} + 0.5	V	4
V_{IL4}	PCI-X Input Low Voltage	-0.5	0.35*V_{CC33}	V	2
V_{IH4}	PCI-X/PCI Input High Voltage	0.5*V_{CC33}	V_{CC33} + 0.5	V	2
V_{IL5}	PCI Input Low Voltage	-0.5	0.3*V_{CC33}	V	2
V_{OL1}	Misc. Output Low Voltage	-	0.4	V	I_{OL} = 6mA, 1, 5
V_{OH1}	Misc. Output High Voltage	$V_{CC33min}$ - 0.5	-	V	I_{OL} = -6mA, 1, 5
V_{OL2}	SDRAM Output Low Voltage	-	0.54	V	I_{OL} = 7.6mA
V_{OH2}	SDRAM Output High Voltage	V_{CC25} - 0.54	-	V	I_{OL} = -7.6mA
V_{OL3}	Intel XScale® Output Low Voltage	-	0.4	V	I_{OL} = 8mA, 5
V_{OH3}	Intel XScale® Output High Voltage	$V_{CC33min}$ - 0.5	-		I_{OL} = -8mA, 4, 5
V_{OL4}	PCI-X Output Low Voltage	-	0.1*V_{CC33}	V	I_{OL} = 1500µA, 2
V_{OH4}	PCI-X Output High Voltage	0.9*V_{CC33}	-	V	I_{OL} = -500µA, 2
V_{OL5}	GigE Output Low Voltage	-	0.4	V	I_{OL} = 12mA, 5
V_{OH5}	GigE Output High Voltage	$V_{CC33min}$ - 0.5	-	V	I_{OL} = -12mA,4, 5
C_{IN}	Input Pin Capacitance	-	8	pF	2, 3
C_{CLK}	Clock Pin Capacitance	5	8	pF	2, 3
L_{PIN}	Ball Inductance	-	22	nH	2, 3

NOTES:
1. Miscellaneous signals include all signals that are not PCI, GigE, Intel XScale®, or SDRAM signals.
2. As required by the *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a.*
3. Not tested.
4. I/O Power Supply
5. V_{CC12}min. = 1.08 V, $V_{CC33min}$ = 3.0 V.

4.4 Targeted AC Specifications

The following section details the AC specifications for GW80314 signal interfaces.

4.4.1 PCI/X Clock Signal Timings

Table 29. PCI/X Clock Timings

Symbol	Parameter	PCI-X		PCI		Units	Notes
		Min.	Max.	Min.	Max.		
T_{F1}	PCI clock Frequency	50	133	25	66	MHz	1,2
T_{C1}	PCI clock Cycle Time	7.5	20	15	40	ns	1,3
T_{CH1}	PCI clock High Time	3	-	6	-	ns	
T_{CL1}	PCI clock Low Time	3	-	6	-	ns	
T_{SR1}	PCI clock Slew Rate	1	6	1	6	V/ns	4
Spread Spectrum Requirements							
f_{MOD}	PCI clock modulation frequency	30	33	30	33	kHz	
f_{spread}	PCI clock frequency spread	-1	0	-1	0	%	

NOTES:
1. The clock frequency may not change beyond the spread-spectrum limits except while SFN_RST# is asserted.
2. The PCI output clock is limited to SFN_CLK, SFN_CLK/2, SFN_CLK/4.
3. The minimum clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.
4. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform.

Table 30. DDR SDRAM Clock Timings

Symbol	Parameter	PC 266		Units
		Min.	Max.	
T_{F2}	DDR SDRAM clock Frequency	66	100	MHz
T_{C2}	DDR SDRAM clock Cycle Time	10	-	ns
T_{CH2}	DDR SDRAM clock High Time	4.5	5.5	ns
T_{CL2}	DDR SDRAM clock Low Time	4.5	5.5	ns
T_{CS2}	DDR SDRAM clock Period Stability	-	+/-90	ps
T_{skew2}	DDR SDRAM clock skew for SD_CLK[2:0] and SD_CLK#[3:0]	-	240	ps

Table 31. Intel XScale® Microprocessor Clock Timings

Symbol	Parameter	XS 100		XS 75		Units
		Min.	Max.	Min.	Max.	
T_{F3}	Intel XScale® microprocessor clock Frequency	-	100	-	75	MHz
T_{C3}	Intel XScale® microprocessor clock Cycle Time	10	-	13	-	ns
T_{CH3}	Intel XScale® microprocessor clock High Time	3	-	5	-	ns
T_{CL3}	Intel XScale® microprocessor clock Low Time	3	-	5	-	ns
T_{CS3}	Intel XScale® microprocessor clock Period Stability	-	+/-175	-	+/-175	ps

4.4.2 Dual-Gigabit Ethernet (GigE) Interface Signal Timings

Table 32. AC Specifications for MII Management Interface

Symbol	Parameter	Condition	Min.	Max.	Units
T_{PERMDC}	Period of MDC MII Management CLock Output	-	60		ns
T_{PWMDC}	Pulse width of MDC Output	-	16		ns
T_{PDMDIO}	Propagation delay of MDIO output from rising edge of MDC	-		7.5	ns
T_{SUMDIO}	Input Setup Time of MDIO to rising edge of MDC	-	4		ns
T_{HMDIO}	Input Hold Time of MDIO after rising edge of MDC	-	3		ns

NOTE: MDC MII Management Interface Clock period is equal to one of the following: SFN_CLK/8, SFN_CLK/16, SFN_CLK/28, SFN_CLK/40, SFN_CLK/56.

Table 33 lists the AC specifications for the G/MII interface of the dual GigE Controller. For propagation delays, the AC loads are assumed to be transmission lines, so numbers quoted in the specifications assume driving a 50 Ohm load connected to a voltage source = $V_{CCIO}/2$.

Table 33. AC Specifications for G/MII and TBI Interface

Symbol	Parameter	Condition	Min.	Max.	Units
T_{CTXCLK}	Period of E[x]_TXCLK inputs	10Mb/s mode	399.98	400.02	ns
		100Mb/s mode	39.998	40.002	ns
$T_{CGTXCLK}$	Period of GTX_CLK input	1000Mb/s mode	7.9992	8.0008	ns
$T_{PWTXCLK}$	Pulse width of E[x]_TXCLK inputs	10Mb/s mode	180	220	ns
		100Mb/s mode	18	22	ns
$T_{PWGTXCLK}$	Pulse width of GTX_CLK input	1000Mb/s mode	3.2	4.8	ns
T_{CRXCLK}	Period of E[x]_RXCLK inputs	10Mb/s mode	399.98	400.02	ns
		100Mb/s mode	39.998	40.002	ns
		1000Mb/s mode	7.9992	8.0008	ns
$T_{CPMARCLK}$	Period of PMA_CLK[x] input	1000Mb/s mode	15.9984	16.0016	ns
$T_{PWRXCLK}$	Pulse width of E[x]_RXCLK input	10Mb/s mode	180	220	ns
		100Mb/s mode	18	22	ns
		1000Mb/s mode	3.2	4.8	ns
$T_{PWPMARCLK}$	Pulse width of PMA_CLK[x] input	1000Mb/s mode	6.4	9.6	ns
T_{SKPMA}	Skew between PMA_CLK[x] inputs	1000Mb/s mode	7.5	8.5	ns
T_{PDTX}	Propagation delay of E[x]_TCG after rising edge of E[x]_TXCLK	10Mb/s or 100Mb/s mode	-	12	ns
T_{PDGTX}	Propagation delay of E[x]_TXG after rising edge of GTX_CLK	1000Mb/s mode	-	5	ns
T_{SURX}	Setup time for E[x]_RCG to rising edge of E[x]_RXCLK	10,100,1000Mb/s modes	2		ns
T_{HRX}	Hold time for E[x]_RCG to rising edge of E[x]_RXCLK	G/MII modes	0		ns

NOTES:
1. All parameters are valid for both ports of GigE interface (i.e., E[x] = E0 or E1).

4.4.3 PCI/X Interface Signal Timings

Table 34. AC Specifications for PCI/X Interface

Symbol	Parameter	PCI-X 133		PCI-X 66		PCI 66		PCI 33		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
T_{OV1}	Clock to Output Valid Delay for bused signals	0.7	3.8	0.7	3.8	1	6	2	11	ns	1,2,3
T_{OV2}	Clock to Output Valid Delay for point to point signals	0.7	3.8	0.7	3.8	2	6	2	12	ns	1,2,3
T_{OF}	Clock to Output Float Delay	-	7	-	7	-	14	-	28	ns	1,7
T_{IS1}	Input Setup to clock for bused signals	1.2	-	1.7	-	3	-	7	-	ns	3,4,8
T_{IS2}	Input Setup to clock for point to point signals	1.2	-	1.7	-	5	-	10,12	-	ns	3,4
T_{IH1}	Input Hold time from clock	0.5	-	0.5	-	0	-	0	-	ns	4
T_{RST}	Reset Active Time	1	-	1	-	1	-	1	-	ms	
T_{RF}	Reset Active to output float delay	-	40	-	40	-	40	-	40	ns	5,6
T_{IS3}	P[x]_REQ64# to Reset setup time	10	-	10	-	10	-	10	-	clocks	
T_{IH2}	Reset to P[x]_REQ64# hold time	-0.6	50	-0.6	50	-0.6	50	-0.6	50	ns	
T_{IS4}	PCI-X initialization pattern to Reset setup time	10	-	10	-	-	-	-	-	clocks	
T_{IH3}	Reset to PCI-X initialization pattern hold time	-0.6	50	-0.6	50	-	-	-	-	ns	
T_{SRST}	Assertion of reset slew rate for battery backup entry		20		20		20		20	ns/V	9

NOTES:
1. See the timing measurement conditions in Figure 10.
2. See Figure 15, Figure 16 and Figure 17.
3. Setup time for point-to-point signals applies to P[x]_REQ# and P[x]_GNT# only. All other signals are bused.
4. See the timing measurement conditions in Figure 9.
5. SFN_RST# is asserted and deasserted asynchronously with respect to SFN_CLK.
6. All output drivers must be floated when SFN_RST# is active.
7. For purposes of Active/Float timing measurements, the HI-Z or “off” state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
9. Relevant reset input pin depends on power-on configuration and may be P1_RST#, P2_RST#, or SFN_RST#. This specification does not apply to systems that do not implement battery backup. Per PCI/X specifications reset slew rate is only specified for the de-assertion edge at 20ns/V.

4.4.4 DDR SDRAM Interface Signal Timings

Table 35. AC Specifications for DDR SDRAM Interface

Symbol	Parameter	Min.	Max.	Units	Notes
T_{VB1}	SD_DQS output valid time before SD_CLK	-	0.9	ns	1
T_{VA1}	SD_DQS output valid time after SD_CLK	-	0.9	ns	1
T_{VB2}	Address and Control write output valid before SD_CLK	3.9	-	ns	1
T_{VA2}	Address and Control write output valid after SD_CLK	4.3	-	ns	1
T_{VB3}	SD_DQS read input valid time before SD_ DQ	-	0.9	ns	2
T_{VA3}	SD_DQS read input valid time after SD_DQ	-	0.9	ns	2
T_{VB4}	SD_DQS write input valid time before SD_ DQ	1.7	-	ns	1
T_{VA4}	SD_DQS write input valid time after SD_DQ	1.7	-	ns	1

NOTES:
1. See Figure 12.
2. See Figure 13.

4.4.5 Intel XScale® Microprocessor Interface Signal Timings

Table 36. AC Specifications for Intel XScale® Microprocessor Interface

Symbol	Parameter	Min.	Max.	Units	Notes
T_{OV1}	Output Valid Delay from XS_CLK - XS_DQ[63:0] and XS_BE[7:0]	3.2	8.5	ns	1,3
T_{OV2}	Output Valid Delay from XS_CLK - XS_DVALID and XS_ABORT	3.2	8.5	ns	1,3
T_{IS1}	Input Setup to XS_CLK - XS_DQ[63:0] and XS_BE[7:0]	0.5	-	ns	2
T_{IH1}	Input Hold from XS_CLK - XS_DQ[63:0],XS_BE[7:0]	2.2	-	ns	2
T_{IS2}	Input Setup to XS_CLK - XS_A[15:0], XS_LEN[2:0]	0.5	-	ns	2
T_{IH2}	Input Hold from XS_CLK - XS_A[15:0],XS_LEN[2:0]	2.2	-	ns	2

NOTES:
1. See Figure 10.
2. See Figure 9.
3. These output valid times are specified with 30 pF loading.

4.4.6 UART Interface Signal Timings

Table 37. AC Specifications for UART Interface

Symbol	Parameter	Minimum	Max.	Units	Notes
T_{HDSR}	U[x]_DSR# Hold Time	0	-	ns	
T_{SDSR}	U[x]_DSR# Setup Time	60	-	ns	
T_{DRDSR}	U[x]_RTS# - U[x]_DSR# Delay Time	30	-	ns	
T_{DWDSR}	U[x]_CTS# - U[x]_DSR# Delay Time	30	-	ns	
T_{HRX}	U[x]_RX Hold Time	30	-	ns	
T_{SRX}	U[x]_RX Setup Time	30	-	ns	
T_{DTX}	U[x]_TX Transmit Cycle Delay Time	125	-	ns	
T_{HRTS}	U[x]_DSR# - U[x]_RTS# Hold Time	20	-	ns	
T_{DRTS}	U[x]_RTS# - U[x]_TX Data Delay Time	-	60	ns	1
T_{DFRTS}	U[x]_RTS# - U[x]_TX Floating Data Delay Time	-	100	ns	1
T_{DRX}	U[x]_RX Receive Cycle Delay Time	150	-	ns	
T_{HCTS}	U[x]_DSR# - U[x]_CTS# Hold Time	20	-	ns	

NOTES:
1. Output has external load of 100pF. Charge and discharge times determined by V_{OL}, V_{OH}, and external load.

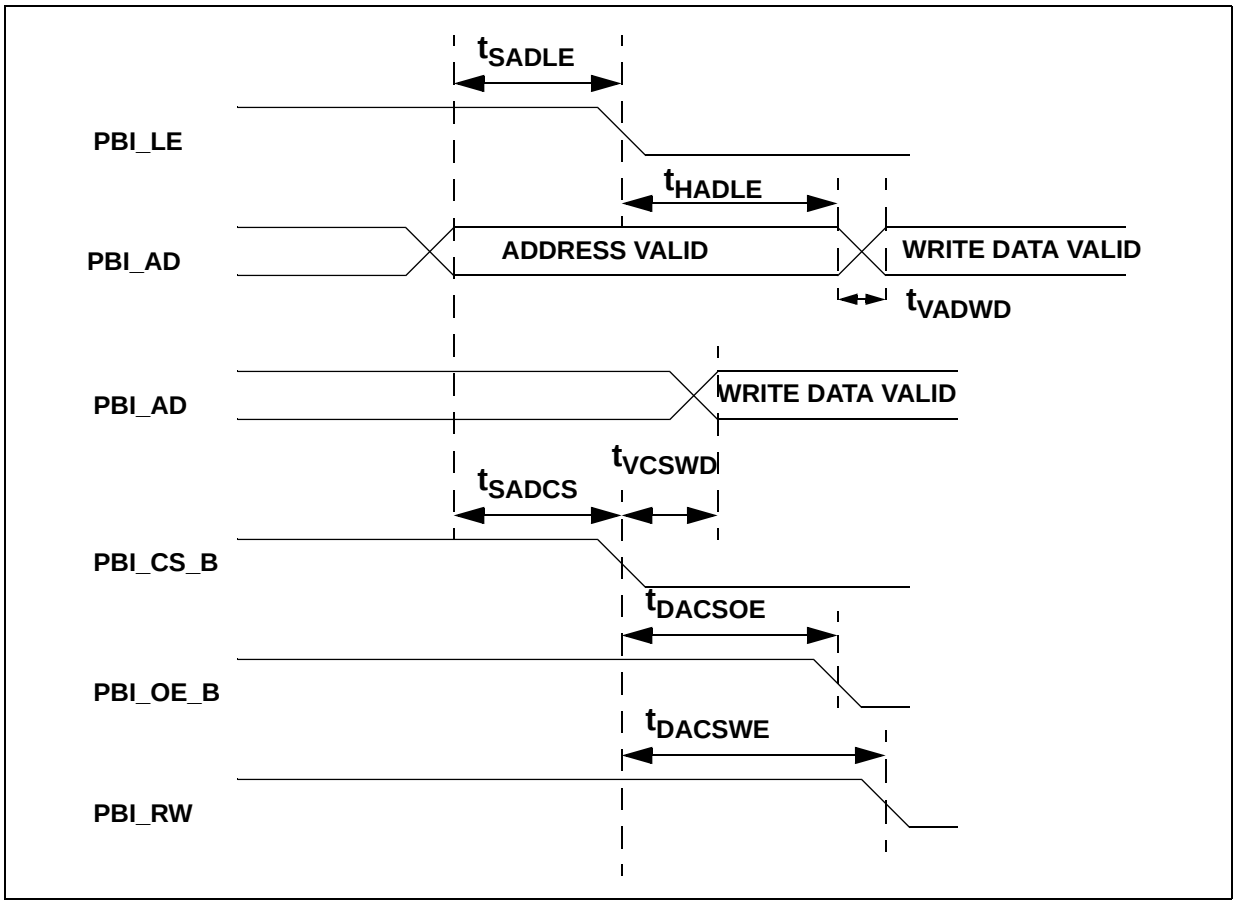
4.4.7 Peripheral Bus Interface (PBI) Signal Timings

Table 38. PBI Interface Timing

Parameter	Timing Relationship	Min.	Max.	Units	Notes
t_{SADLE}	Setup time from address valid to PBI_LE assertion	-6.0 + w		ns	1
t_{HADLE}	Hold time from PBI_LE assertion to address release	7.5 + w			1, 2
t_{SADCS}	Setup time from address valid to PBI_CS_B assertion	-7.5 + w		ns	1
t_{DACSOE}	Delay time from PBI_CS_B assertion to PBI_OE_B assertion	-1.0 + w	2.5 + w	ns	1
t_{DACSWE}	Delay time from PBI_CS_B assertion to PBI_RW assertion	0.0 + w	2.0 + w	ns	1
t_{HWDCS}	Hold time from PBI_CS_B deassertion to data release for write data	0.5		ns	
t_{DDCSWE}	Delay time from PBI_CS_B deassertion to PBI_RW deassertion in handshaking mode	-2.0 + w	0.0 + w	ns	1
t_{DHWECS}	Delay time from PBI_RW deassertion to PBI_CS_B deassertion in non-handshaking mode	0.0 + w	2.0 + w	ns	1
t_{DDCSOE}	Delay time from PBI_CS_B deassertion to PBI_OE_B deassertion	-1.0	2.5	ns	
t_{VADRD}	Delay time from address valid to Read Data valid in latch mode		2.1 + w	ns	1, 3
t_{WVRD}	Data valid window	3.7		ns	
t_{VADWD}	Write Data valid after address is released in latch mode	4.5		ns	
t_{VCSWD}	Write Data valid after PBI_CS_B assertion in non-latch mode	7.5		ns	

NOTES:
1. Can be programmed to multiple integer SFN clock cycles. Assuming programmed to least amount of integer clock cycles. Note that “+w” indicates programmable wait states.
2. Calculation includes one SFN clock cycle with a period of 7.5 ns.
3. Calculation includes two SFN clock cycles. SFN clock cycle period is 7.5 ns.

Figure 6. Address Window Signal Timing Diagram



NOTE: All timing relationships are independent of each other.

Figure 7. Data Window Signal Timing Diagram

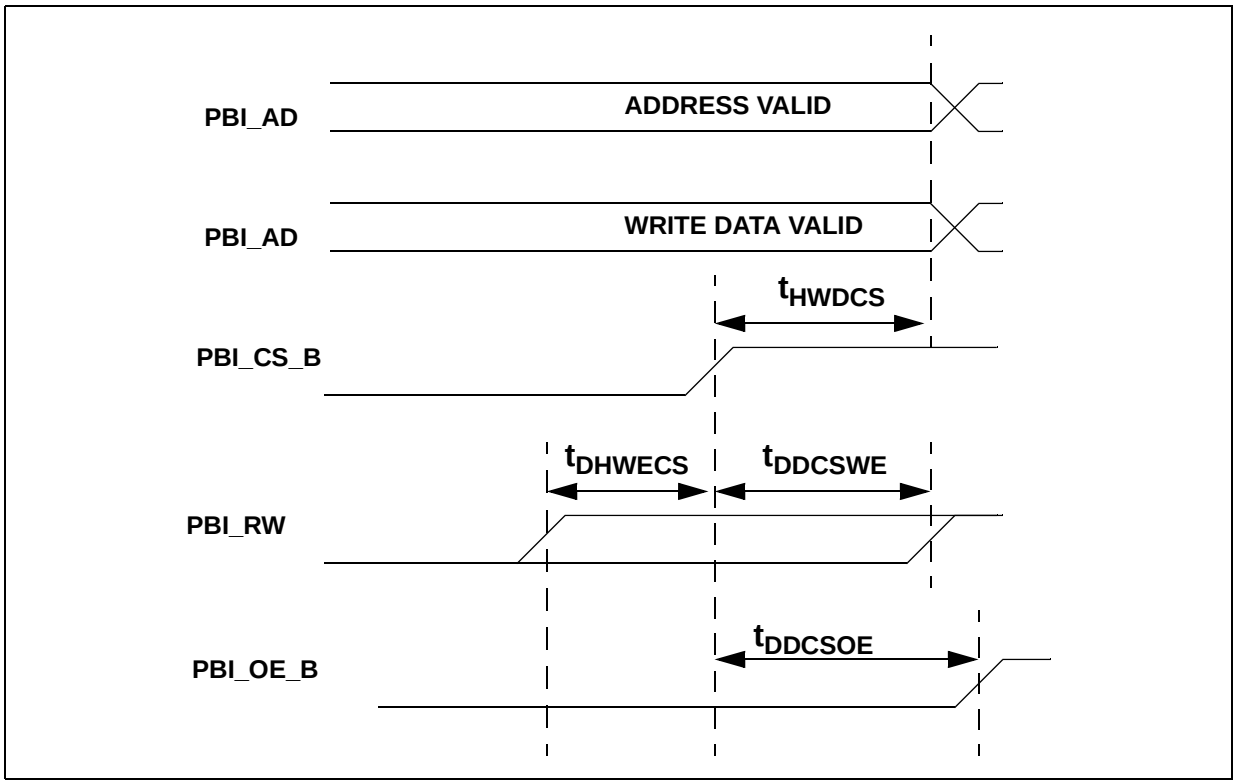
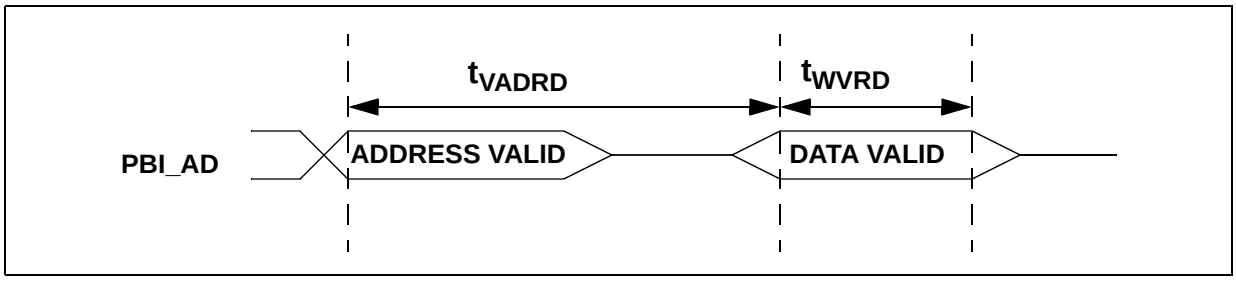


Figure 8. Address to Read Data Timing Diagram



4.4.8 I²C Interface Signal Timings

Table 39 lists the AC specifications for GW80314 I²C interfaces. The specifications are valid for both the GPIO I²C interface and the I²C interface contained within the DDR SDRAM controller.

Table 39. AC Specifications for I²C Interface

Symbol	Parameter	Std. Mode		Units	Notes
		Min.	Max.		
F_{SCL}	SD_I2C_CLK/I2C_SCLK Clock Frequency	0	100	KHz	
T_{BUF}	Bus Free Time Between STOP and START Condition	4.7	-	µs	1
T_{HDSTA}	Hold Time (repeated) START condition	4	-	µs	1,3
T_{LOW}	SD_I2C_CLK/I2C_SCLK Clock Low Time	4.7	-	µs	1,2
T_{HIGH}	SD_I2C_CLK/I2C_SCLK Clock High Time	4	-	µs	1,2
T_{SUSTA}	Setup Time for a Repeated START condition	4.7	-	µs	1
T_{HDDAT}	Data Hold Time	0	3.45	µs	1
T_{SUDAT}	Data Setup Time	250	-	ns	1
T_{SR}	SD_I2C_CLK, SD_I2C_SDA, I2C_SCLK, and I2C_SDA Rise Time	-	1000	ns	1
T_{SF}	SD_I2C_CLK, SD_I2C_SDA, I2C_SCLK, and I2C_SDA Fall Time	-	300	ns	1
T_{SUSTO}	Setup Time for STOP Condition	4	-	µs	1

NOTES:
1. See Figure 11.
2. Not tested.
3. After this period, the first clock pulse in generated.

4.4.9 Boundary Scan Test Signal Timings

Table 40. Boundary Scan Test Signal Timings

Symbol	Parameter	Min.	Max.	Units	Notes
T_{BSF}	TCK Frequency	0	10	MHz	
T_{BSCH}	TCK High Time	50	-	ns	Measured at 1.5V, 1
T_{BSCL}	TCK Low Time	50	-	ns	Measured at 1.5V, 1
T_{BSCR}	TCK Rise Time	-	25	ns	0.8V to 2.0V, 1
T_{BSCF}	TCK Fall Time	-	25	ns	2.0V to 0.8V, 1
T_{SIS1}	Input Setup to TCK	10	-	ns	4
T_{BSIH1}	Input Hold from TCK	10	-	ns	4
T_{BSOV1}	TDO Output Valid Delay from falling edge of TCK.	-	15	ns	2, 3
T_{OF1}	TDO Output Float Delay from falling edge of TCK	-	15	ns	2, 5

NOTES:
1. Not tested.
2. Outputs precharged to V_{CC5}.
3. See Figure 10.
4. See Figure 9.
5. A float condition occurs when the output current becomes less than I_{LO}. Float delay is not tested. See Figure 10.

4.5 AC Timing Waveforms

Figure 9. Input Timing Measurement Waveforms

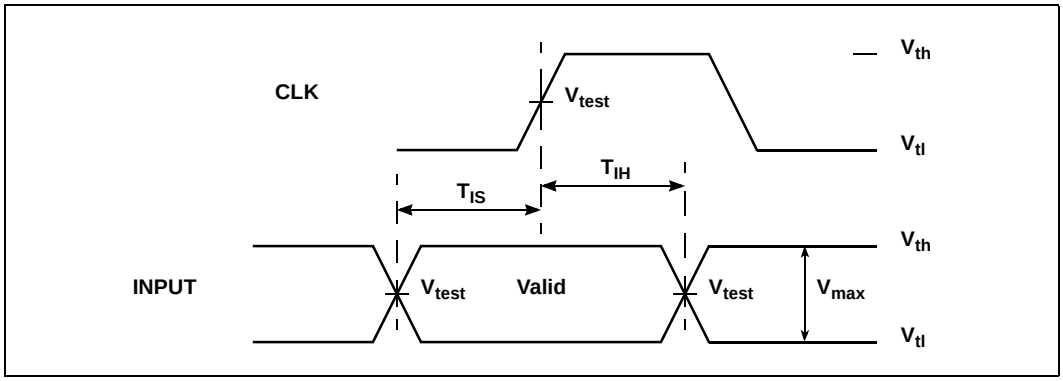


Figure 10. Output Timing Measurement Waveforms

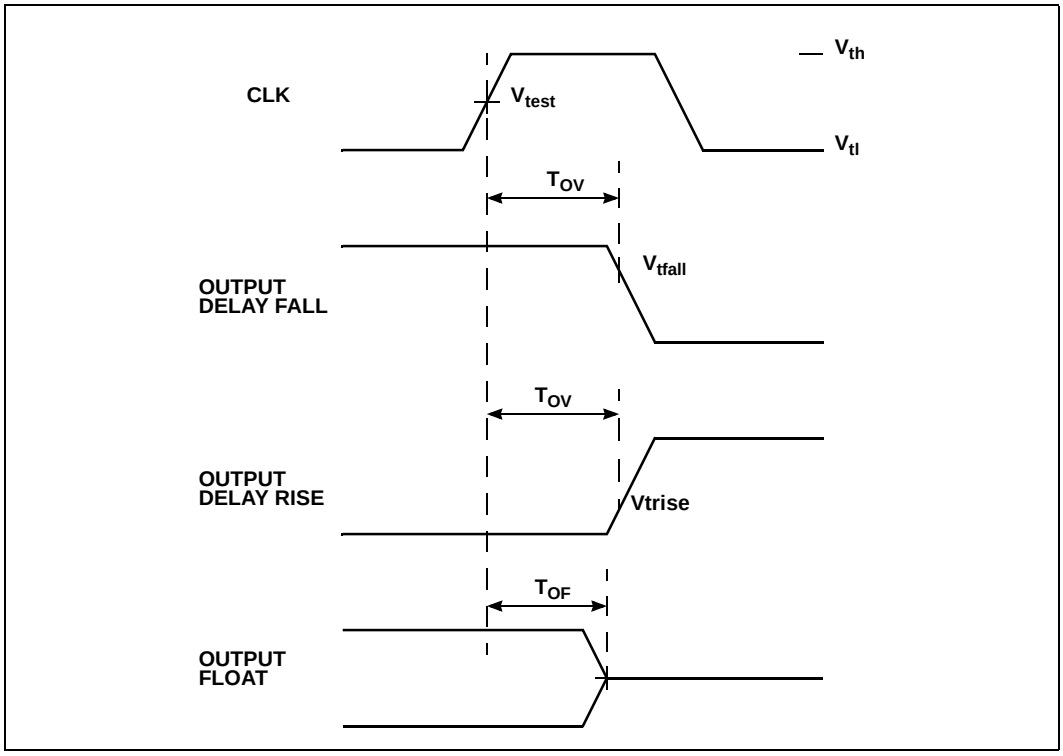


Figure 11. I²C Interface Signal Timings

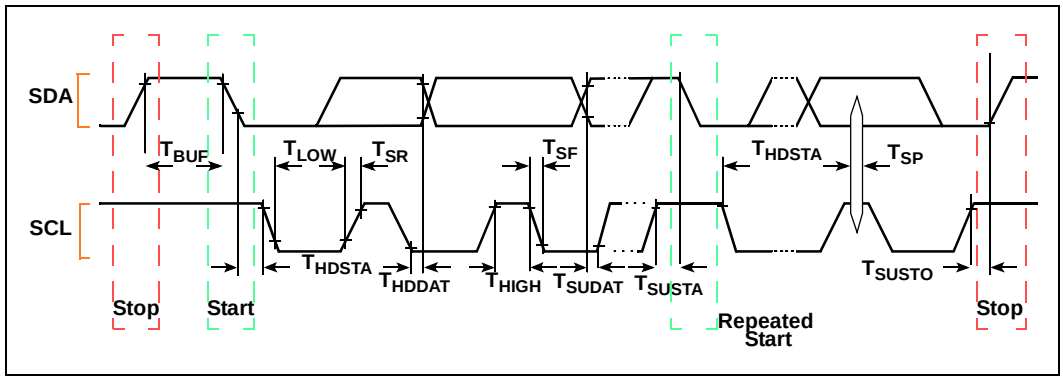


Figure 12. DDR SDRAM Write Timings

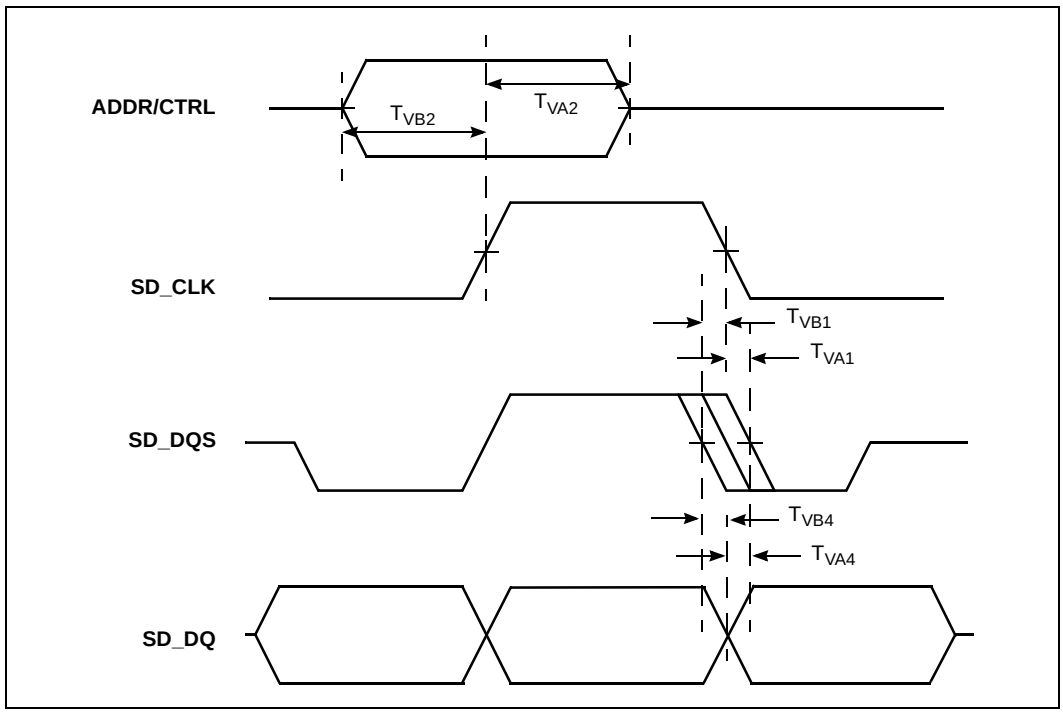
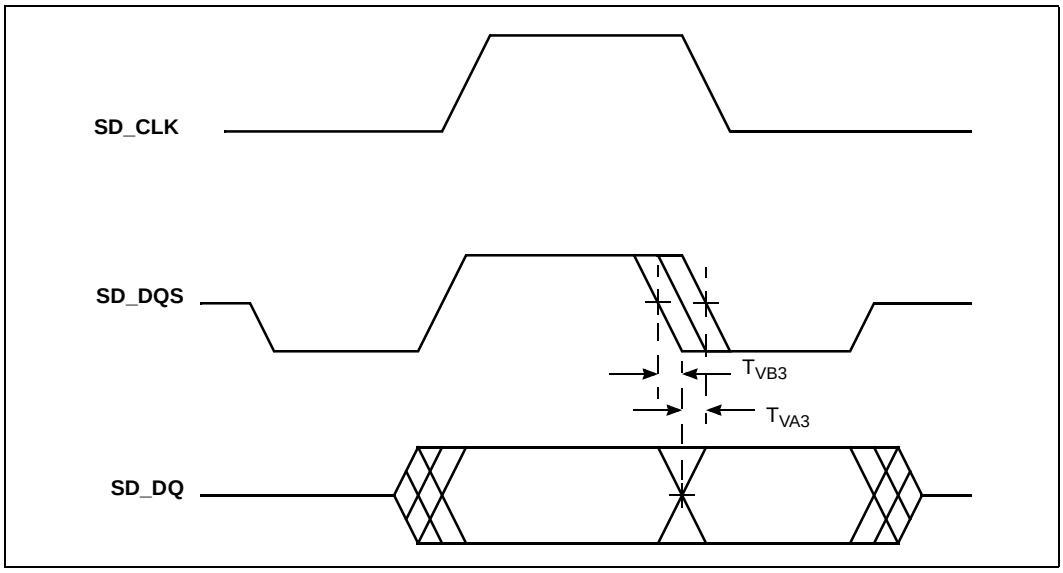


Figure 13. DDR SDRAM Read Timings



4.6 AC Test Conditions

Table 41 and Figure 14 through Figure 17 summarize the AC test and measurement conditions to be used for the GW80314.

Table 41. AC Measurement Conditions

Symbol	PCI-X	PCI	DDR	Intel XScale® Microprocessor	GigE	Units	Notes
V_{tch}	$0.6*V_{CC33}$	$0.6*V_{CC33}$	-	$0.6*V_{CC33}$	$0.6*V_{CC33}$	V	
V_{tcl}	$0.2*V_{CC33}$	$0.2*V_{CC33}$	-	$0.2*V_{CC33}$	$0.2*V_{CC33}$	V	
V_{th}	$0.6*V_{CC33}$	$0.6*V_{CC33}$	2.0	$0.6*V_{CC33}$	$0.6*V_{CC33}$	V	
V_{tl}	$0.25*V_{CC33}$	$0.2*V_{CC33}$	0.5	$0.2*V_{CC33}$	$0.2*V_{CC33}$	V	
V_{test}	$0.4*V_{CC33}$	$0.4*V_{CC33}$	1.25	$0.4*V_{CC33}$	$0.4*V_{CC33}$	V	
V_{trise}	$0.285*V_{CC33}$	$0.285*V_{CC33}$	1.25	$0.285*V_{CC33}$	$0.285*V_{CC33}$	V	
V_{fall}	$0.615*V_{CC33}$	$0.615*V_{CC33}$	1.25	$0.615*V_{CC33}$	$0.615*V_{CC33}$	V	
V_{max}	$0.4*V_{CC33}$	$0.4*V_{CC33}$	1.5	$0.4*V_{CC33}$	$0.4*V_{CC33}$	V	
Slew Rate	1 - 6	1 - 6	1.5	1.5	1.5	V/ns	1

NOTE: Input signal slew rate is measured between V_{IL} and V_{IH}.

Figure 14. AC Test Load for all Signals Except PCI and DDR SDRAM

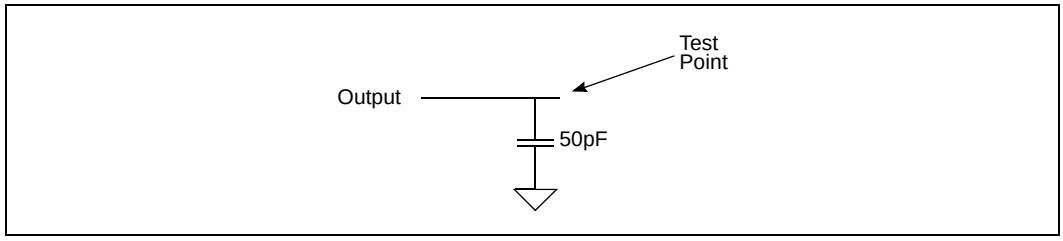


Figure 15. PCI/PCI-X $T_{OV(max)}$ Rising Edge AC Test Load

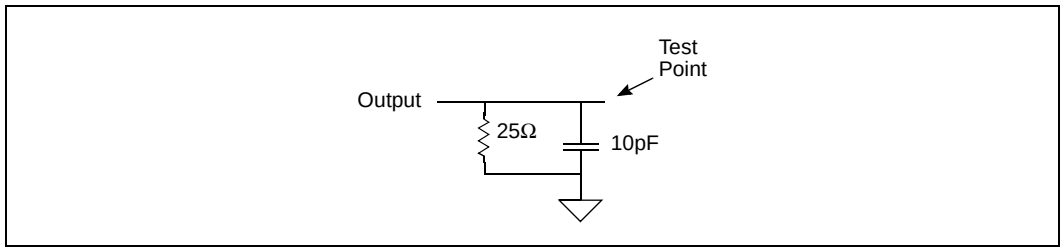


Figure 16. PCI/PCI-X $T_{OV(max)}$ Falling Edge AC Test Load

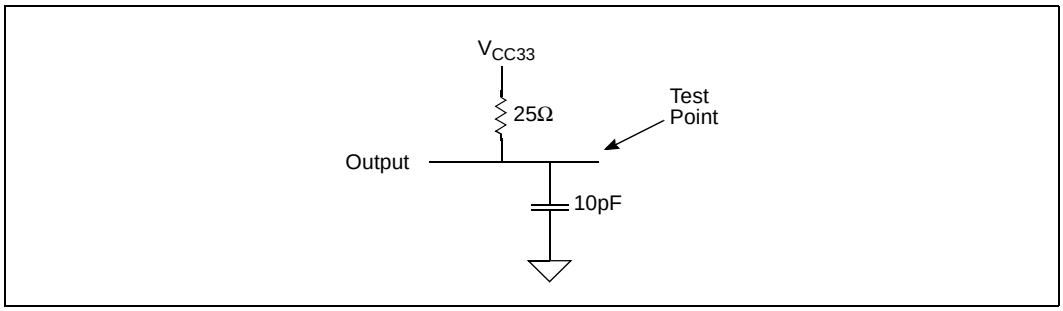
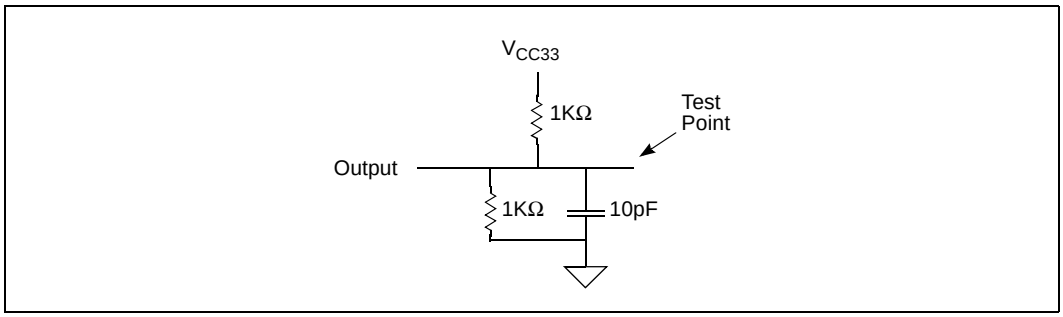


Figure 17. PCI/PCI-X $T_{OV(min)}$ AC Test Load



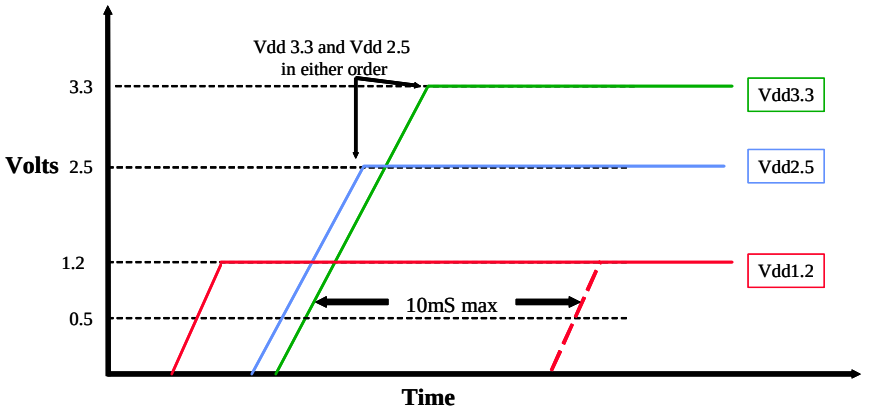
4.7 Power Sequencing

The power-up and power-down sequences for the 1.2 V/2.5 V/3.3 V supply rails are specified below:

- The 1.2 V rail can be ramped before the 2.5 V and/or 3.3 V rails.
- Current transients can occur when the 1.2 V supply is ramped after the 2.5 V and/or 3.3 V supply rails.
- The transients are acceptable when the 1.2 V lag is less than or equal to 20 ms.
- Transient currents of up to 2 A/$V_{DD2.5}$ and 4 A/$V_{DD3.3}$ can occur on the supplies until $V_{DD1.2}$ >= ~0.6 V.
- The 1.2 V supply can power-down before 3.3 V/2.5 V by no more than 20 ms, or any time after.

These requirements are illustrated in Figure 18.

Figure 18. Correct Power Sequence for V_{DD33}, V_{DD25}, and V_{DD12}



- Vdd 3.3 and Vdd 2.5 can come up in either order relative to each other
- Vdd 1.2 can proceed V3.3 and Vdd 2.5 or lag up to 20mS max
- If Vdd 1.2 lags Vdd 3.3 and/or Vdd 2.5 transient currents of up to 2A/Vdd 2.5 and 4A/Vdd 3.3 occur on the supplies until Vdd 1.2 >= ~0.6v
- 1.2V can power down before 3.3V/2.5V by no more than 20ms or any time after 3.3V/2.5V.

Power-sequencing rules must be applied for both power-up and power-down. While only power-up sequencing is described in the graphs and paragraphs below, power-down sequencing must comply with the same rules.

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