

Analog Multiplexers/ Demultiplexers

High-Performance Silicon-Gate CMOS

MC74HC4051A, MC74HC4052A, MC74HC4053A

The MC74HC4051A, MC74HC4052A and MC74HC4053A utilize silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The HC4051A, HC4052A and HC4053A are identical in pinout to the metal-gate MC14051AB, MC14052AB and MC14053AB. The Channel-Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel-Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors they are compatible with LSTTL outputs.

These devices have been designed so that the ON resistance (R_{ON}) is more linear over input voltage than R_{ON} of metal-gate CMOS analog switches.

For a multiplexer/demultiplexer with injection current protection, see HC4851A and HC4852A.

Features

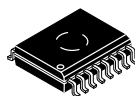
- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range ($V_{CC} - V_{EE}$) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range ($V_{CC} - GND$) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal-Gate Counterparts
- Low Noise
- In Compliance with the Requirements of JEDEC Standard No. 7A
- Chip Complexity: HC4051A – 184 FETs or 46 Equivalent Gates
HC4052A – 168 FETs or 42 Equivalent Gates
HC4053A – 156 FETs or 39 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR-Free and are RoHS Compliant

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.

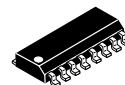


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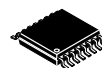
www.onsemi.com



SOIC-16 WIDE
DW SUFFIX
CASE 751G



SOIC-16
D SUFFIX
CASE 751B

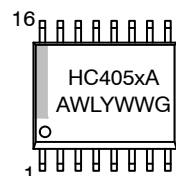


TSSOP-16
DT SUFFIX
CASE 948F

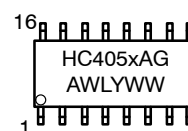


QFN16
MN SUFFIX
CASE 485AW

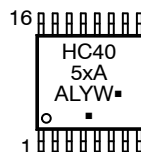
MARKING DIAGRAMS



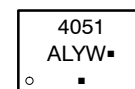
SOIC-16 WIDE



SOIC-16



TSSOP-16



QFN16

x = 1, 2 or 3
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

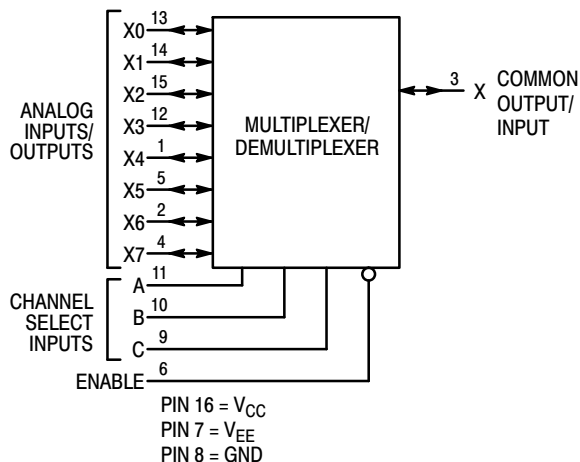
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

MC74HC4051A, MC74HC4052A, MC74HC4053A

LOGIC DIAGRAM
MC74HC4051A
Single-Pole, 8-Position Plus Common Off

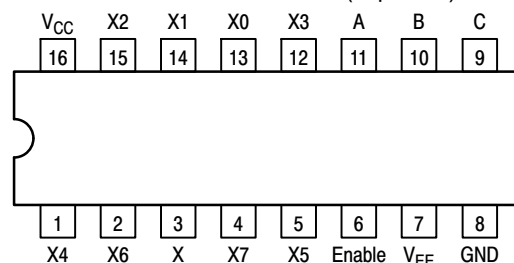


FUNCTION TABLE – MC74HC4051A

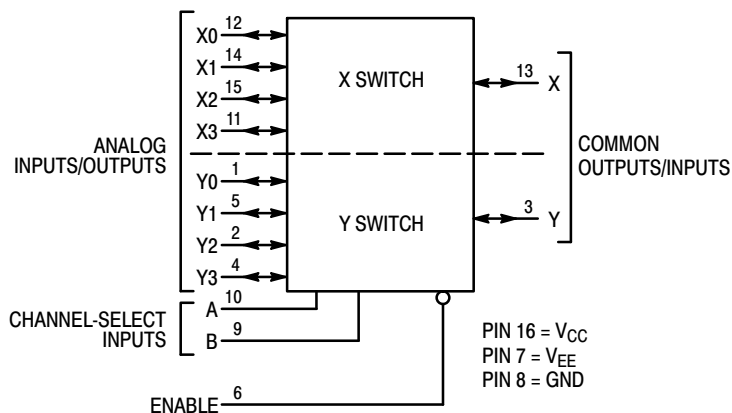
| Control Inputs | | | | ON Channels |
|----------------|--------|---|---|-------------|
| Enable | Select | | | |
| | C | B | A | |
| L | L | L | L | X0 |
| L | L | L | H | X1 |
| L | L | H | L | X2 |
| L | L | H | H | X3 |
| L | H | L | L | X4 |
| L | H | L | H | X5 |
| L | H | H | L | X6 |
| L | H | H | H | X7 |
| H | X | X | X | NONE |

X = Don't Care

Pinout: MC74HC4051A (Top View)



LOGIC DIAGRAM
MC74HC4052A
Double-Pole, 4-Position Plus Common Off

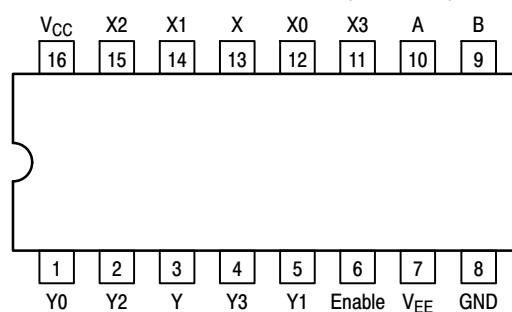


FUNCTION TABLE – MC74HC4052A

| Control Inputs | | | | |
|----------------|--------|---|-------------|----|
| Enable | Select | | | |
| | B | A | ON Channels | |
| L | L | L | Y0 | X0 |
| L | L | H | Y1 | X1 |
| L | H | L | Y2 | X2 |
| L | H | H | Y3 | X3 |
| H | X | X | NONE | |

X = Don't Care

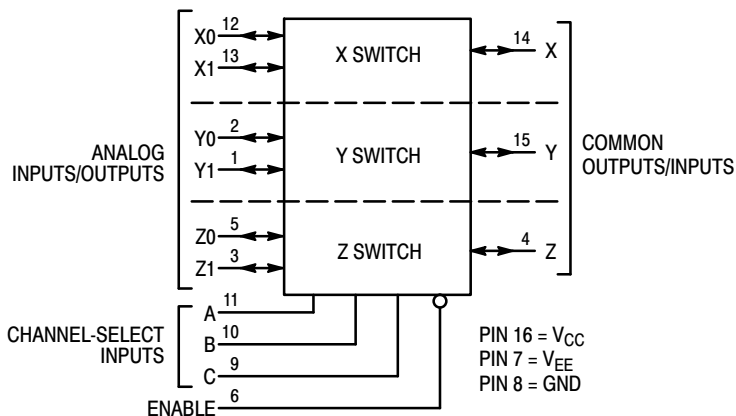
Pinout: MC74HC4052A (Top View)



MC74HC4051A, MC74HC4052A, MC74HC4053A

LOGIC DIAGRAM MC74HC4053A

Triple Single-Pole, Double-Position Plus Common Off



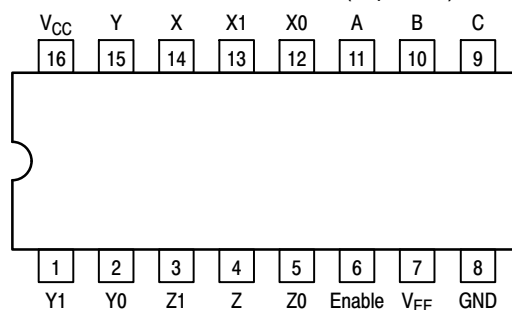
NOTE: This device allows independent control of each switch. Channel-Select Input A controls the X-Switch, Input B controls the Y-Switch and Input C controls the Z-Switch

FUNCTION TABLE – MC74HC4053A

| Control Inputs | | | | ON Channels | | |
|----------------|---|---|---|-------------|----|----|
| Enable | C | B | A | | | |
| L | L | L | L | Z0 | Y0 | X0 |
| L | L | L | H | Z0 | Y0 | X1 |
| L | L | H | L | Z0 | Y1 | X0 |
| L | L | H | H | Z0 | Y1 | X1 |
| L | H | L | L | Z1 | Y0 | X0 |
| L | H | L | H | Z1 | Y0 | X1 |
| L | H | H | L | Z1 | Y1 | X0 |
| L | H | H | H | Z1 | Y1 | X1 |
| H | X | X | X | NONE | | |

X = Don't Care

Pinout: MC74HC4053A (Top View)



MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------|---|----------------------------------|------|
| V_{CC} | Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE}) | -0.5 to +7.0 -0.5 to +14.0 | V |
| V_{EE} | Negative DC Supply Voltage (Referenced to GND) | -7.0 to +5.0 | V |
| V_{IS} | Analog Input Voltage | $V_{EE} - 0.5$ to $V_{CC} + 0.5$ | V |
| V_{in} | Digital Input Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| I | DC Current, Into or Out of Any Pin | ± 25 | mA |
| P_D | Power Dissipation in Still Air, SOIC Package† TSSOP Package† | 500 450 | mW |
| T_{stg} | Storage Temperature Range | -65 to +150 | °C |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds SOIC or TSSOP Package | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: -7 mW/°C from 65° to 125°C

TSSOP Package: -6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------|---|------------------|---------------------------|------|
| V_{CC} | Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE}) | 2.0 2.0 | 6.0 12.0 | V |
| V_{EE} | Negative DC Supply Voltage, Output (Referenced to GND) | -6.0 | GND | V |
| V_{IS} | Analog Input Voltage | V_{EE} | V_{CC} | V |
| V_{in} | Digital Input Voltage (Referenced to GND) | GND | V_{CC} | V |
| V_{IO}^* | Static or Dynamic Voltage Across Switch | | 1.2 | V |
| T_A | Operating Temperature Range, All Package Types | -55 | +125 | °C |
| t_r, t_f | Input Rise/Fall Time (Channel Select or Enable Inputs) $V_{CC} = 2.0\text{ V}$ $V_{CC} = 3.0\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6.0\text{ V}$ | 0 0 0 0 | 1000 600 500 400 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

*For voltage drops across switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND) $V_{EE} = \text{GND}$, Except Where Noted

| Symbol | Parameter | Condition | V_{CC} V | Guaranteed Limit | | | Unit |
|----------|---|--|--------------------------|------------------------------|------------------------------|------------------------------|------|
| | | | | -55 to 25°C | ≤85°C | ≤125°C | |
| V_{IH} | Minimum High-Level Input Voltage, Channel-Select or Enable Inputs | $R_{on} = \text{Per Spec}$ | 2.0 3.0 4.5 6.0 | 1.50 2.10 3.15 4.20 | 1.50 2.10 3.15 4.20 | 1.50 2.10 3.15 4.20 | V |
| V_{IL} | Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs | $R_{on} = \text{Per Spec}$ | 2.0 3.0 4.5 6.0 | 0.5 0.9 1.35 1.8 | 0.5 0.9 1.35 1.8 | 0.5 0.9 1.35 1.8 | V |
| I_{in} | Maximum Input Leakage Current, Channel-Select or Enable Inputs | $V_{in} = V_{CC}$ or GND, $V_{EE} = -6.0\text{ V}$ | 6.0 | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| I_{CC} | Maximum Quiescent Supply Current (per Package) | Channel Select, Enable and $V_{IS} = V_{CC}$ or GND; $V_{EE} = \text{GND}$ $V_{IO} = 0\text{ V}$ $V_{EE} = -6.0$ | 6.0 6.0 | 1 4 | 10 40 | 20 80 | μA |

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DC CHARACTERISTICS — Analog Section

| Symbol | Parameter | Condition | V _{CC} | V _{EE} | Guaranteed Limit | | | Unit |
|------------------|--|---|-------------------|-------------------------|-------------------|-------------------|-------------------|------|
| | | | | | –55 to 25°C | ≤85°C | ≤125°C | |
| R _{on} | Maximum “ON” Resistance | V _{in} = V _{IL} or V _{IH} ; V _{IS} = V _{CC} to V _{EE} ; I _S ≤ 2.0 mA (Figures 1, 2) | 4.5 4.5 6.0 | 0.0 – 4.5 – 6.0 | 190 120 100 | 240 150 125 | 280 170 140 | Ω |
| | | V _{in} = V _{IL} or V _{IH} ; V _{IS} = V _{CC} or V _{EE} (Endpoints); I _S ≤ 2.0 mA (Figures 1, 2) | 4.5 4.5 6.0 | 0.0 – 4.5 – 6.0 | 150 100 80 | 190 125 100 | 230 140 115 | |
| ΔR _{on} | Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package | V _{in} = V _{IL} or V _{IH} ; V _{IS} = 1/2 (V _{CC} – V _{EE}); I _S ≤ 2.0 mA | 4.5 4.5 6.0 | 0.0 – 4.5 – 6.0 | 30 12 10 | 35 15 12 | 40 18 14 | Ω |
| I _{off} | Maximum Off–Channel Leakage Current, Any One Channel | V _{in} = V _{IL} or V _{IH} ; V _{IO} = V _{CC} – V _{EE} ; Switch Off (Figure 3) | 6.0 | – 6.0 | 0.1 | 0.5 | 1.0 | μA |
| | Maximum Off–Channel Leakage Current, Common Channel | V _{in} = V _{IL} or V _{IH} ; V _{IO} = V _{CC} – V _{EE} ; Switch Off (Figure 4) | 6.0 6.0 6.0 | – 6.0 – 6.0 – 6.0 | 0.2 0.1 0.1 | 2.0 1.0 1.0 | 4.0 2.0 2.0 | |
| | Maximum On–Channel Leakage Current, Channel–to–Channel | V _{in} = V _{IL} or V _{IH} ; Switch–to–Switch = V _{CC} – V _{EE} ; (Figure 5) | 6.0 6.0 6.0 | – 6.0 – 6.0 – 6.0 | 0.2 0.1 0.1 | 2.0 1.0 1.0 | 4.0 2.0 2.0 | |

AC CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|--|---|--|------------------|-------|--------|------|
| | | | –55 to 25°C | ≤85°C | ≤125°C | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Channel–Select to Analog Output (Figure 9) | 2.0 | 270 | 320 | 350 | ns |
| | | 3.0 | 90 | 110 | 125 | |
| | | 4.5 | 59 | 79 | 85 | |
| | | 6.0 | 45 | 65 | 75 | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Analog Input to Analog Output (Figure 10) | 2.0 | 40 | 60 | 70 | ns |
| | | 3.0 | 25 | 30 | 32 | |
| | | 4.5 | 12 | 15 | 18 | |
| | | 6.0 | 10 | 13 | 15 | |
| t _{PLZ} , t _{PHZ} | Maximum Propagation Delay, Enable to Analog Output (Figure 11) | 2.0 | 160 | 200 | 220 | ns |
| | | 3.0 | 70 | 95 | 110 | |
| | | 4.5 | 48 | 63 | 76 | |
| | | 6.0 | 39 | 55 | 63 | |
| t _{PZL} , t _{PZH} | Maximum Propagation Delay, Enable to Analog Output (Figure 11) | 2.0 | 245 | 315 | 345 | ns |
| | | 3.0 | 115 | 145 | 155 | |
| | | 4.5 | 49 | 69 | 83 | |
| | | 6.0 | 39 | 58 | 67 | |
| C _{in} | Maximum Input Capacitance, Channel–Select or Enable Inputs | | 10 | 10 | 10 | pF |
| C _{I/O} | Maximum Capacitance Analog I/O | | 35 | 35 | 35 | pF |
| | Common O/I: HC4051A | | 130 | 130 | 130 | |
| | HC4052A | | 80 | 80 | 80 | |
| | HC4053A | | 50 | 50 | 50 | |
| | Feed–through | | 1.0 | 1.0 | 1.0 | |
| C _{PD} | Power Dissipation Capacitance (Figure 13)* | Typical @ 25°C, V _{CC} = 5.0 V, V _{EE} = 0 V | | | | pF |
| | | HC4051A | 45 | | | |
| | | HC4052A | 80 | | | |
| | | HC4053A | 45 | | | |

* Used to determine the no–load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}.

MC74HC4051A, MC74HC4052A, MC74HC4053A

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

| Symbol | Parameter | Condition | V _{CC} V | V _{EE} V | Limit* | | | Unit |
|--------|---|--|----------------------|----------------------|--------|-----|-----|------------------|
| | | | | | 25°C | | | |
| BW | Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 6) | f _{in} = 1MHz Sine Wave; Adjust f _{in} Voltage to Obtain 0dBm at V _{OS} ; Increase f _{in} Frequency Until dB Meter Reads -3dB; R _L = 50Ω, C _L = 10pF | | | '51 | '52 | '53 | MHz |
| | | | 2.25 | -2.25 | 80 | 95 | 120 | |
| | | | 4.50 | -4.50 | 80 | 95 | 120 | |
| | | | 6.00 | -6.00 | 80 | 95 | 120 | |
| - | Off-Channel Feed-through Isolation (Figure 7) | f _{in} = Sine Wave; Adjust f _{in} Voltage to Obtain 0dBm at V _{IS} f _{in} = 10kHz, R _L = 600Ω, C _L = 50pF | 2.25 | -2.25 | -50 | | | dB |
| | | | 4.50 | -4.50 | -50 | | | |
| | | | 6.00 | -6.00 | -50 | | | |
| | | f _{in} = 1.0MHz, R _L = 50Ω, C _L = 10pF | 2.25 | -2.25 | -40 | | | |
| | | | 4.50 | -4.50 | -40 | | | |
| | | | 6.00 | -6.00 | -40 | | | |
| - | Feedthrough Noise. Channel-Select Input to Common I/O (Figure 8) | V _{in} ≤ 1MHz Square Wave (t _r = t _f = 6ns); Adjust R _L at Setup so that I _S = 0A; Enable = GND R _L = 600Ω, C _L = 50pF | 2.25 | -2.25 | 25 | | | mV _{pp} |
| | | | 4.50 | -4.50 | 105 | | | |
| | | | 6.00 | -6.00 | 135 | | | |
| | | R _L = 10kΩ, C _L = 10pF | 2.25 | -2.25 | 35 | | | |
| | | | 4.50 | -4.50 | 145 | | | |
| | | | 6.00 | -6.00 | 190 | | | |
| - | Crosstalk Between Any Two Switches (Figure 12) (Test does not apply to HC4051A) | f _{in} = Sine Wave; Adjust f _{in} Voltage to Obtain 0dBm at V _{IS} f _{in} = 10kHz, R _L = 600Ω, C _L = 50pF | 2.25 | -2.25 | -50 | | | dB |
| | | | 4.50 | -4.50 | -50 | | | |
| | | | 6.00 | -6.00 | -50 | | | |
| | | f _{in} = 1.0MHz, R _L = 50Ω, C _L = 10pF | 2.25 | -2.25 | -60 | | | |
| | | | 4.50 | -4.50 | -60 | | | |
| | | | 6.00 | -6.00 | -60 | | | |
| THD | Total Harmonic Distortion (Figure 14) | f _{in} = 1kHz, R _L = 10kΩ, C _L = 50pF THD = THD _{measured} - THD _{source} V _{IS} = 4.0V _{pp} sine wave V _{IS} = 8.0V _{pp} sine wave V _{IS} = 11.0V _{pp} sine wave | 2.25 | -2.25 | 0.10 | | | % |
| | | | 4.50 | -4.50 | 0.08 | | | |
| | | | 6.00 | -6.00 | 0.05 | | | |
| | | | | | | | | |

*Limits not tested. Determined by design and verified by qualification.

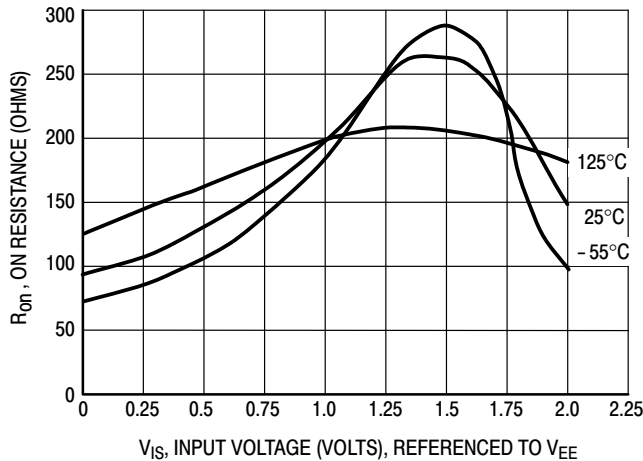


Figure 1a. Typical On Resistance, V_{CC} - V_{EE} = 2.0 V

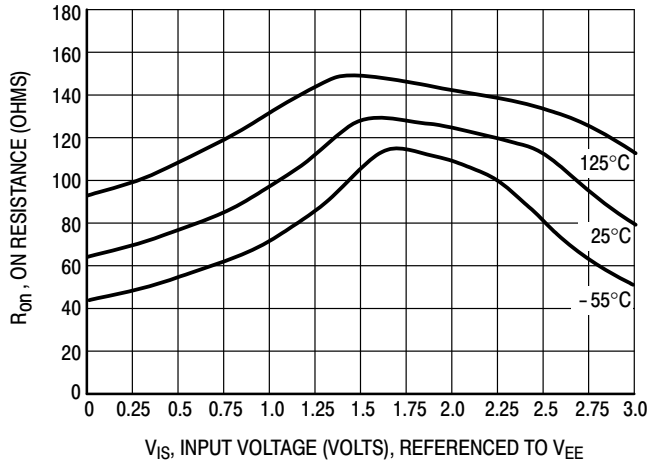


Figure 1b. Typical On Resistance, V_{CC} - V_{EE} = 3.0 V

MC74HC4051A, MC74HC4052A, MC74HC4053A

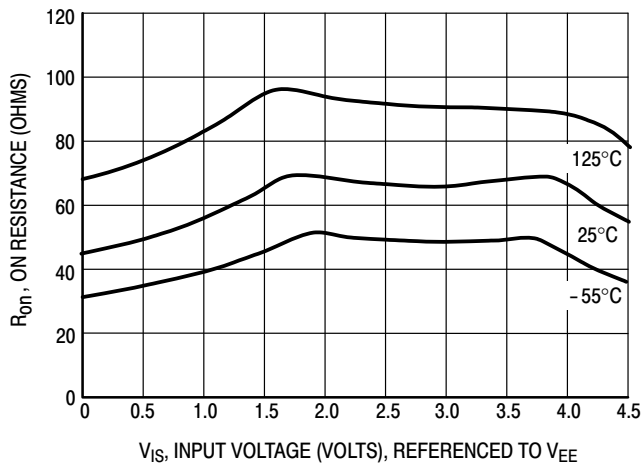


Figure 1c. Typical On Resistance, $V_{CC} - V_{EE} = 4.5 \text{ V}$

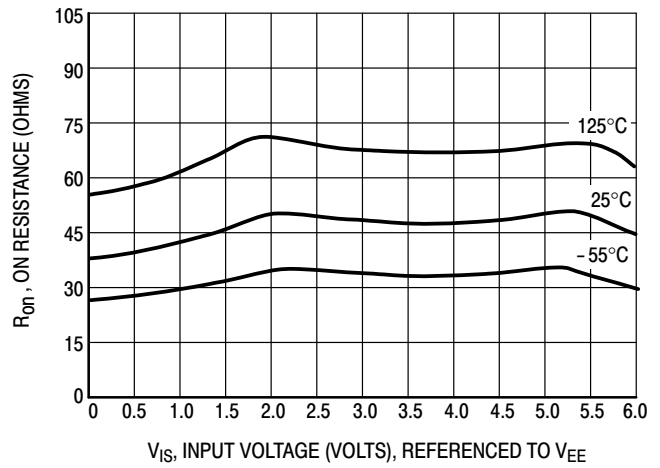


Figure 1d. Typical On Resistance, $V_{CC} - V_{EE} = 6.0 \text{ V}$

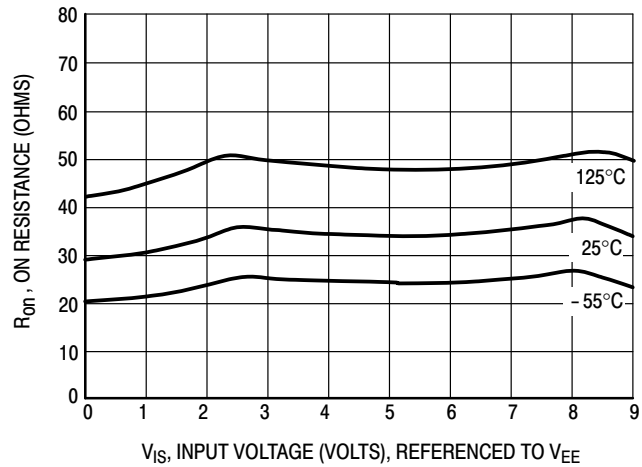


Figure 1e. Typical On Resistance, $V_{CC} - V_{EE} = 9.0 \text{ V}$

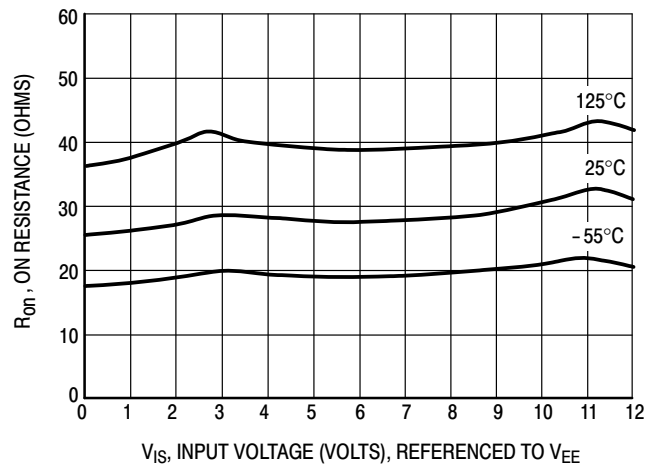


Figure 1f. Typical On Resistance, $V_{CC} - V_{EE} = 12.0 \text{ V}$

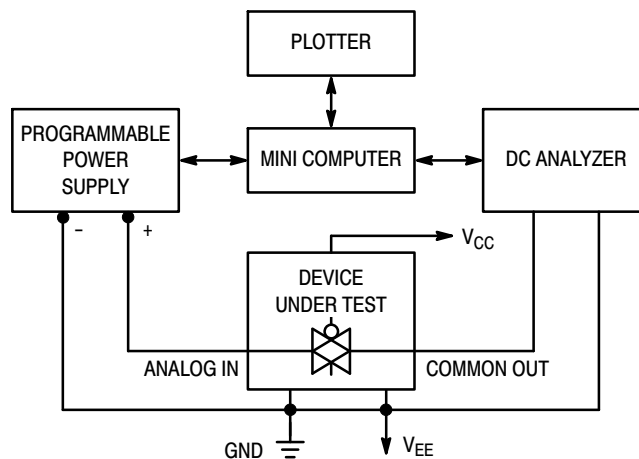


Figure 2. On Resistance Test Set-Up

MC74HC4051A, MC74HC4052A, MC74HC4053A

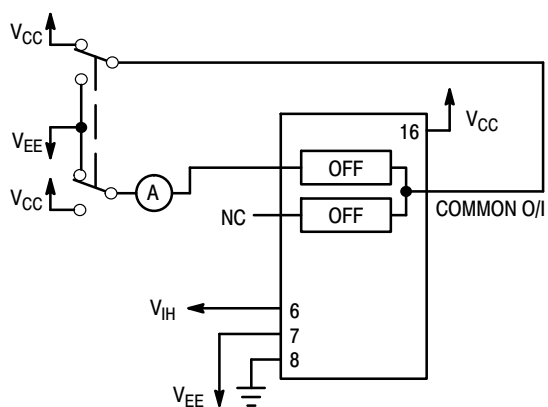


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

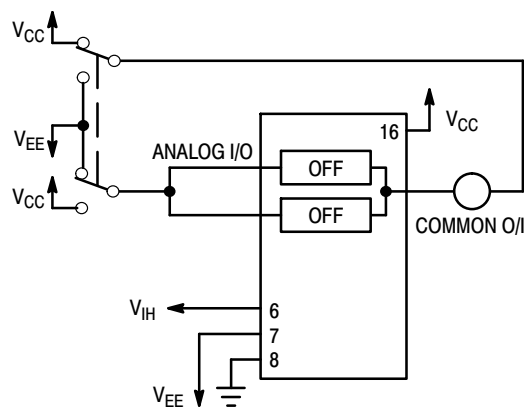


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

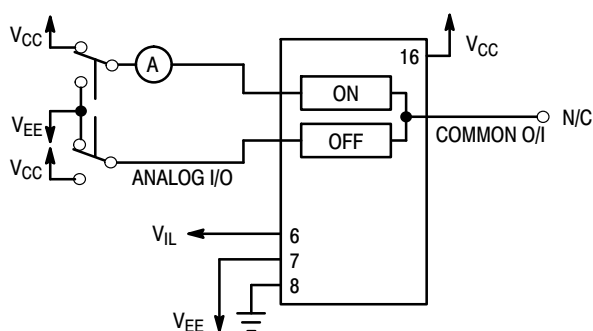
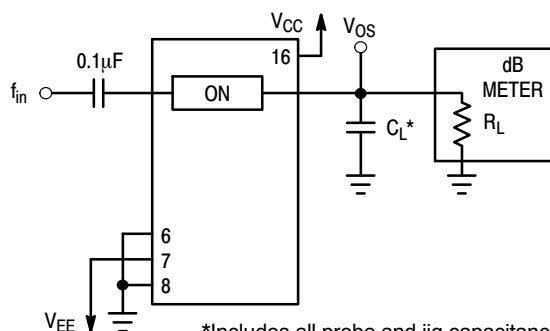
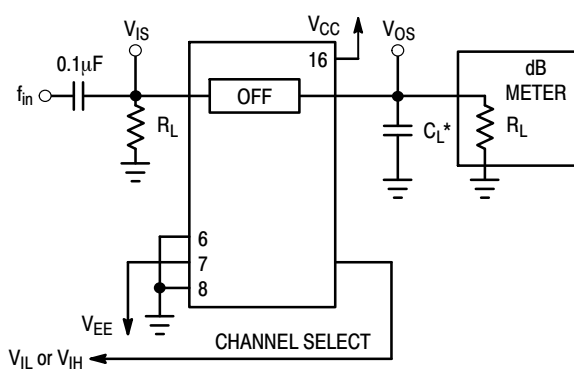


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up



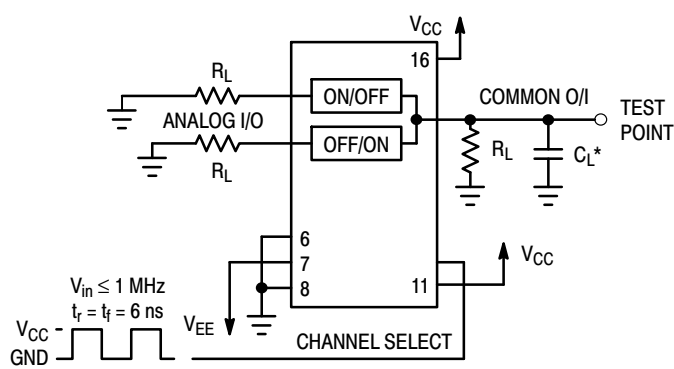
*Includes all probe and jig capacitance

Figure 6. Maximum On Channel Bandwidth, Test Set-Up



*Includes all probe and jig capacitance

Figure 7. Off Channel Feedthrough Isolation, Test Set-Up



*Includes all probe and jig capacitance

Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set-Up

MC74HC4051A, MC74HC4052A, MC74HC4053A

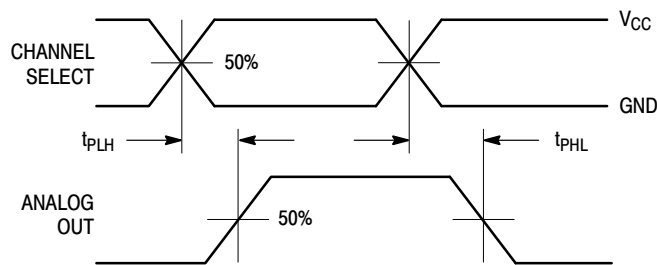
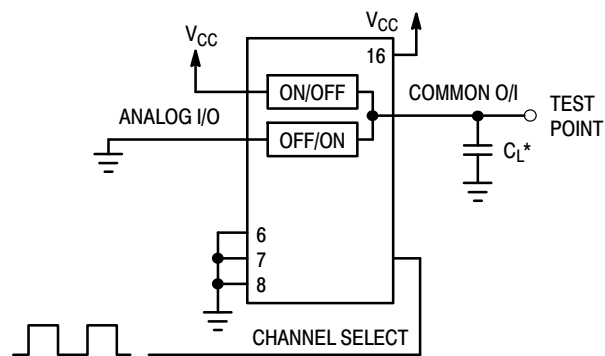


Figure 9a. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 9b. Propagation Delay, Test Set-Up Channel Select to Analog Out

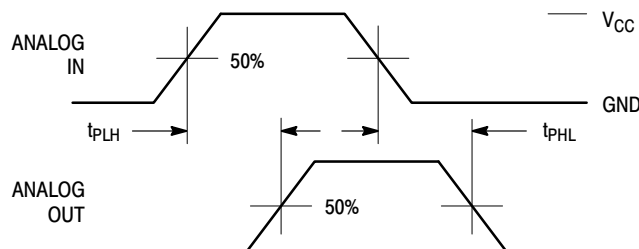
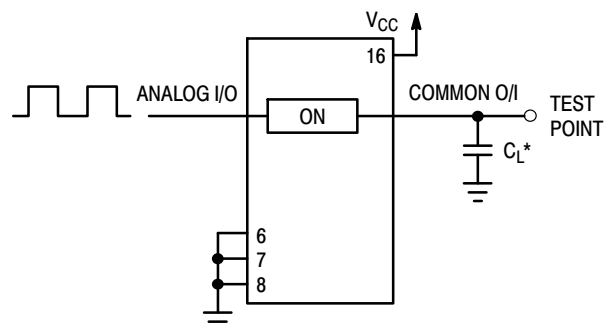


Figure 10a. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance

Figure 10b. Propagation Delay, Test Set-Up Analog In to Analog Out

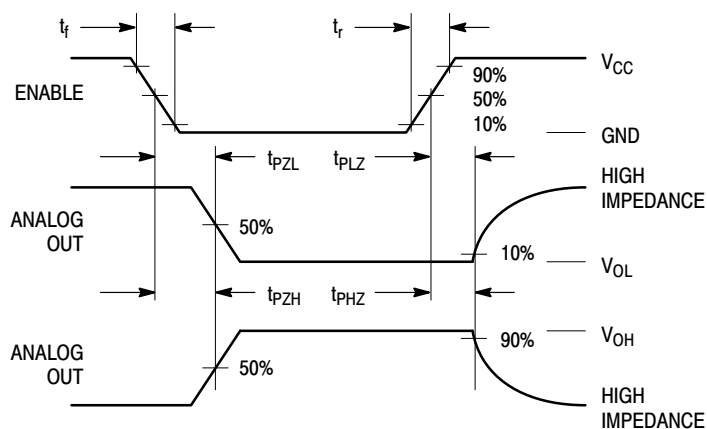


Figure 11a. Propagation Delays, Enable to Analog Out

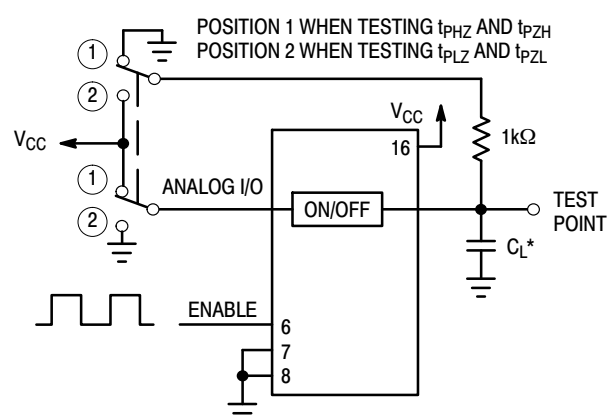
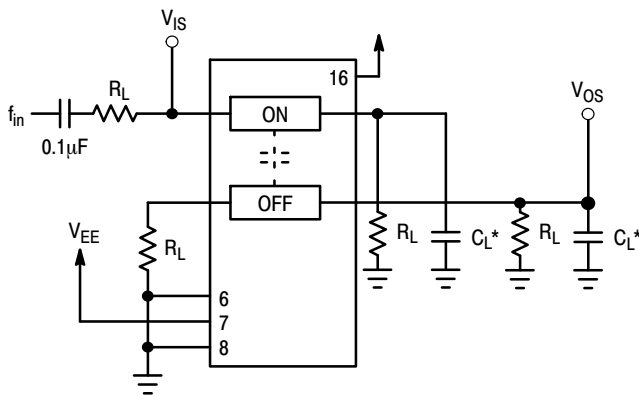


Figure 11b. Propagation Delay, Test Set-Up Enable to Analog Out

MC74HC4051A, MC74HC4052A, MC74HC4053A



*Includes all probe and jig capacitance

Figure 12. Crosstalk Between Any Two Switches, Test Set-Up

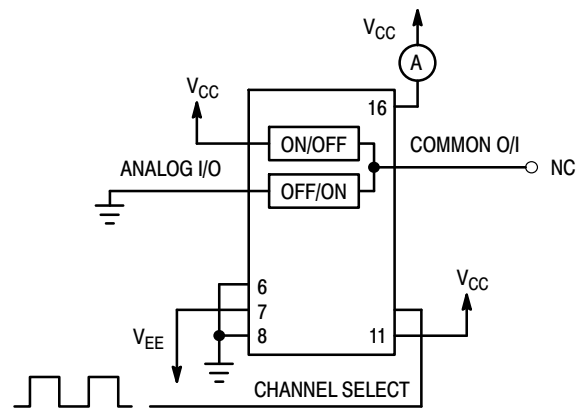
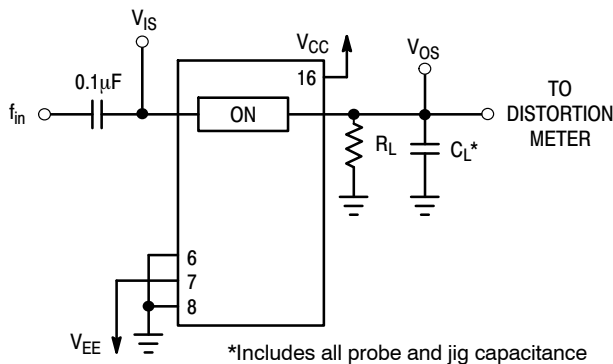


Figure 13. Power Dissipation Capacitance, Test Set-Up



*Includes all probe and jig capacitance

Figure 14a. Total Harmonic Distortion, Test Set-Up

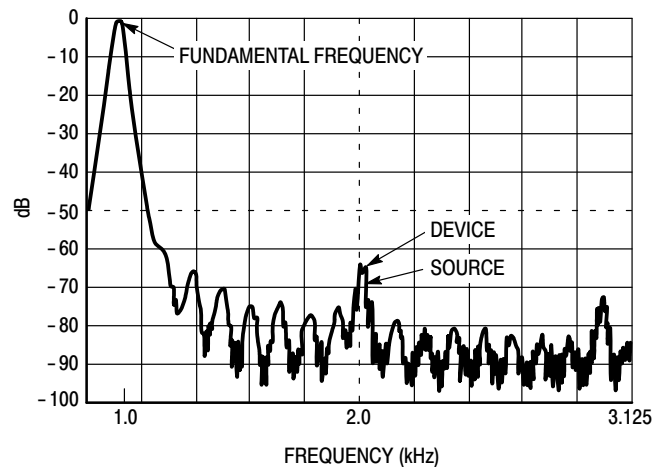


Figure 14b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

$$\begin{aligned} V_{CC} &= +5V = \text{logic high} \\ \text{GND} &= 0V = \text{logic low} \end{aligned}$$

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE} . The positive peak analog voltage should not exceed V_{CC} . Similarly, the negative peak analog voltage should not go below V_{EE} . In this example, the difference between V_{CC} and V_{EE} is ten volts. Therefore, using the configuration of Figure 15, a maximum analog signal of ten volts peak-to-peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and

outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feed-through noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$$\begin{aligned} V_{CC} - \text{GND} &= 2 \text{ to } 6 \text{ volts} \\ V_{EE} - \text{GND} &= 0 \text{ to } -6 \text{ volts} \\ V_{CC} - V_{EE} &= 2 \text{ to } 12 \text{ volts} \\ &\text{and } V_{EE} \leq \text{GND} \end{aligned}$$

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external Germanium or Schottky diodes (D_x) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

MC74HC4051A, MC74HC4052A, MC74HC4053A

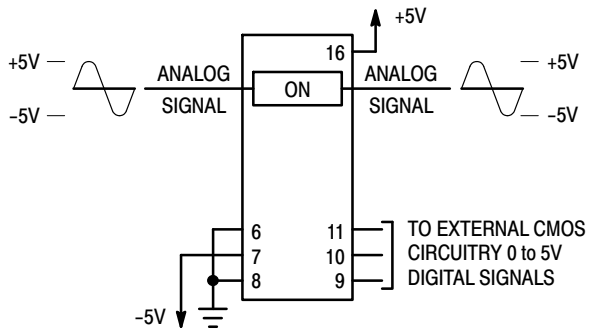


Figure 15. Application Example

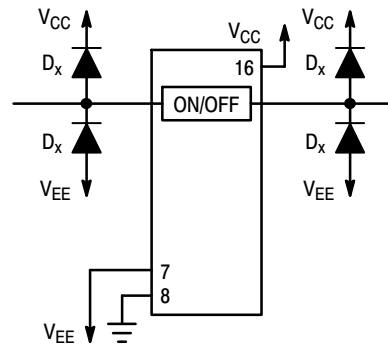
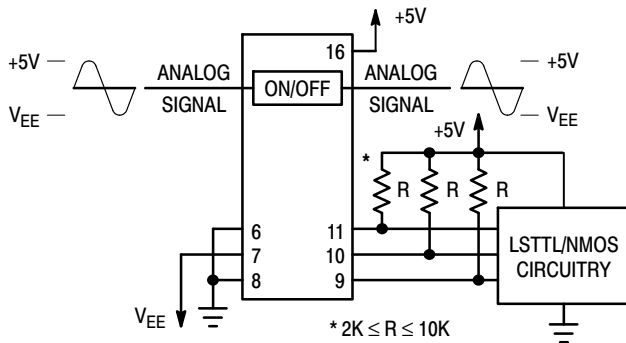
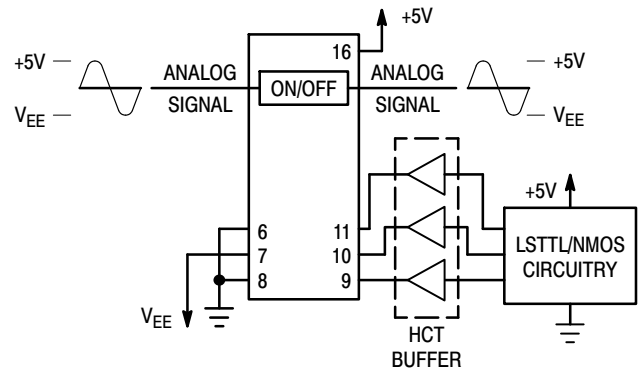


Figure 16. External Germanium or Schottky Clipping Diodes



a. Using Pull-Up Resistors



b. Using HCT Interface

Figure 17. Interfacing LSTTL/NMOS to CMOS Inputs

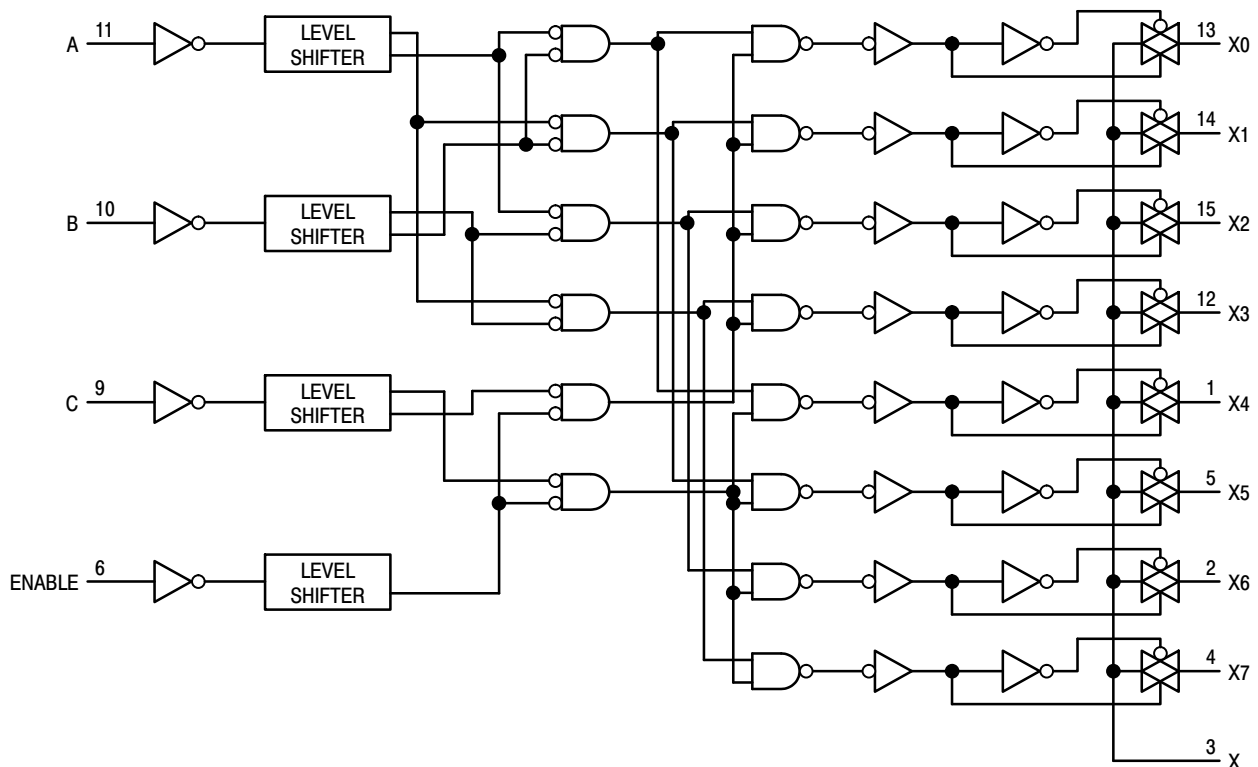


Figure 18. Function Diagram, HC4051A

MC74HC4051A, MC74HC4052A, MC74HC4053A

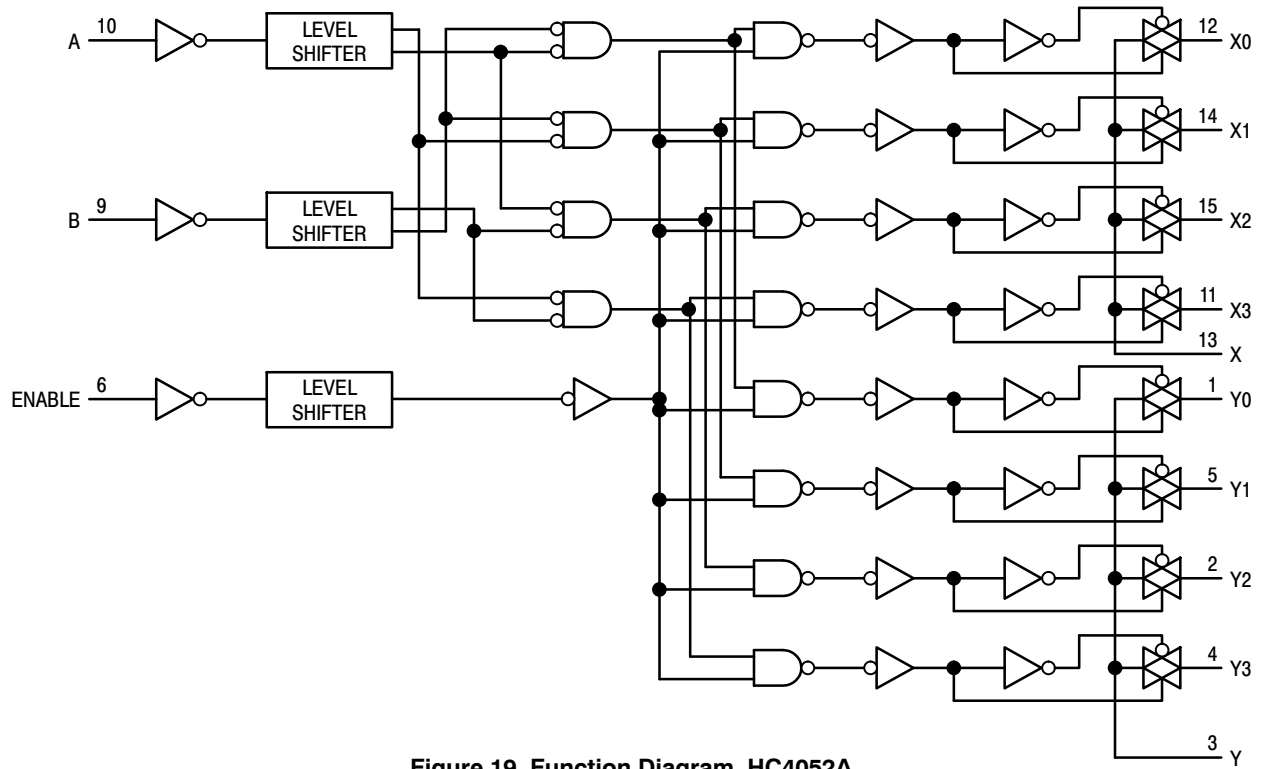


Figure 19. Function Diagram, HC4052A

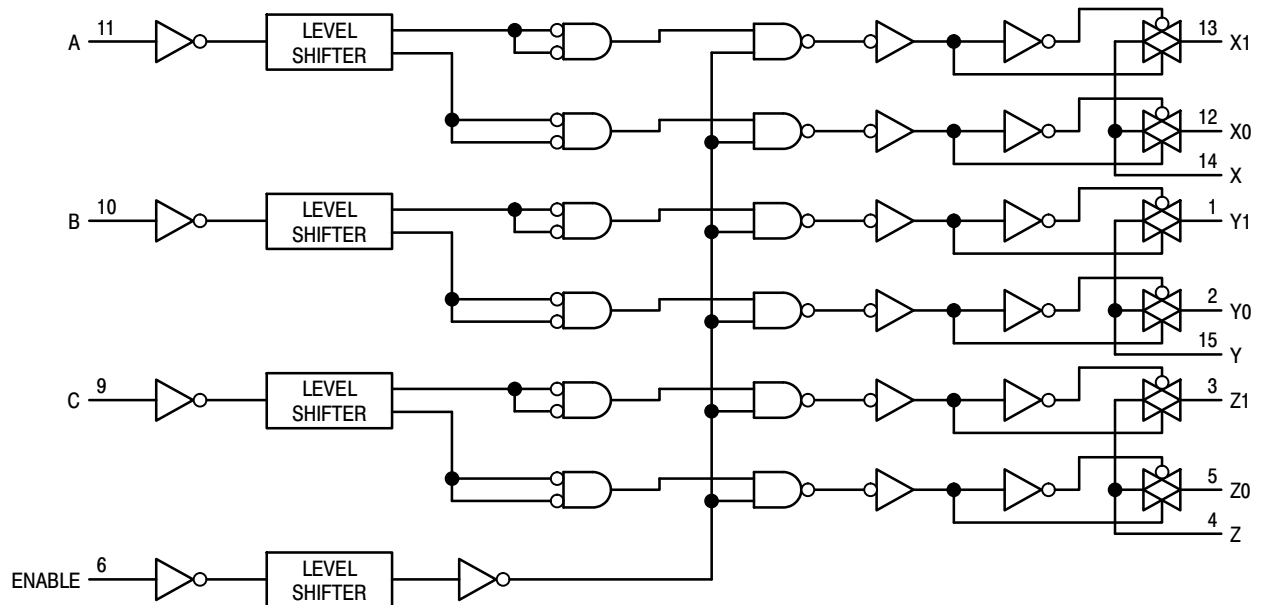


Figure 20. Function Diagram, HC4053A

MC74HC4051A, MC74HC4052A, MC74HC4053A

ORDERING INFORMATION

| Device | Package | Shipping† |
|--------------------------------------|---------------------------|--------------------------|
| MC74HC4051ADG | SOIC–16 (Pb–Free) | 48 Units / Rail |
| MC74HC4051ADR2G | | 2500 Units / Tape & Reel |
| NLV74HC4051ADR2G* | | 2500 Units / Tape & Reel |
| MC74HC4051AADR2G | | 2500 Units / Tape & Reel |
| NLV74HC4051AADR2G* | | 2500 Units / Tape & Reel |
| MC74HC4051ADWG | SOIC–16 WIDE (Pb–Free) | 48 Units / Rail |
| MC74HC4051ADWR2G | | 1000 Units / Tape & Reel |
| NLVHC4051ADWR2G* | | 1000 Units / Tape & Reel |
| MC74HC4051ADTG | TSSOP–16 (Pb–Free) | 96 Units / Rail |
| MC74HC4051ADTR2G | | 2500 Units / Tape & Reel |
| NLVHC4051ADTR2G* | | 2500 Units / Tape & Reel |
| NLVHC4051AADTR2G* | | 2500 Units / Tape & Reel |
| NLVHC4051AMNTWG* (In Development) | QFN16 (Pb–Free) | 3000 Units / Tape & Reel |

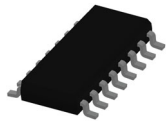
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|--------------------------------------|---------------------------|--------------------------|
| MC74HC4052ADG | SOIC–16 (Pb–Free) | 48 Units / Rail |
| MC74HC4052ADR2G | | 2500 Units / Tape & Reel |
| NLV74HC4052ADR2G* | | 2500 Units / Tape & Reel |
| MC74HC4052ADWG | SOIC–16 WIDE (Pb–Free) | 48 Units / Rail |
| MC74HC4052ADWR2G | | 1000 Units / Tape & Reel |
| MC74HC4052ADTG | TSSOP–16 (Pb–Free) | 96 Units / Rail |
| MC74HC4052ADTR2G | | 2500 Units / Tape & Reel |
| NLV74HC4052ADTRG* | | 2500 Units / Tape & Reel |
| NLVHC4052ADTR2G* | | 2500 Units / Tape & Reel |
| NLVHC4052AMNTWG* (In Development) | QFN16 (Pb–Free) | 3000 Units / Tape & Reel |

| | | |
|--------------------|---------------------------|--------------------------|
| MC74HC4053ADG | SOIC–16 (Pb–Free) | 48 Units / Rail |
| MC74HC4053ADR2G | | 2500 Units / Tape & Reel |
| NLV74HC4053ADR2G* | | 2500 Units / Tape & Reel |
| MC74HC4053ADWG | SOIC–16 WIDE (Pb–Free) | 48 Units / Rail |
| NLV74HC4053ADWRG* | | 1000 Units / Tape & Reel |
| MC74HC4053ADWR2G | | 1000 Units / Tape & Reel |
| NLV74HC4053ADWR2G* | | 1000 Units / Tape & Reel |
| MC74HC4053ADTG | TSSOP–16 (Pb–Free) | 96 Units / Rail |
| MC74HC4053ADTR2G | | 2500 Units / Tape & Reel |
| NLVHC4053ADTR2G* | | 2500 Units / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

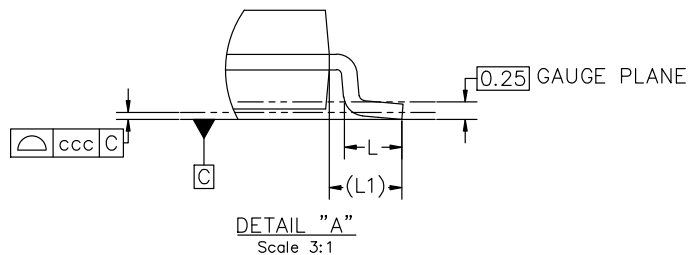
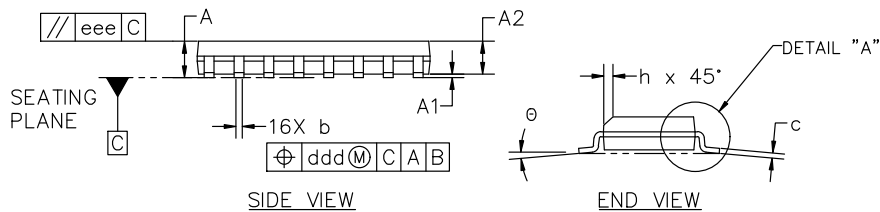
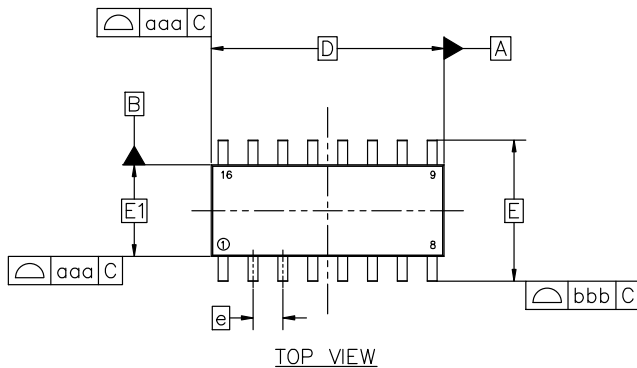


SOIC-16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

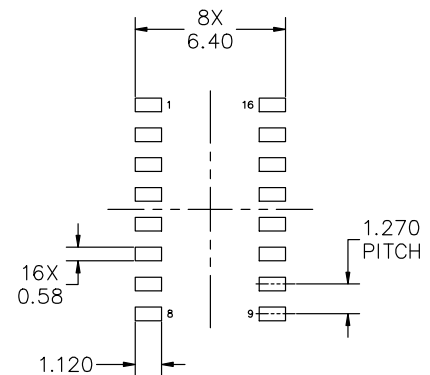
DATE 29 MAY 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



| MILLIMETERS | | | |
|--------------------------------|----------|------|------|
| DIM | MIN | NOM | MAX |
| A | 1.35 | 1.55 | 1.75 |
| A1 | 0.00 | 0.05 | 0.10 |
| A2 | 1.35 | 1.50 | 1.65 |
| b | 0.35 | 0.42 | 0.49 |
| c | 0.19 | 0.22 | 0.25 |
| D | 9.90 BSC | | |
| E | 6.00 BSC | | |
| E1 | 3.90 BSC | | |
| e | 1.27 BSC | | |
| h | 0.25 | --- | 0.50 |
| L | 0.40 | 0.83 | 1.25 |
| L1 | 1.05 REF | | |
| θ | 0° | --- | 7° |
| TOLERANCE OF FORM AND POSITION | | | |
| aaa | 0.10 | | |
| bbb | 0.20 | | |
| ccc | 0.10 | | |
| ddd | 0.25 | | |
| eee | 0.10 | | |



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D

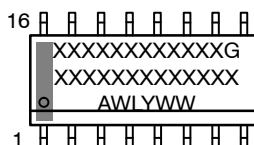
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SOIC-16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code

A = Assembly Location

WL = Wafer Lot

Y = Year

WW = Work Week

G = Pb-Free Package

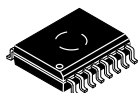
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

| | | | |
|--|--|--|--|
| STYLE 1: PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR 15. EMITTER 16. COLLECTOR | STYLE 2: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION 4. CATHODE 5. CATHODE 6. NO CONNECTION 7. ANODE 8. CATHODE 9. CATHODE 10. ANODE 11. NO CONNECTION 12. CATHODE 13. CATHODE 14. NO CONNECTION 15. ANODE 16. CATHODE | STYLE 3: PIN 1. COLLECTOR, DYE #1 2. BASE, #1 3. EMITTER, #1 4. COLLECTOR, #1 5. COLLECTOR, #2 6. BASE, #2 7. EMITTER, #2 8. COLLECTOR, #2 9. COLLECTOR, #3 10. BASE, #3 11. EMITTER, #3 12. COLLECTOR, #3 13. COLLECTOR, #4 14. BASE, #4 15. EMITTER, #4 16. COLLECTOR, #4 | STYLE 4: PIN 1. COLLECTOR, DYE #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. COLLECTOR, #3 6. COLLECTOR, #3 7. COLLECTOR, #4 8. COLLECTOR, #4 9. BASE, #4 10. EMITTER, #4 11. BASE, #3 12. EMITTER, #3 13. BASE, #2 14. EMITTER, #2 15. BASE, #1 16. EMITTER, #1 |
| STYLE 5: PIN 1. DRAIN, DYE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. DRAIN, #3 6. DRAIN, #3 7. DRAIN, #4 8. DRAIN, #4 9. GATE, #4 10. SOURCE, #4 11. GATE, #3 12. SOURCE, #3 13. GATE, #2 14. SOURCE, #2 15. GATE, #1 16. SOURCE, #1 | STYLE 6: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. CATHODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE 15. ANODE 16. ANODE | STYLE 7: PIN 1. SOURCE N-CH 2. COMMON DRAIN (OUTPUT) 3. COMMON DRAIN (OUTPUT) 4. GATE P-CH 5. COMMON DRAIN (OUTPUT) 6. COMMON DRAIN (OUTPUT) 7. COMMON DRAIN (OUTPUT) 8. SOURCE P-CH 9. SOURCE P-CH 10. COMMON DRAIN (OUTPUT) 11. COMMON DRAIN (OUTPUT) 12. COMMON DRAIN (OUTPUT) 13. GATE N-CH 14. COMMON DRAIN (OUTPUT) 15. COMMON DRAIN (OUTPUT) 16. SOURCE N-CH | |

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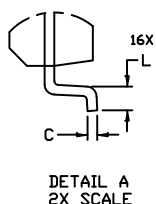
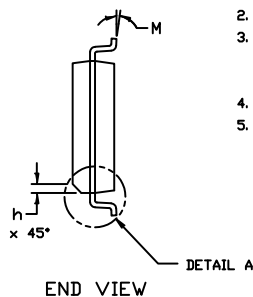
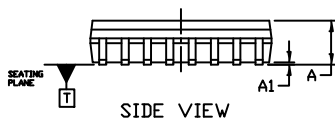
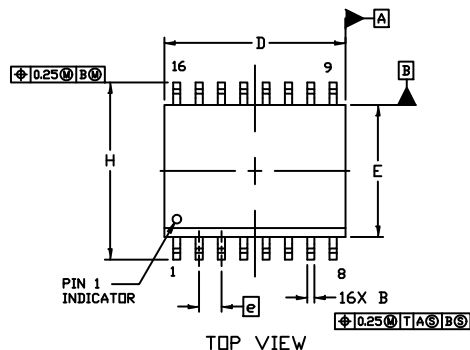
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



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SCALE 1:1

SOIC-16 WB CASE 751G ISSUE E

DATE 08 OCT 2021

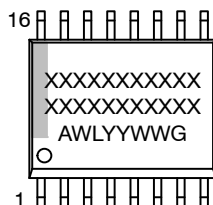


NOTES:

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2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

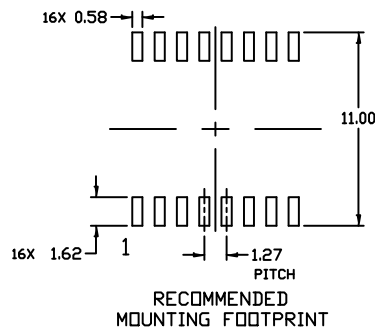
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|-----|-------------|-------|
| | MIN. | MAX. |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 10.15 | 10.45 |
| E | 7.40 | 7.60 |
| e | 1.27 | BSC |
| H | 10.05 | 10.55 |
| h | 0.53 | REF |
| L | 0.50 | 0.90 |
| M | 0° | 7° |

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

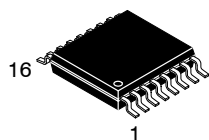
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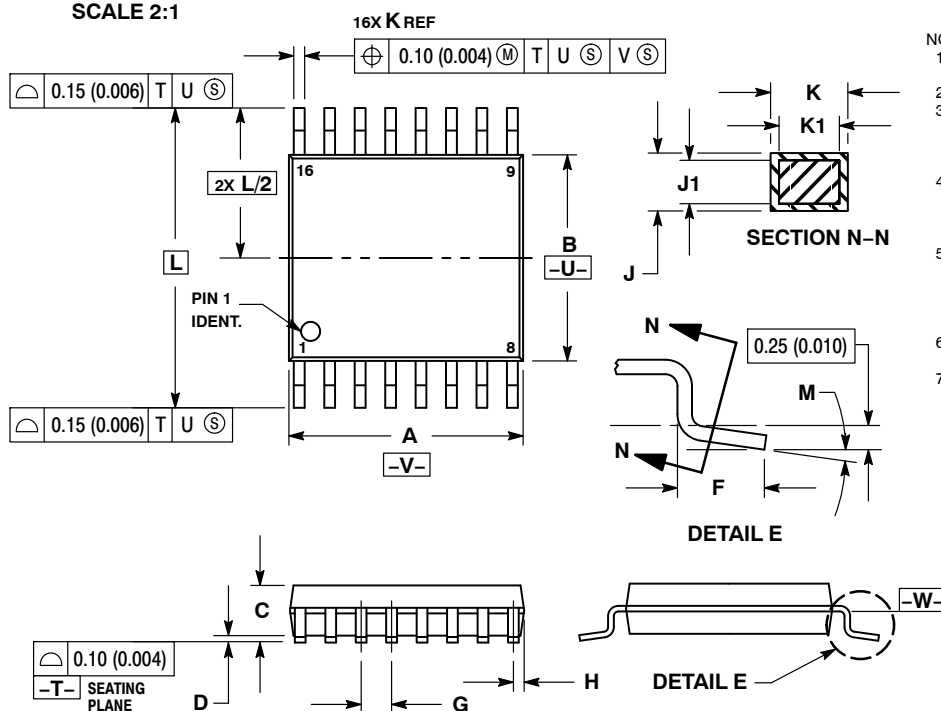
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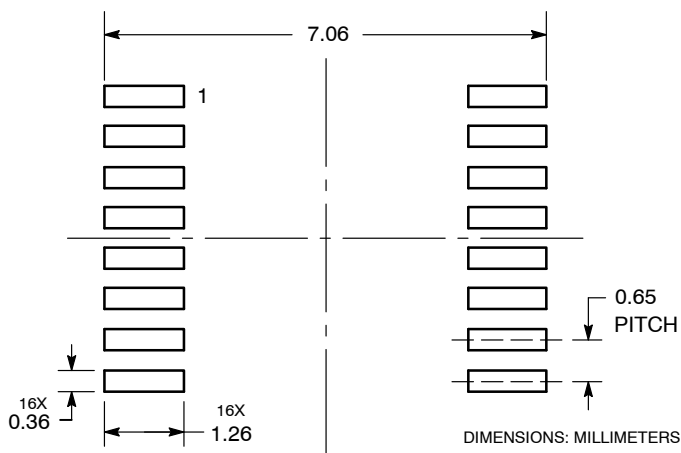


TSSOP-16 WB
CASE 948F
ISSUE B

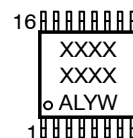
DATE 19 OCT 2006



RECOMMENDED SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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