# NLAS7213

# High-Speed USB 2.0 (480 Mbps) DPST Switch

The NLAS7213 is a DPST switch optimized for high−speed USB 2.0 applications within portable systems. It features ultra−low off capacitance, $C_{OFF}$ = 3.0 pF (typ), and a bandwidth above 1118 MHz. It is optimized for applications that use a single USB interface connector to route multiple signal types. The $C_{ON}$ and $R_{ON}$ of both switches are suitably low to allow the NLAS7213 to pass any speed USB data or audio signals going to a moderately resistive terminal such as an external headset.

The NLAS7213 is protected on all pins with 8 kV Human Body Model ESD protection. It is offered in a 1.5 x 1.5 mm UQFN8 package.

### Features

- $R_{ON}$: 8.5 Ω Max @ $V_{CC}$ = 3.3 V
- $C_{OFF}$: 3.0 pF Typ @ $V_{CC}$ = 3.3 V
- $V_{CC}$ Operating Range: 1.65 V to 4.5 V
- > 1118 MHz Bandwidth
- OVT up to 5.25 V on D+/D− Pins
- 1.5 x 1.5 x 0.55 mm UQFN8
- 8 kV ESD Protection on All Pins
- This is a Pb−Free Device

### Typical Applications

- High Speed USB 2.0 Data
- Mobile Phones
- Portable Devices

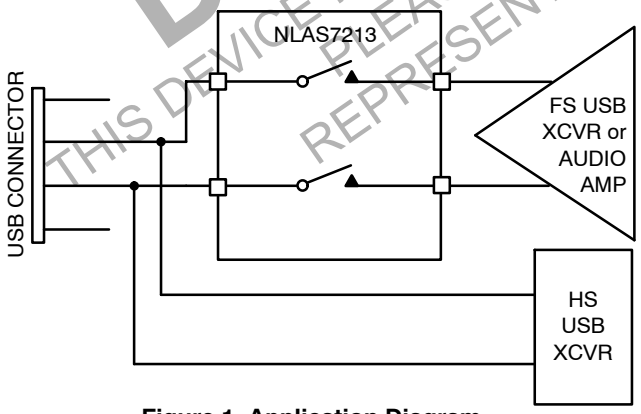


**Figure 1. Application Diagram**

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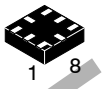
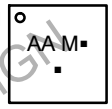
**MARKING DIAGRAM**



**UQFN8**
**(1.5 x 1.5 mm)**
**CASE 523AH**




AA = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

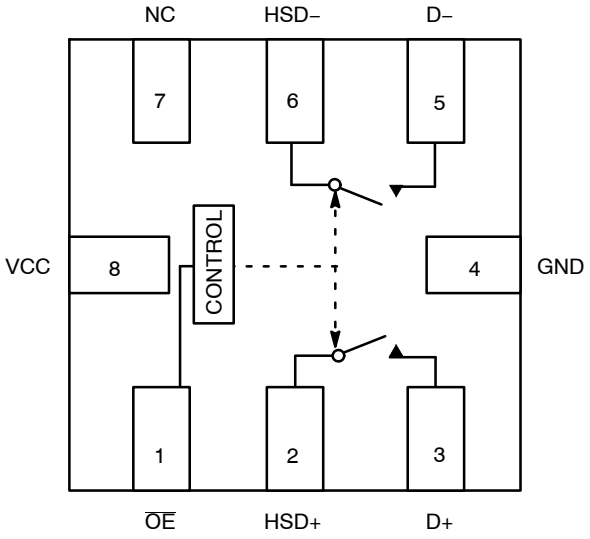



**Figure 2. Pin Connections and Logic Diagram**
(Top View)

**Table 1. PIN DESCRIPTION**

| Pin | Function |
|---|---|
| $\overline{OE}$ | Control Input Select Line |
| HSD+, HSD−, D+, D− | Data Ports |

**Table 2. TRUTH TABLE**

| $\overline{OE}$ | Both Switches |
|---|---|
| 1 | OPEN |
| 0 | CLOSED |



## MAXIMUM RATINGS

| Symbol | Pins | Parameter | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | $V_{CC}$ | Positive DC Supply Voltage | −0.5 to +4.6 | V |
| $V_{IS}$ | HSD+, HSD− | Analog Signal Voltage | −0.5 to $V_{CC}$ + 0.3 | V |
| | D+, D− | | −0.5 to +5.25 | |
| $V_{IN}$ | $\overline{OE}$ | Control Input Voltage | −0.5 to +4.6 | V |
| $I_{CC}$ | $V_{CC}$ | Positive DC Supply Current | 50 | mA |
| $T_S$ | | Storage Temperature | −65 to +150 | °C |
| $I_{IS\_CON}$ | HSD+, HSD−, D+, D− | Analog Signal Continuous Current−Closed Switch | ±300 | mA |
| $I_{IS\_PK}$ | HSD+, HSD−, D+, D− | Analog Signal Continuous Current 10% Duty Cycle | ±500 | mA |
| $I_{IN}$ | $\overline{OE}$ | Control Input Current | ±20 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Pins | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | | Positive DC Supply Voltage | 1.65 | 4.5 | V |
| $V_{IS}$ | HSD+, HSD− | Analog Signal Voltage | GND | $V_{CC}$ | V |
| | D+, D− | | GND | 4.5 | |
| $V_{IN}$ | $\overline{OE}$ | Digital Select Input Voltage | GND | $V_{CC}$ | V |
| $T_A$ | | Operating Temperature Range | −40 | +85 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## ESD PROTECTION

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| ESD | Human Body Model − All Pins | 8.0 | kV |

## DC ELECTRICAL CHARACTERISTICS

**CONTROL INPUT** (Typical: T = 25°C, $V_{CC}$ = 3.3 V)

| Symbol | Pins | Parameter | Test Conditions | $V_{CC}$ (V) | –40°C to +85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $V_{IH}$ | $\overline{OE}$ | Control Input HIGH Voltage | | 2.7<br>3.3<br>4.2 | 1.3<br>1.3<br>1.4 | – | – | V |
| $V_{IL}$ | $\overline{OE}$ | Control Input LOW Voltage | | 2.7<br>3.3<br>4.2 | – | – | 0.4<br>0.4<br>0.4 | V |
| $I_{IN}$ | $\overline{OE}$ | Control Input Leakage Current | $V_{IS}$ = GND | 1.65 – 4.5 | – | – | ±1.0 | μA |

**SUPPLY CURRENT AND LEAKAGE** (Typical: T = 25°C, $V_{CC}$ = 3.3 V, $V_{IN}$ = $V_{CC}$ or GND)

| Symbol | Pins | Parameter | Test Conditions | $V_{CC}$ (V) | –40°C to +85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $I_{CC}$ | $V_{CC}$ | Quiescent Supply Current | $V_{IS}$ = $V_{CC}$ or GND; $I_D$ = 0 A | 1.65 – 4.5 | – | – | 1.0 | μA |
| $I_{NC(OFF)}$ | HSD+,<br>HSD– | OFF State Leakage Current | $V_{COM}$ = 3.6 V, $V_{NC}$ = 1.0 V | 1.65 – 4.5 | – | – | ±1.0 | μA |
| $I_{OFF}$ | | Power OFF Leakage Current | $V_{IS}$ = GND | 0 | – | – | ±1.0 | μA |

**ON RESISTANCE** (Typical: T = 25°C, $V_{CC}$ = 3.3 V)

| Symbol | Pins | Parameter | Test Conditions | $V_{CC}$ (V) | –40°C to +85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $R_{ON}$ | | On–Resistance | $I_{ON}$ = –8 mA<br>$V_{IS}$ = 0 to 0.4 V | 2.7<br>3.3<br>4.2 | – | 9.0<br>8.0<br>7.2 | 9.5<br>8.5<br>7.5 | Ω |
| $R_{FLAT}$ | | On–Resistance Flatness | $I_{ON}$ = –8 mA<br>$V_{IS}$ = 0 to 0.4 V | 2.7<br>3.3<br>4.2 | – | 0.8<br>0.5<br>0.3 | – | Ω |
| $\Delta R_{ON}$ | | On–Resistance Matching | $I_{ON}$ = –8 mA<br>$V_{IS}$ = 0 to 0.4 V | 2.7<br>3.3<br>4.2 | – | 0.07<br>0.07<br>0.04 | – | Ω |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## AC ELECTRICAL CHARACTERISTICS

**TIMING/FREQUENCY** (Typical: T = 25°C, $V_{CC}$ = 3.3 V, $R_L$ = 50 Ω, $C_L$ = 35 pF, f = 1 MHz)

| Symbol | Pins | Parameter | Test Conditions | $V_{CC}$ (V) | −40°C to +85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $t_{ON}$ | | Turn−ON Time (Figures 6, 7) | | 1.65 – 4.5 | – | 13.0 | 30.0 | ns |
| $t_{OFF}$ | | Turn−OFF Time (Figures 6, 7) | | 1.65 – 4.5 | – | 12.0 | 25.0 | ns |
| $t_{PD}$ | | Propagation Delay | | 1.65 – 4.5 | – | 0.25 | – | ns |
| BW | | −3 dB Bandwidth | $C_L$ = 5 pF | 1.65 – 4.5 | – | 1118 | – | MHz |

**ISOLATION** (Typical: T = 25°C, $V_{CC}$ = 3.3 V, $R_L$ = 50 Ω, $C_L$ = 5 pF)

| Symbol | Pins | Parameter | Test Conditions | −40°C to +85°C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $O_{IRR}$ | Open | OFF−Isolation | f = 240 MHz | – | −20 | – | dB |
| $X_{TALK}$ | HSD+, HSD− | Non−Adjacent Channel Crosstalk | f = 240 MHz | – | −30 | – | dB |

**CAPACITANCE** (Typical: T = 25°C, $V_{CC}$ = 3.3 V, f = 1 MHz)

| Symbol | Pins | Parameter | Test Conditions | −40°C to +85°C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $C_{IN}$ | $\overline{OE}$ | Control Pin Input Capacitance | $V_{IS}$ = 3.3 $V_{p-p}$, $V_{CC}$ = 0 V | – | 2.0 | – | pF |
| $C_{ON}$ | I/O to GND | ON Capacitance | $V_{IS}$ = 3.3 $V_{p-p}$, $\overline{OE}$ = 0 V | – | 3.0 | – | pF |
| $C_{OFF}$ | I/O to GND | OFF Capacitance | $V_{IS}$ = 3.3 $V_{p-p}$, $\overline{OE}$ = 3.3 V | – | 3.0 | – | pF |

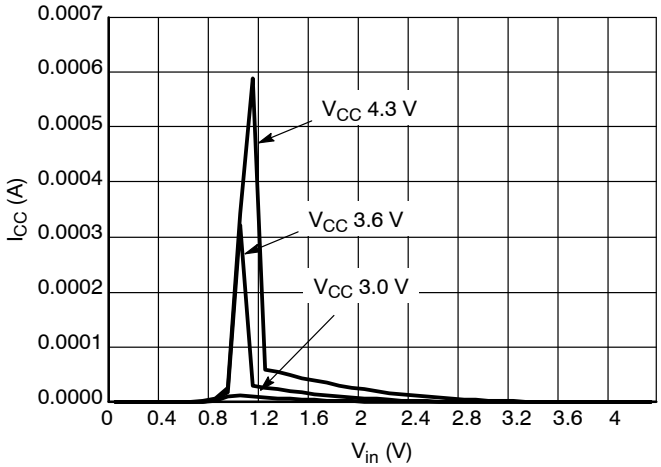



**Figure 3. $I_{CC}$ vs. $V_{in}$**

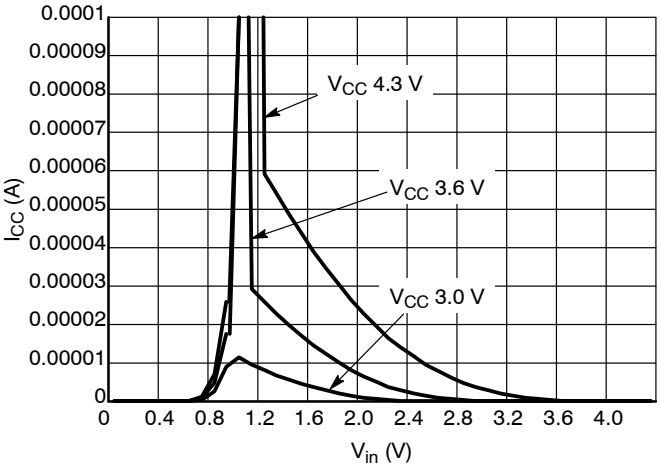
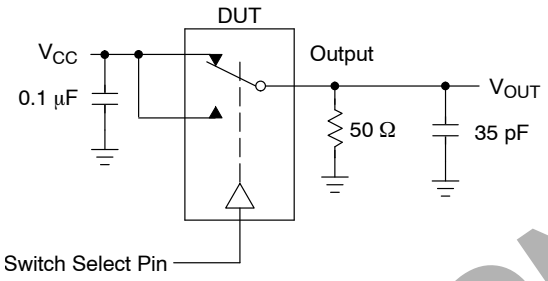



**Figure 4. $I_{CC}$ vs. $V_{in}$**



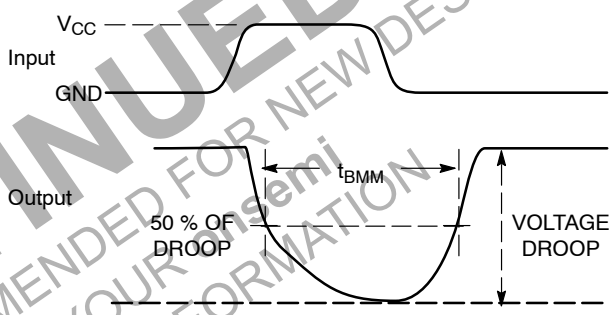
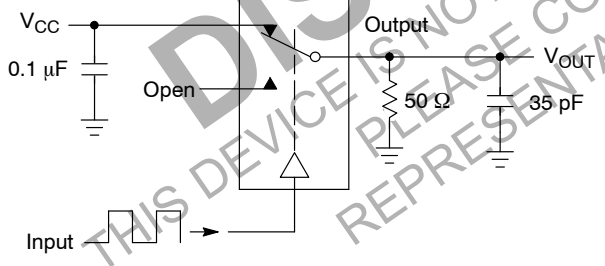




**Figure 5. $t_{BBM}$ (Time Break−Before−Make)**



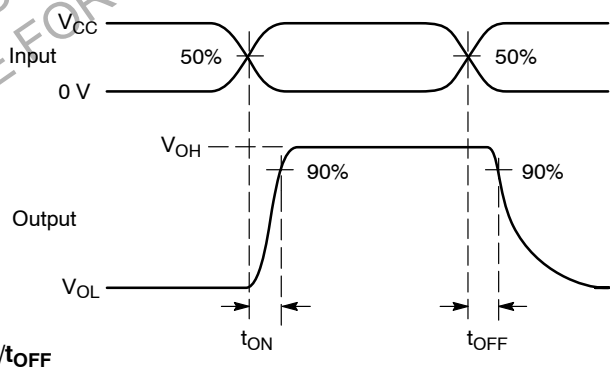
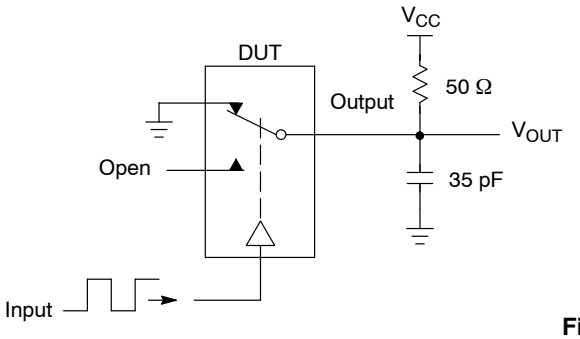




**Figure 6. $t_{ON}/t_{OFF}$**



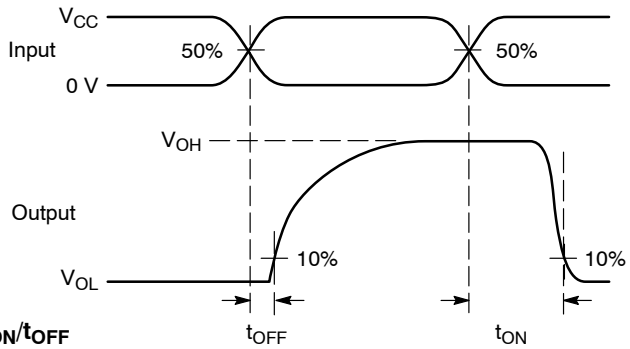
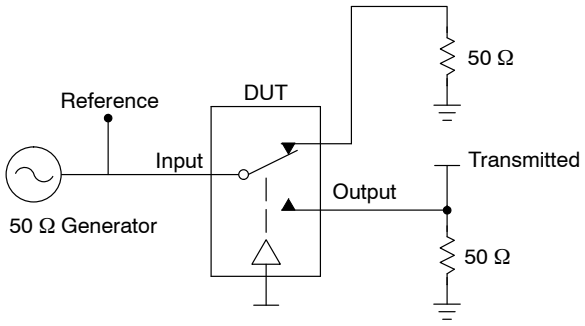




**Figure 7. $t_{ON}/t_{OFF}$**




Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. $V_{ISO}$, Bandwidth and $V_{ONL}$ are independent of the input signal direction.

$V_{ISO}$ = Off Channel Isolation = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for $V_{IN}$ at 100 kHz

$V_{ONL}$ = On Channel Loss = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for $V_{IN}$ at 100 kHz to 50 MHz

Bandwidth (BW) = the frequency 3 dB below $V_{ONL}$
$V_{CT}$ = Use $V_{ISO}$ setup and test to all other switch analog input/outputs terminated with 50 Ω

**Figure 8. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/$V_{ONL}$**

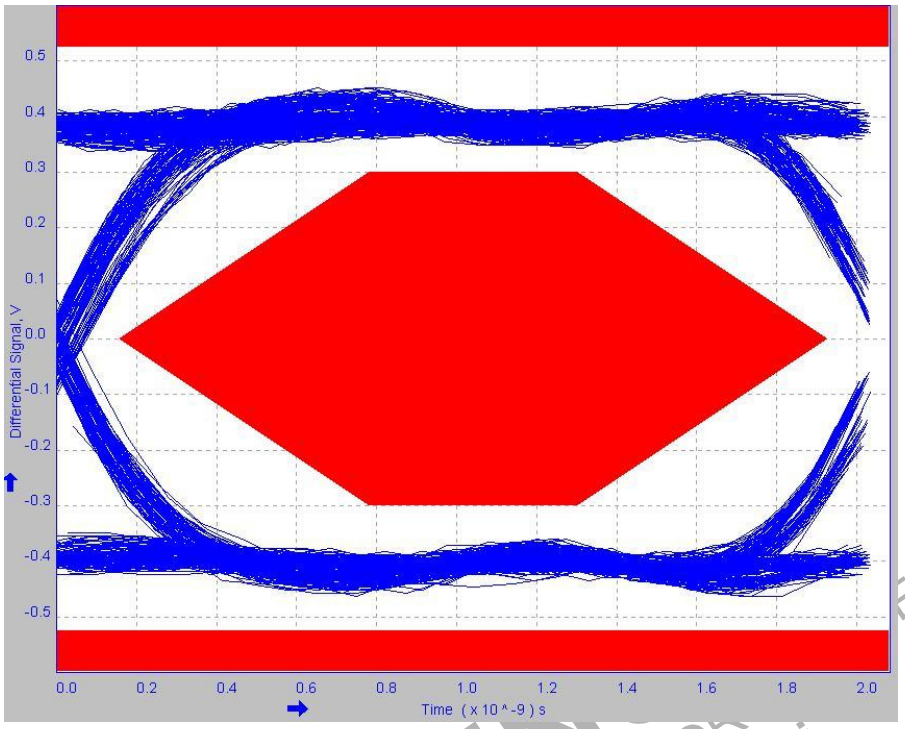



**Figure 9. Signal Quality**

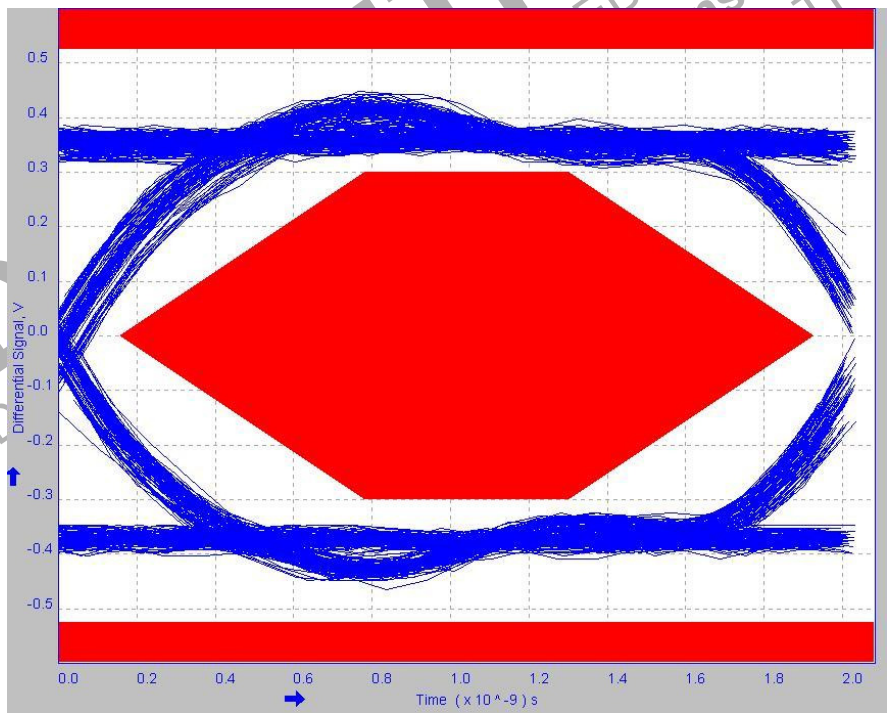



**Figure 10. Near End Eye Diagram**

| Near End Test Data | | | | | Min | Max |
|---|---|---|---|---|---|---|
| Std. | Consecutive Jitter Range | −44.80 | 76.30 | ps | −200 ps | +200 ps |
| | Paired JK Jitter Range | −63.59 | 56.33 | ps | | |
| | Paired KJ Jitter Range | −44.15 | 45.68 | ps | | |
| NO | Consecutive Jitter Range | −58.40 | 90.58 | ps | −200 ps | +200 ps |
| | Paired JK Jitter Range | −65.90 | 70.64 | ps | | |
| | Paired KJ Jitter Range | −52.43 | 55.14 | ps | | |

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NLAS7213MUTBG | UQFN8<br>(Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

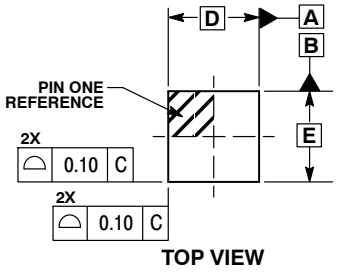
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

ON Semiconductor®

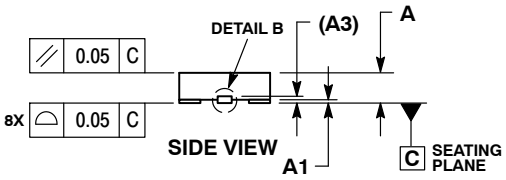
**UQFN8, 1.5x1.5, 0.5P**
CASE 523AH−01
ISSUE O

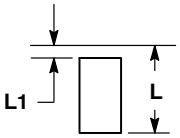
DATE 08 NOV 2007


**SCALE 4:1**

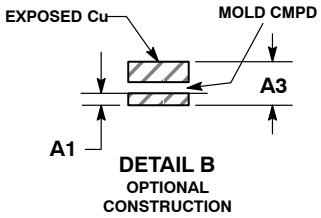



**TOP VIEW**

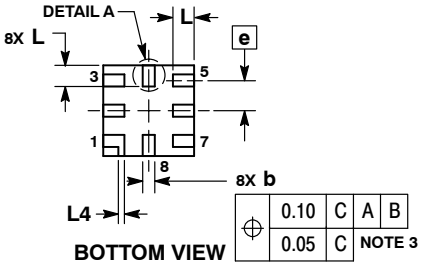



**DETAIL A**
**OPTIONAL CONSTRUCTION**




**DETAIL B**
**OPTIONAL CONSTRUCTION**

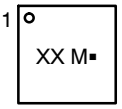



**BOTTOM VIEW**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A3 | 0.13 REF | |
| b | 0.15 | 0.25 |
| D | 1.50 BSC | |
| E | 1.50 BSC | |
| e | 0.50 BSC | |
| L | 0.30 | 0.40 |
| L1 | 0.00 | 0.03 |
| L4 | 0.10 REF | |

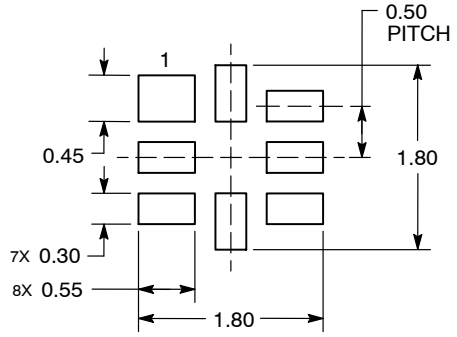
### GENERIC MARKING DIAGRAM*




XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

### SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON25688D** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **8 PIN UQFN, 1.5X1.5, 0.5P** | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales