

XIO2000A Implementation Guide

Interface Business Unit

ABSTRACT

This document is provided to assist platform designers using the XIO2000A PCI Express to PCI Translation Bridge. Detailed information can be found in the XIO2000A Data Manual. However, this document provides board design suggestions for the various device features when designing in the XIO2000A.

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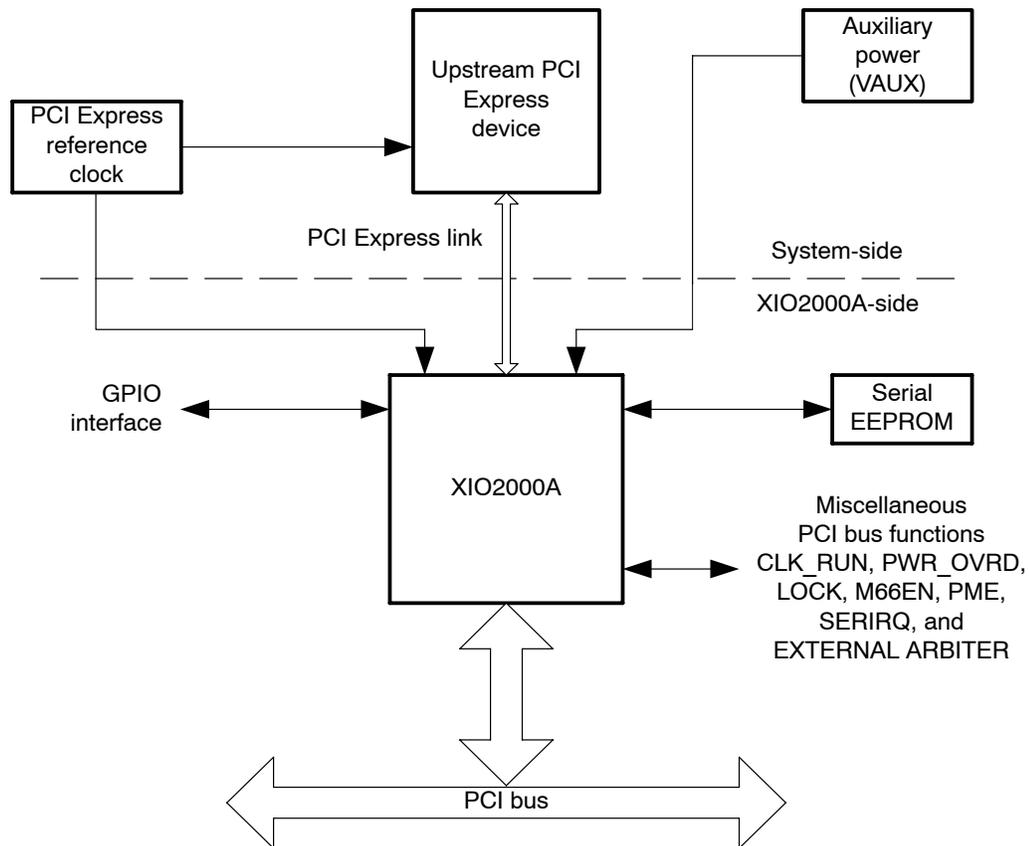
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1 XIO2000A Typical System Implementation

Figure 1 represents a typical implementation of the XIO2000A PCI Express to PCI translation bridge. The device serves as a bridge between an upstream PCI Express device and up to six downstream PCI bus devices. The XIO2000A operates only with the PCI Express interface as the primary bus and the PCI bus interface as the secondary bus. The PCI bus interface is 32 bits wide and operates at either 33 MHz or 66 MHz.

Figure 1. Typical System Integration



Either a common differential 100-MHz PCI Express reference clock or an asynchronous single-ended 125-MHz reference clock is supported. Figure 1 illustrates the common 100-MHz reference clock option.

If V_{AUX} power states are a system requirement, the XIO2000A maintains system configuration information in “sticky” register bits.

The EEPROM can set various configuration registers but is not necessary if those registers are settable via software/BIOS for the system.

The serial IRQ bus passes ISA-style legacy interrupts upstream to the system host controller. Some PCI devices require ISA-style legacy interrupts to function properly. The XIO2000A converts serial bus IRQs into PCI Express upstream MSI messages.

Up to eight general-purpose inputs/outputs (GPIOs) exist for further system customization. Options exist for the clock run, LOCK, PME, M66 enable, external arbiter, and power override features, if any of the PCI bus devices require these features.

2 Power Considerations

2.1 1.5-V and 3.3-V Digital Supplies

The XIO2000A requires both 1.5-V and 3.3-V digital power.

The 1.5-V terminals are named V_{DD_15} . These terminals supply power to the digital core. The 1.5-V core allows for a significant reduction in both power consumption and logic switching noise.

The 3.3-V terminals are named V_{DD_33} and supply power to most of the input and output cells.

Both the V_{DD_15} and V_{DD_33} supplies must have 0.1- μ F bypass capacitors to V_{SS} (ground) for proper operation. The recommendation is one capacitor for each power terminal.

The via associated with the H14 terminal pad must connect to a 1000-pF bypass capacitor. The other side of the capacitor must connect to V_{SS} (ground) for proper operation. When placing and connecting all bypass capacitors, high-speed board design rules must be followed.

2.2 1.5-V and 3.3-V Analog Supplies

Both 1.5-V and 3.3-V analog power is required by the XIO2000A. Because circuit noise on the analog power terminals must be minimized, a Pi filter is recommended. All V_{DDA_15} terminals must be connected together and share one Pi filter. All V_{DDA_33} terminals must be connected together and share a second Pi filter.

Both the 1.5-V and 3.3-V analog supplies must have 0.1- μ F bypass capacitors connected to V_{SSA} (ground) in order for proper operation. The recommendation is one capacitor for each power terminal. In addition, one 1000-pF capacitor per Pi filter is recommended. This 1000-pF capacitor is attached to the device side of the Pi filter and to V_{SSA} (ground). High-speed board design rules must be followed when connecting bypass capacitors to V_{DDA} and V_{SSA} .

2.3 V_{CCP} Clamping Rail

The XIO2000A has a PCI bus I/O clamp rail (V_{CCP}) which can be either 3.3 V or 5 V depending on the system implementation. For 33-MHz PCI bus implementations, V_{CCP} may be connected to either 3.3 V or 5.0 V. For 66-MHz PCI bus implementations, a 3.3-V connection is the only approved configuration. The power source for this clamp rail is a standard digital supply. Other than digital supply bypass capacitors, one 0.1- μ F capacitor per terminal, no additional components are required.

If V_{CCP} is attached to a 5.0-V supply, the XIO2000A will only output 3.3-V amplitude signals on the PCI bus. The received PCI bus signal amplitudes may be either 3.3 V or 5.0 V. The PCI bus I/O cells are 5.0-V tolerant and the XIO2000A device is not damaged by 5.0-V input signal amplitudes.

2.4 Combined Power Outputs

To support V_{AUX} system requirements, the XIO2000A internally combines main power with V_{AUX} power. There are three combined power rails in the XIO2000A. These three power rails are distributed to the analog circuits, digital logic, and I/O cells that must operate during the V_{AUX} state. Each of the three power rails has an output terminal for the external attachment of bypass capacitors to minimize circuit switching noise. These terminals are named $V_{DD_15_COMB}$, $V_{DD_33_COMB}$, and $V_{DD_33_COMBIO}$.

The recommended bypass capacitors for each combined output terminal are 1000 pF, 0.01 μ F, and 1.0 μ F. When placing these capacitors on the bottom side of the circuit board, the smallest capacitor is positioned next to the via associated with the combined output terminal and the largest capacitor is the most distant from the via. The circuit board trace width connecting the combined output terminal via to the capacitors must be at least 12 to 15 mils wide with the trace length as short as possible.

Other than the three recommended capacitors, no external components or devices must be attached to these combined output terminals.

2.5 Auxiliary Power

If V_{AUX} power is available in the system, the XIO2000A has the $V_{DD_33_AUX}$ terminal to support this feature. Without fully understanding a system's V_{AUX} power distribution design, recommending external components for the XIO2000A is difficult. At a minimum, a 0.1- μ F bypass capacitor is placed near the XIO2000A and attached to the system's V_{AUX} power supply. A robust design may include a Pi filter with bulk capacitors (5 μ F to 100 μ F) to minimize voltage fluctuations. When the system is cycling main power or is in the V_{AUX} state, the $V_{DD_33_AUX}$ terminal requirements are that the input voltage cannot exceed 3.6 V or drop below 3.0 V for proper operation of the bridge.

If V_{AUX} power is not present within the system, this terminal is connected to V_{SS} thru a resistor with a value greater than 3.0 k Ω .

2.6 V_{SS} and V_{SSA} Terminals

For proper operation of the XIO2000A, we recommend a unified V_{SS} and V_{SSA} ground plane. The circuit board stack-up recommendation is to implement a layer 2 ground plane directly under the XIO2000A device. Both the circuit board vias and ground trace widths that connect the V_{SS} and V_{SSA} ball pads to this ground plane must be oversized to provide a low impedance connection.

2.7 Capacitor Selection Recommendations

When selecting bypass capacitors for the XIO2000A device, X7R-type capacitors are recommended. The frequency versus impedance curves, quality, stability, and cost of these capacitors make them a logical choice for most computer systems.

The selection of bulk capacitors with low-ESR specifications is recommended to minimize low-frequency power supply noise. Today, the best low-ESR bulk capacitors are radial leaded aluminum electrolytic capacitors. These capacitors typically have ESR specifications that are less than 0.01 Ω at 100 kHz. Also, several manufacturers sell D size surface mount specialty polymer solid aluminum electrolytic capacitors with ESR specifications slightly higher than 0.01 Ω at 100 kHz. Both of these bulk capacitor options significantly reduce low-frequency power supply noise and ripple.

2.8 Power-Up/Down Sequencing

NOTE: The power sequencing recommendations in this section exclude the $V_{DD_33_AUX}$ terminal.

All XIO2000A analog and digital power terminals must be controlled during the power-up and power-down sequence. Absolute maximum power terminal ratings must not be exceeded to prevent damaging the device. All power terminals must remain within 3.6 V to prevent damaging the XIO2000A.

2.9 Power Supply Filtering Recommendations

To meet the PCI-Express jitter specifications, low-noise power supplies are required on several of the XIO2000A voltage terminals. The power terminals that require low-noise power include V_{DDA_15} and V_{DDA_33} . This section provides guidelines for the filter design to create low-noise power sources.

The least expensive solution for low-noise power sources is to filter existing 3.3-V and 1.5-V power supplies. This solution requires analysis of the noise frequencies present on the power supplies. The XIO2000A has external interfaces operating at clock rates of 33 MHz, 66 MHz, 100 MHz, 125 MHz, and 2.5 GHz. Other devices near the XIO2000A may produce switching noise at different frequencies. Also, the power supplies that generate the 3.3-V and 1.5-V power rails may add low frequency ripple noise. Linear regulators have feedback loops that typically operate in the 100-kHz range. Switching power supplies typically have operating frequencies in the 500-kHz range. When analyzing power supply noise frequencies, the first, third, and fifth harmonic of every clock source should be considered.

Critical analog circuits within the XIO2000A must be shielded from this power supply noise. The fundamental requirement for a filter design is to reduce power supply noise to a peak-to-peak amplitude of less than 25 millivolts. This maximum noise amplitude must apply to all frequencies from 0 Hz to 12.5 GHz.

The following information should be considered when designing a power supply filter:

- Ideally, the series resonance frequency for each filter component should be greater than the fifth harmonic of the maximum clock frequency. With a maximum clock frequency of 1.25 GHz, the third harmonic is 3.75 GHz and the fifth harmonic is 6.25 GHz. Finding inductors and capacitors with a series resonance frequency above 6.25 GHz is both difficult and expensive. Components with a series resonance frequency in the 4- to 6-GHz range are a good compromise.
- The inductor(s) associated with the filter must have a dc resistance low enough to pass the required current for the connected power terminals. The voltage drop across the inductor must be low enough to meet the minus 10 percent voltage margin requirement associated with each XIO2000A power terminal. Power supply output voltage variation must be considered as well as voltage drops associated with any connector pins and circuit board power distribution geometries.
- The Q versus frequency curve associated with the inductor must be appropriate to reduce power terminal noise to less than the maximum peak-to-peak amplitude requirement for the XIO2000A. Recommending a specific inductor is difficult because every system design is different; therefore, the noise frequencies and noise amplitudes are different. Many factors will influence the inductor selection for the filter design. Power supplies must have adequate input and output filtering. A sufficient number of bulk and bypass capacitors are required to minimize switching noise. Assuming that board level power is properly filtered and minimal low frequency noise is present, frequencies less than 10 MHz, an inductor with a Q greater than 20 from approximately 10 MHz to 3 GHz should be adequate for most system applications.

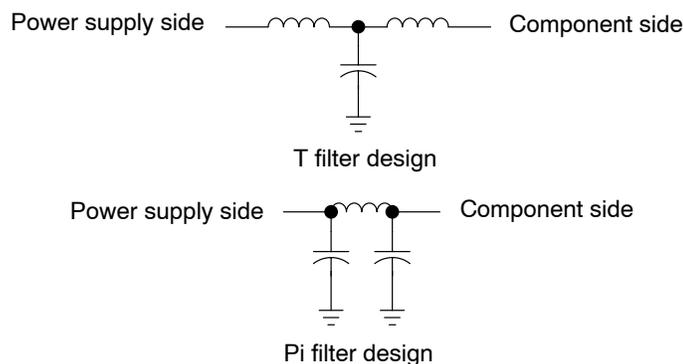
- The series component(s) in the filter may either be an inductor or a ferrite bead. Testing has been performed on both component types. When measuring PCI-Express link jitter, the inductor or ferrite bead solutions produce equal results. When measuring circuit board EMI, the ferrite bead is a superior solution.

NOTE: The XIO2200A reference schematics include ferrite beads in the analog power supply filters.

- When designing filters associated with power distribution, the power supply is a low-impedance source and the device power terminals are a low impedance load. The best filter for this application is a T filter. Please see Figure 2 for a T filter circuit. Some system may require this type of filter design if the power supplies or nearby components are exceptionally noisy. This type of filter design is recommended if a significant amount of low frequency noise, frequencies less than 10 MHz, is present in a system.
- For most applications a Pi filter will be adequate. See Figure 2 for a Pi filter circuit. When implementing a Pi filter, the two capacitors and the inductor must be next to each other on the circuit board and must be connected together with wide low impedance traces. Capacitor ground connections must be short and low impedance.
- If a significant amount of high frequency noise, frequencies greater than 300 MHz, is present in a system, creating an internal circuit board capacitor will help reduce this noise. This is accomplished by locating power and ground planes next to each other in the circuit board stack-up. A gap of 0.003 mils between the power and ground planes will significantly reduce this high frequency noise.
- Another option for filtering high-frequency logic noise is to create an internal board capacitor using signal layer copper plates. When a component requires a low-noise power supply, usually the Pi filter is located near the component. Directly under the Pi filter, a plate capacitor may be created. In the circuit board stack-up, select a signal layer that is physically next to a ground plane. Then, generate an internal 0.25 inch by 0.25 inch plate on that signal layer. Assuming a 0.006-mil gap between the signal layer plate and the internal ground plane, this generates a 12-pF capacitor. By connecting this plate capacitor to the trace between the Pi filter and the component's power terminals, an internal circuit board high frequency bypass capacitor is created. This solution is extremely effective for switching frequencies above 300 MHz.

Figure 2 illustrates two different filter designs that may be used with the XIO2000A to provide low-noise power to critical power terminals.

Figure 2. Filter Design



3 PCI Express Interface Considerations

The XIO2000A has an x1 PCI Express interface that is fully compliant to the *PCI Express Base Specification*, Revision 1.0a. The remainder of this section describes implementation considerations for the XIO2000A primary PCI Express interface.

3.1 2.5-Gb/s Transmit and Receive Links

The XIO2000A TX and RX terminals attach to the upstream PCI Express device over a 2.5-Gb/s high-speed differential transmit and receive PCI Express x1 Link. The connection details are provided in the following table.

XIO2000A Terminal Name	Upstream PCI Express Device Terminal Name	Comments
TXP (H17)	RXP	XIO2000A transmit positive differential terminal connects to the upstream device receive positive differential terminal.
TXN (H16)	RXN	XIO2000A transmit negative differential terminal connects to the upstream device receive negative differential terminal.
RXP (E17)	TXP	XIO2000A receive positive differential terminal connects to the upstream device transmit positive differential terminal.
RXN (E16)	TXN	XIO2000A receive negative differential terminal connects to the upstream device transmit negative differential terminal.

The XIO2000A TXP and TXN terminals comprise a low-voltage, 100- Ω differentially driven signal pair. The RXP and RXN terminals for the XIO2000A receive a low-voltage, 100- Ω differentially driven signal pair. The XIO2000A has integrated 50- Ω termination resistors to V_{SS} on both the RXP and RXN terminals eliminating the need for external components.

Each lane of the differential signal pair must be ac-coupled. The recommended value for the series capacitor is 0.1 μ F. To minimize stray capacitance associated with the series capacitor circuit board solder pads, 0402-sized capacitors are recommended.

When routing a 2.5-Gb/s low-voltage, 100- Ω differentially driven signal pair, the following circuit board design guidelines must be considered:

1. The PCI-Express drivers and receivers are designed to operate with adequate bit error rate margins over a 20-inch maximum length signal pair routed through FR4 circuit board material.
2. Each differential signal pair must be 100- Ω differential impedance with each single-ended lane measuring in the range of 50- Ω to 55- Ω impedance to ground.
3. The differential signal trace lengths associated with a PCI Express high-speed link must be length-matched to minimize signal jitter. This length-matching requirement applies only to the P and N signals within a differential pair. It is not necessary to length match the transmitter differential to the receiver differential pair. The absolute maximum trace length difference between the TXP signal and TXN signal must be less than 5 mils. This also applies to the RXP and RXN signal pair.
4. If a differential signal pair is broken into segments by vias, series capacitors, or connectors, the length of the positive signal trace must be length matched to the negative signal trace for each segment. Trace length differences over all segments are additive and must be less than 5 mils.

- The location of the series capacitors is critical. For add-in cards, the series capacitors are located between the TXP/TXN terminals and the PCI-Express connector. In addition, the capacitors are placed near the PCI Express connector. This translates to two capacitors on the motherboard for the downstream link and two capacitors on the add-in card for the upstream link. If both the upstream device and the downstream device reside on the same circuit board, the capacitors are near the TXP/TXN terminals for each link.
- The number of vias must be minimized. Each signal trace via reduces the maximum trace length by approximately 2 inches. For example, if 6 vias are needed, the maximum trace length is 8 inches.
- When routing a differential signal pair, 45-degree angles are preferred over 90-degree angles. Signal trace length matching is easier with 45-degree angles and overall signal trace length is reduced.
- The differential signal pairs must not be routed over gaps in the power planes or ground planes. This causes impedance mismatches.
- If vias are used to change from one signal layer to another signal layer, it is important to maintain the same 50- Ω impedance reference to the ground plane. Changing reference planes causes signal trace impedance mismatches. If changing reference planes cannot be prevented, bypass capacitors connecting the two reference planes next to the signal trace vias helps reduce the impedance mismatch.
- If possible, the differential signal pairs must be routed on the top and bottom layers of a circuit board. Signal propagation speeds are faster on external signal layers.

3.2 PCI Express Transmitter Reference Resistor

The REF0_PCIE (L16) and REF1_PCIE (L17) terminals connect to an external resistor to set the drive current for the PCI Express TX driver. The recommended resistor value is 14,532 Ω with 1 percent tolerance.

A 14,532- Ω resistor is a custom value. To eliminate the need for a custom resistor, two series resistors are recommended: a 14,300- Ω , 1% resistor and a 232- Ω , 1% resistor. Trace lengths must be kept short to minimize noise coupling into the reference resistor terminals.

3.3 PCI-Express Reference Clock Inputs

The XIO2000A requires an external reference clock for the PCI-Express interface. The *PCI Express Base Specification* and *PCI Express Card Electromechanical Specification* provide information concerning the requirements for this reference clock. The XIO2000A is designed to meet all stated specifications when the reference clock input is within all PCI Express operating parameters. This includes both standard clock oscillator sources or spread spectrum clock oscillator sources.

The XIO2000A supports two options for the PCI Express reference clock: a 100-MHz common differential reference clock or a 125-MHz asynchronous single-ended reference clock. Both implementations are described in the following paragraphs.

The first option is a system-wide, 100-MHz differential reference clock. A single clock source with multiple differential clock outputs is connected to all PCI Express devices in the system. The differential connection between the clock source and each PCI Express device is point-to-point. This system implementation is referred to as a common clock design.

The XIO2000A is optimized for this type of system clock design. The REFCLK+ (C17) and REFCLK- (C16) terminals provide differential reference clock inputs to the XIO2000A. The circuit board routing rules associated with the 100-MHz differential reference clock are the same as the 2.5-Gb/s TX and RX link routing rules itemized in Section 3.1. The only difference is that the differential reference clock does not require series capacitors. The requirement is a dc connection from the clock driver output to the XIO2000A receiver input. Electrical specifications for these differential inputs are included in the XIO2000A Data Manual.

Terminating the differential clock signal is circuit board design specific. However, the XIO2000A design has no internal 50- Ω -to-ground termination resistors. Both REFCLK inputs, at approximately 20 k Ω to ground, are high-impedance inputs.

The second option is a 125-MHz asynchronous single-ended reference clock. In this case, the devices at each end of the PCI Express link have different clock sources. The XIO2000A has a 125-MHz single-ended reference clock option for asynchronous clocking designs. When the REFCLK_SEL input terminal (A16) is tied to V_{DD_33}, this clocking mode is enabled.

The single-ended reference clock is attached to the REFCLK+ (C17) terminal. The REFCLK+ input, at approximately 20 k Ω , is a high-impedance input. Any clock termination design must account for a high-impedance input. The REFCLK- (C16) terminal is attached to a 0.1- μ F capacitor. The capacitor's second terminal is connected to V_{SSA}. Electrical specifications for this single-ended input are included in the XIO2000A Data Manual.

When using a single-ended reference clock, care must be taken to ensure interoperability from a system jitter standpoint. The *PCI Express Base Specification* does not ensure interoperability when using a differential reference clock commonly used in PC applications along with a single-ended clock in a noncommon clock architecture. System jitter budgets must be verified to ensure interoperability. See the *PCI Express Jitter and BER White Paper* from the PCI-SIG.

3.4 PCI Express Reset

The XIO2000A PCI Express reset ($\overline{\text{PERST}}$) terminal (J17) connects to the upstream PCI Express device's $\overline{\text{PERST}}$ output. The J17 input cell has hysteresis and is operational during both the main power state and V_{AUX} power state. No external components are required.

See the XIO2000A Data Manual and the PCI-Express Card Electromechanical Specification to fully understand the $\overline{\text{PERST}}$ electrical requirements and timing requirements associated with power-up and power-down sequencing. Also, the Data Manual identifies all configuration and memory-mapped register bits that are reset by $\overline{\text{PERST}}$.

3.5 PCI Express Wake

$\overline{\text{WAKE}}$ is an open-drain output from the XIO2000A that is driven low to re-activate the PCI Express link hierarchy's main power rails and reference clocks. This PCI Express side-band signal is connected to the $\overline{\text{WAKE}}$ input on the upstream PCI Express device. $\overline{\text{WAKE}}$ is operational during both the main power state and V_{AUX} power state.

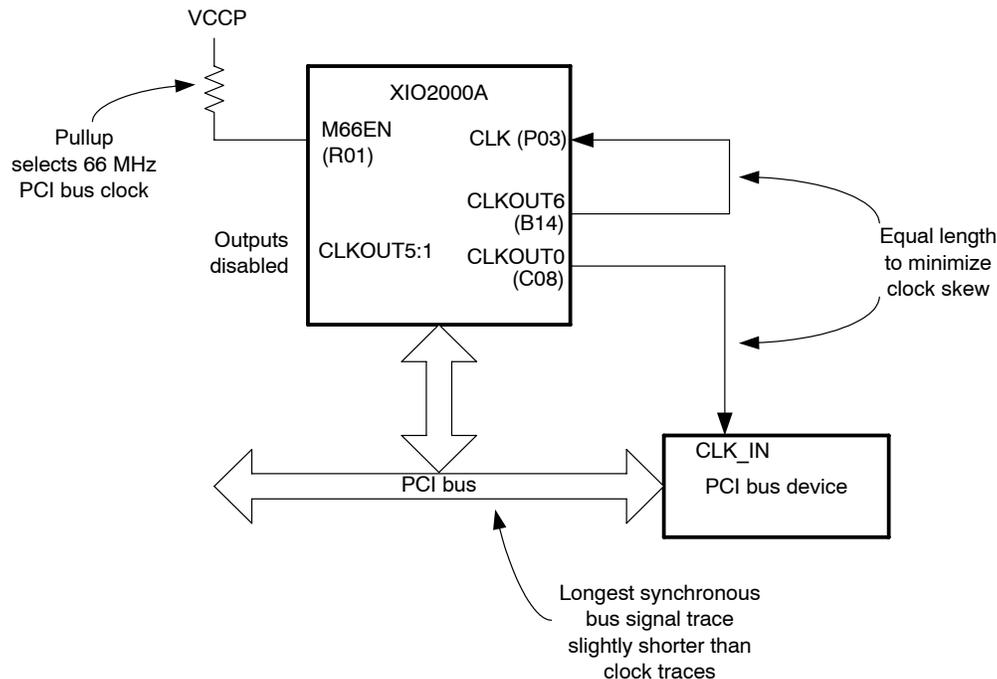
Because $\overline{\text{WAKE}}$ is an open-drain output, a system side pullup resistor is required to prevent the signal from floating. The drive capability of this open-drain output is 4 mA. Therefore, the value of the selected pullup resistor must be large enough to assure a logic low signal level at the receiver. A robust system design will select a pullup resistor value that de-rates the output driver current capability by a minimum of 50%. At 3.3 V with a de-rated drive current equal to 2 mA, the minimum resistor value is 1.65 k Ω . Larger resistor values are recommended to reduce the current drain on the V_{AUX} supply.

4 PCI Bus Interface Considerations

The XIO2000A has a 32-bit PCI interface that can operate at either 33 MHz or 66 MHz. This interface is compliant with the *PCI Local Bus Specification*, Revision 2.3. The remainder of this section describes implementation considerations for the XIO2000A secondary PCI bus interface.

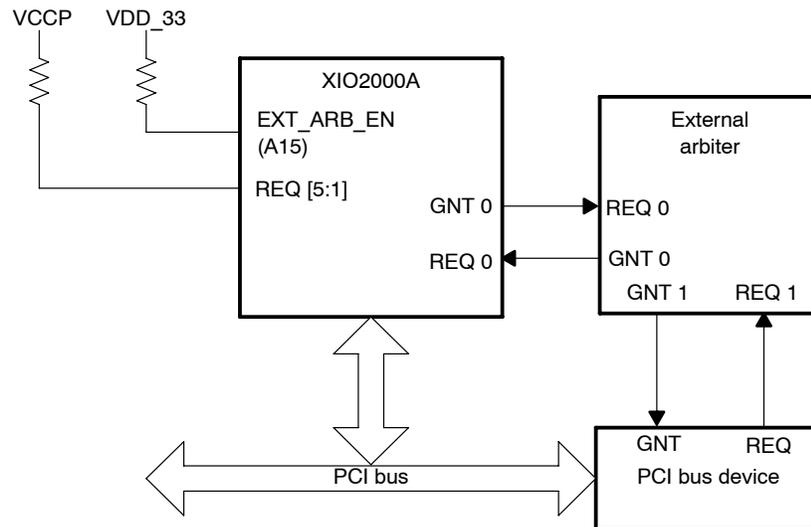
- AD31:0, C/BE[3:0], PAR, DEVSEL, FRAME, STOP, TRDY, PERR, SERR, and IRDY are required signals and must be connected to each PCI bus device. The maximum signal loading specification for a 66-MHz bus is 30 pF and for a 33-MHz bus is 50 pF. All of these signals are bused and synchronous to the PCI clock. All synchronous PCI bus signals must be length matched to meet clock setup and hold requirements. PCI bus approved pullup resistors connected to V_{CCP} are needed on the following terminals: IRDY, TRDY, FRAME, STOP, PERR, SERR, and DEVSEL.
- The XIO2000A supports up to six external PCI bus devices with individual CLKOUT, \overline{REQ} and \overline{GNT} signals. An internal PCI bus clock generator function provides six low-skew clock outputs. Plus, there are six \overline{REQ} inputs and six \overline{GNT} outputs from the internal PCI bus arbiter. Each PCI bus device connects to one CLKOUT signal, one \overline{REQ} signal, and one \overline{GNT} signal. All three signals are point-to-point connections. The \overline{REQ} and \overline{GNT} signals are synchronous and must be length matched to meet clock setup and hold requirements. Unused CLKOUT signals can be disabled by asserting the appropriate CLOCK_DISABLE bit in the clock control register at offset D8h. Unused \overline{REQ} signals can be disabled using a weak pullup resistor to V_{CCP} . Unused \overline{GNT} signals are no connects.
- An external clock feedback feature is provided to de-skew PCI bus clocks. Connecting the CLKOUT[6] terminal (B14) to the CLK terminal (P03) is required if any of the other six CLKOUT[5:0] terminals are used to clock PCI bus devices. All connected CLKOUT[6:0] signals must be length matched within 10 mils to minimize clock skew and satisfy PCI bus setup and hold requirements for synchronous signals. The CLKOUT signals should be slightly longer than the longest synchronous PCI bus signal trace. Figure 3 illustrates the external PCI bus clock feedback feature. The use of series resistors on the 7 PCI bus clocks should be considered to reduce circuit board EMI.

NOTE: There is one exception to this length-matching rule associated with connecting a CLKOUT signal to PCI socket: For this case, the CLKOUT signal connected to a PCI socket should be 2.5 inches shorter than the other CLKOUT signals.

Figure 3. External PCI Bus Clock Feedback


- The M66EN terminal (R01) determines the operating frequency for the secondary PCI bus. When $\overline{\text{PERST}}$ is deasserted and if a pullup resistor to V_{CCP} is detected on terminal R01, the XIO2000A CLKOUT terminals operate at 66 MHz. A pulldown resistor to V_{SS} switches the CLKOUT terminals to 33-MHz operation. If the PCI bus is desired to run at 66 MHz, but there may be 33-MHz add-in cards connected to the bus, the M66EN terminal is connected to V_{CCP} through a 5-k Ω resistor and bused to all PCI bus slots which may require the lower speed clock. For this system configuration, add-in cards are required to short the M33EN signal to ground if they only operate at 33-MHz.
- IDSEL for each PCI bus device must be resistively coupled (100 Ω) to one of the address lines between AD31 and AD16. See the XIO2000A Data Manual for the configuration register transaction device number to AD bit translation chart.
- PCI interrupts can be routed to the $\overline{\text{INT}}[\text{D:A}]$ inputs on the XIO2000A. These four inputs are asynchronous to the PCI bus clock and detect state changes even if the PCI bus clock is stopped. For each $\overline{\text{INT}}[\text{D:A}]$ input, an approved PCI bus pullup resistor to V_{CCP} is required to keep each interrupt signal from floating.
- $\overline{\text{PRST}}$ is a required PCI bus signal and must be connected to all devices. This output signal is asynchronous to the PCI bus clock. Because the output driver is always enabled and either driving high or low, no pullup resistor is needed.
- $\overline{\text{LOCK}}$ is an optional PCI bus signal. If $\overline{\text{LOCK}}$ is present in a system, it is connected to each PCI bus device that supports the feature and must meet PCI bus loading requirements for the selected clock frequency. An approved PCI bus pullup resistor to V_{CCP} is required to keep this signal from floating. $\overline{\text{LOCK}}$ is a bused signal and synchronous to the PCI bus clock. All synchronous PCI bus signals must be length matched to meet clock setup and hold requirements.

- SERIRQ is an optional PCI bus signal. When $\overline{\text{PERST}}$ is deasserted, if a pullup resistor to V_{CCP} is detected on terminal T04, the serial IRQ interface is enabled. A pulldown resistor to V_{SS} disables this feature. If SERIRQ is present in a system, it is connected to each PCI bus device that supports the feature and must meet PCI bus loading requirements for the selected clock frequency. An approved PCI bus pullup resistor to V_{CCP} is required to keep this signal from floating. SERIRQ is a bused signal and synchronous to the PCI bus clock. All synchronous PCI bus signals must be length matched to meet clock setup and hold requirements.
- $\overline{\text{CLKRUN}}$ is an optional PCI bus signal that is shared with the GPIO0 terminal (T05). When $\overline{\text{PERST}}$ is de-asserted and if a pullup resistor to $V_{\text{DD_33}}$ is detected on terminal B15 (CLKRUN_EN), the clock run feature is enabled. A no connect on the B15 terminal disables the CLKRUN feature. If $\overline{\text{CLKRUN}}$ is required in a system, this terminal is connected to each PCI bus device and must meet PCI bus loading requirements for the selected clock frequency. An approved PCI bus pullup resistor to $V_{\text{DD_33}}$ is required per the PCI Mobile Design Guide. $\overline{\text{CLKRUN}}$ is a bused signal and synchronous to the PCI bus clock. All synchronous PCI bus signals must be length matched to meet clock setup and hold requirements.
- PWR_OVRD is an optional PCI bus signal that is shared with the GPIO1 terminal (U05). In PWR_OVRD mode, this terminal is always an output and is asynchronous to the PCI bus clock. When the power override control bits in the general control register at offset D4h are set to 001b or 011b, the U05 terminal operates as the PWR_OVRD signal. Prior to setting the power override control bits, the GPIO1 // PWR_OVRD terminal defaults to a standard GPIO terminal.
- $\overline{\text{PME}}$ is an optional PCI bus input terminal to detect power management events from downstream devices. The $\overline{\text{PME}}$ terminal (M15) is operational during both main power states and VAUX states. The $\overline{\text{PME}}$ receiver has hysteresis and expects an asynchronous input signal. The board design requirements associated with this $\overline{\text{PME}}$ terminal are the same whether or not the terminal is connected to a downstream device. If the system includes a VAUX supply, the $\overline{\text{PME}}$ terminal requires a weak pullup resistor connected to VAUX to keep the terminal from floating. If no VAUX supply is present, the pullup resistor is connected to $V_{\text{DD_33}}$.
- The bridge supports external PCI bus clock sources. If an external clock is a system requirement, the external clock source is connected to the CLK terminal (P03). The trace length relationship between the synchronous bus signals and the external clock signals that is previously described is still required to meet PCI bus setup and hold. For external clock mode, all seven CLKOUT[6:0] terminals can be disabled using the clock control register at offset D8h. Plus, the XIO2000A clock run feature must be disabled with external PCI bus clocks because there is no method of turning off external clocks.
- The XIO2000A supports an external PCI bus arbiter. When $\overline{\text{PERST}}$ is deasserted, the logic state of the EXT_ARB_EN terminal (A15) is checked. If an external arbiter is required, terminal A15 is connected to $V_{\text{DD_33}}$. When connecting the XIO2000A to an external arbiter, the bus REQ signal to the external arbiter is the bridge's GNT0 output terminal (A08). Likewise, the bus GNT signal from the external arbiter is connected to the bridge's REQ0 input terminal (B08). When in external arbiter mode, all internal XIO2000A port arbitration features are disabled. Figure 4 illustrates the connectivity of an external arbiter.

Figure 4. External Arbiter Connections


4.1 Bus Parking

Because of the shared bus nature of PCI, if the bus is idle at any given time, some device on the bus must drive floating signals to stable states. These signals are the address/data lines, the command/byte enables, and a valid parity. If no devices are requesting use of the bus, it is the responsibility of the arbiter to assign ownership of the bus so that the bus signals are never floating while in idle states.

If the XIO2000A internal arbiter is enabled then there are two modes supported for bus parking. The default mode for bus parking is for the arbiter to continue to assert $\overline{\text{GNT}}$ for the last bus master. In this mode when all devices have deasserted their $\overline{\text{REQ}}$ signals, the arbiter will continue to assert the $\overline{\text{GNT}}$ for the last bus master and that device is required to drive a stable pattern onto the required signals. This will continue until another device requests use of the bus resulting in the arbiter removing $\overline{\text{GNT}}$ from the current bus owner and granting it to the new requestor.

Alternatively, the XIO2000A can be configured to self-park. In this mode any time no devices have their $\overline{\text{REQ}}$ asserted, the XIO2000A removes $\overline{\text{GNT}}$ from the current bus owner and drives a stable pattern onto the required lines.

It is suggested that implementations use the default mode of bus parking. The PCI Specification recommends leaving the current $\overline{\text{GNT}}$ signal asserted if no devices are asserting $\overline{\text{REQ}}$. Some PCI bus masters release their $\overline{\text{REQ}}$ signals after having begun a transaction, even if that transaction requires the use of the bus for an extended time. If the XIO2000A self-parks the bus, then these bus masters have their transaction lengths limited to the latency timer setting. This may result in increased arbitration for the bus, higher overhead for transactions, and decreased bus performance.

5 Miscellaneous Terminal Considerations

5.1 GPIO Terminals

There are eight General Purpose Input/Output (GPIO) terminals in the XIO2000A. All eight GPIO terminals are 3.3 V tolerant. Four of the GPIO terminals are shared with other miscellaneous functions. The remaining four terminals are always general purpose inputs or outputs.

One Classic PCI configuration register defines the GPIO terminal direction as either an input or an output. A second register either defines the GPIO output state or reports the GPIO input state. The power-up default is GPIO input mode. The power-up default signal level for each GPIO terminal is determined by either an internal active pullup transistor or any externally attached components. Internal active pullup transistors are present on GPIO terminals 0, 1, 2, 3, 4, 6, and 7. When a GPIO terminal is configured as an input, the internal active pullup transistor is enabled. If a GPIO terminal is configured as an output, the internal active pullup transistor is disabled.

The following list of GPIO terminals have special requirements that must be considered when interfacing to the GPIO terminals:

- GPIO0: If CLK_RUN mode is selected, this terminal (T05) requires a pullup resistor to V_{DD_33} per the PCI Mobile Design Guide. Otherwise, this terminal operates as a standard GPIO bit.
- GPIO1: If the power override control bits in the general control register are set to 001b or 011b, this terminal is the PCI bus PWR_OVRD output. Otherwise, this terminal operates as a standard GPIO bit.
- GPIO2: This terminal must be a logic one at the de-assertion of $\overline{\text{PERST}}$ to enable PCI Express 1.0a compatibility mode. After the de-assertion of $\overline{\text{PERST}}$, this terminal operates as a standard GPIO bit.
- GPIO4//SCL and GPIO5//SDA: These terminals share the SCL and SDA signals for the external EEPROM. If the GPIO5//SDA terminal is a 1b at the de-assertion of $\overline{\text{PERST}}$, the serial EEPROM interface is enabled. A 0b disables the serial EEPROM interface. If the serial EEPROM interface is enabled, external pullup resistors to V_{DD_33} are required on both terminals per the serial EEPROM specification. Otherwise, these terminals operate as standard GPIO bits.
- GPIO3, GPIO6, and GPIO7: These terminals always operate as standard GPIO bits.

5.2 $\overline{\text{GRST}}$ Terminal

$\overline{\text{GRST}}$ is a global reset terminal that is provided for custom reset requirements. When this input is asserted low, all registers, state machines, digital logic, and analog circuits are returned to their power-up default state. This reset is asynchronous to all external reference clock and internal clock domains. The $\overline{\text{GRST}}$ input buffer has hysteresis and an internal active pullup resistor. This input is powered either by main power or by VAUX power. Therefore, global resets may be initiated during either power state.

During an XIO2000A device power-up from the D3_{cold} power state, there is no requirement to assert this terminal low. An internal power-up reset function performs an equivalent reset to $\overline{\text{GRST}}$. Because this input is powered during V_{AUX} states, it is imperative that any external circuits connected to $\overline{\text{GRST}}$ do not erroneously drive this input low when main power is lost. This results in the reset of sticky control bits and power management state-machines.

If the system designer has no need for a custom reset, the $\overline{\text{GRST}}$ terminal can simply be left floating. An internal active pullup resistor will guarantee a non-reset state.

5.3 Reserved Terminals

The XIO2000A has multiple reserved input and output terminals. The recommendation for all output terminals is a no connect state. Do not connect these output terminals to other signals or external components. Doing so may increase power consumption or cause output driver signal conflicts.

The input terminals must be connected to either $V_{\text{DD}_{33}}$ or V_{SS} . The reserved terminal table in the XIO2000A Data Manual provides the connection requirements. The connection may either be a direct short to the recommended supply/ground plane or through a pullup/down resistor. Leakage currents associated with each input must be considered when selecting the resistor option. The minimum leakage current is $\pm 1 \mu\text{A}$ and the maximum is $\pm 100 \mu\text{A}$. Because the leakage current varies from input to input, the safest resistor option is to assume $\pm 100 \mu\text{A}$.

6 Interrupt Configurations

The XIO2000A provides system designers with two options when configuring interrupts.

Standard parallel PCI bus interrupts may be connected to XIO2000A terminals $\overline{\text{INTA}}$, $\overline{\text{INTB}}$, $\overline{\text{INTC}}$, and $\overline{\text{INTD}}$. When a PCI bus device asserts or de-asserts one of these inputs, the XIO2000A asynchronously detects the state change and generates upstream PCI Express interrupt messages. This interrupt conversion logic is always enabled and operates even when PCI bus clocks are stopped. The PCI Express interface must be link trained and in the L0 Link Active State for interrupt messages to be sent upstream. The XIO2000A Data Manual illustrates the PCI Express message format for assert and deassert INTx messages.

Interrupts can also be signaled through the serial IRQ interface (terminal T04, SERIRQ). The SERIRQ interface detects ISA style IRQ interrupts associated with bus frame IRQ0 to IRQ15. These interrupts are necessary for some 16-bit PC Cards to function properly. Both edge mode and level mode serial IRQ interrupts are supported. When a serial IRQ interrupt is detected and the XIO2000A is properly configured, an MSI message is generated and sent upstream on the PCI Express interface. The XIO2000A Data Manual includes a section that includes additional detail associated with the serial IRQ and MSI message functionality.

When the XIO2000A is used in an option card, an interrupt binding is required by the PCI-to-PCI Bridge Architecture Specification, Revision 1.0. This binding is between the PCI bus device number (as given in the Type 1 configuration address and, therefore, the IDSEL line) and the $\text{INTx}\#$ line it uses when requesting an interrupt.

The PCI bus connector has only four interrupt lines assigned to it: $\overline{\text{INTA}}$, $\overline{\text{INTB}}$, $\overline{\text{INTC}}$, and $\overline{\text{INTD}}$. Multiple PCI bus devices might have to share these four interrupts. The XIO2000A fully supports the conversion of all four PCI bus INTx lines to upstream PCI-Express assert and deassert INTx messages. But, the XIO2000A only supports 16 IDSEL lines. Therefore, only device numbers 0 to 15 are listed in the Table 1 binding table.

Because only the BIOS knows how the PCI $\text{INTx}\#$ lines are routed, a mechanism is required to inform the device driver which IRQ its device will request an interrupt on. The interrupt line register in each PCI bus device stores this information. Behind a PCI-to-PCI bridge, the BIOS code assumes the binding is as listed and writes the IRQ number into each device. The interrupt binding defined in Table 1 is mandatory for option cards using PCI-to-PCI bridges.

Table 1. Interrupt Bindings for Option Cards Using PCI-to-PCI Bridges

Device Number on Secondary Bus	Interrupt Pin on PCI Bus Device/Connector	Interrupt Pin on XIO2000A
0, 4, 8, 12	INTA# INTB# INTC# INTD#	INTA# INTB# INTC# INTD#
1, 5, 9, 13	INTA# INTB# INTC# INTD#	INTB# INTC# INTD# INTA#
2, 6, 10, 14	INTA# INTB# INTC# INTD#	INTC# INTD# INTA# INTB#
3, 7, 11, 15	INTA# INTB# INTC# INTD#	INTD# INTA# INTB# INTC#

7 Software Considerations

The XIO2000A PCI Express to PCI translation bridge is natively supported by either BIOS software and/or operating system software that recognizes the classic PCI-to-PCI bridge programming model. XIO2000A classic PCI configuration register space uses a type 1 PCI bridge header. All other XIO2000A advanced features default to a disabled state and do not require configuration register initialization for basic operation.

However, to fully use advanced features within the XIO2000A, custom device drivers are required. The best example of an advanced feature is the PCI Express Extended Virtual Channel Configuration Register space. Software for this feature is not presently supported by either today's operating systems or by Texas Instruments. Designers should plan to develop custom device drivers if this advanced feature is required in a system.

7.1 Serial EEPROM Interface Configuration

An external serial EEPROM port is provided on the XIO2000A for power-up configuration support. Typically, the system BIOS initializes the configuration registers associated with the serial EEPROM feature. But for custom systems or PCI-Express add-in cards, this feature is provided to automate basic XIO2000A configuration register initialization.

The registers loaded by the serial EEPROM feature are located in the classic PCI configuration space. The names of these registers include the subsystem ID and subsystem vendor ID, general control, clock control and mask, arbiter control and mask, and serial IRQ control registers.

NOTE: The serial EEPROM also loads TI proprietary registers. The data loaded into these 12 bytes must not be changed from the values specified in the EEPROM register loading map. Otherwise, the operational state of the bridge is indeterminate.

Terminal T07, named GPIO5 // SDA, provides a basic EEPROM enable or disable option. When PERST is deasserted, the logic state of this terminal is checked. If a 1b is detected, the serial EEPROM interface is enabled. A 0b disables the interface. An external pullup or pulldown resistor is required to generate the appropriate logic state.

Immediately after the detection of a 1b on terminal T07, the XIO2000A performs the following actions:

1. Bit 3 (SBDETECT) in the serial-bus control and status register is set.
2. Bit 4 (ROMBUSY) in the serial-bus control and status register is set and a serial EEPROM download is initiated to device address 1010000b and word address 00h.
3. The EEPROM data byte in word address 00h is checked. If bit 7 is asserted, this indicates an End-of-List Indicator and the serial-bus state-machine aborts the download. A 00h value indicates a valid PCI Express-to-PCI Bus Bridge function header. EEPROM word address 00h must only be loaded with either 00h, 80h or FFh. Other byte values must not be used because they may cause configuration register download errors and leave the XIO2000A in an indeterminate state.
4. After a valid function header is detected, the EEPROM data byte in word address 01h is read. This location determines the number of bytes that are downloaded into the bridge configuration registers and must equal 1Eh.
5. The starting EEPROM word address is 02h and the ending address is 1Fh. While downloading the 1Eh data bytes, each byte is loaded into the specified bridge configuration register. The XIO2000A Data Manual includes an EEPROM register loading map.
6. The last data byte at word address 20h is checked for a valid end-of-list indicator byte. This data byte must equal 80h.
7. When the serial EEPROM interface state machine is finished, the ROMBUSY status bit is deasserted. If any errors are detected during the download procedure, bit 0 (ROM_ERR) in the serial-bus control and status register is set. If ROM_ERR status is asserted, the state of any configuration register targeted by the EEPROM download is unknown.

Additional detail is provided in the XIO2000A Data Manual related to the serial EEPROM function and configuration register download map.

7.2 BIOS Considerations

This section provides a high-level overview of the registers which must be programmed by the BIOS upon initialization of the XIO2000A. In general, the only registers which must be programmed for proper operation within a Windows operating system are those registers which are EEPROM loadable. Other registers may be changed according to system implementation. Microsoft provides the following reference documents concerning architecture and driver support for PCI and PCI Express devices in Windows:

<http://www.microsoft.com/whdc/system/bus/pci/default.mspx>

7.2.1 Classic PCI Configuration Registers

Primary Bus Number Register (PCI offset 18h) – This register indicates the bus number of the PCI bus segment that the primary PCI Express interface is connected to. The bridge uses this information to determine how to respond to a type 0 configuration transaction. The register default is 00h.

Secondary Bus Number Register (PCI offset 19h) – This register indicates the bus number of the PCI bus segment that the secondary PCI interface is connected to. The bridge uses this information to determine how to respond to a type 1 configuration transaction. The register default is 00h.

Subordinate Bus Number Register (PCI offset 1Ah) – This register indicates the bus number of the highest number PCI bus segment that is downstream of the bridge. The bridge uses this information to determine how to respond to a type 1 configuration transaction. The register default is 00h.

Subsystem Vendor ID and Subsystem ID Registers (PCI offsets 84h and 86h) – These registers are used for subsystem and option card identification purposes. Typically, these registers contain the OEM vendor ID and an OEM identified designator. These fields can be programmed using the EEPROM or BIOS. If using BIOS, the subsystem access register at offset D0h is written to update the subsystem vendor ID and subsystem ID registers.

GPIO Control and Data Registers (PCI offsets B4h and B6h) – These registers determine the direction of the GPIO terminals and set the default state for all GPIO outputs. The initialization state for these registers is system architecture dependent. The control register default is GPIO input mode.

General Control Register (PCI offset D4h) – This register controls various bridge power management and interface operation specific functions that are fully described in the XIO2000A Data Manual. This register can be programmed using the EEPROM or BIOS.

Clock Control and Mask Registers (PCI offsets D8h and D9h) – These registers control enabling or disabling the seven secondary PCI bus clock outputs during both normal power states and power override states. This register can be programmed using the EEPROM or BIOS. The exact number of required PCI bus clocks is system implementation specific. Unused clock outputs must be disabled.

Arbiter Control and Request Mask Registers (PCI offsets DCh and DDh) – These registers control the internal classic PCI bus arbiter function. Register options include PCI bus high/low priority tier selection, bus parking, request masking, arbitration timeout, and automatic request masking. This register can be programmed using the EEPROM or BIOS.

Serial IRQ Mode and Edge Control Registers (PCI offsets E0h, E2h and E3h) – These registers control the operating characteristics of the serial IRQ interface. Register options include internal classic PCI bus arbiter function. Register options include start frame pulse width, continuous versus quiet mode, interface drive mode, and level versus edge mode interrupt detection. This register can be programmed using the EEPROM or BIOS.

8 Power Management Considerations

8.1 D3/L2 Power Management Information

The *PCI Express Card Electromechanical Specification* contains a section that specifies the operation of a PCI Express device when transitioning from D0/L0 to D3/L2 and back to D0/L0 power management states. Because the primary interface on the XIO2000A is PCI Express, the bridge supports this specification for both D3_{hot} and D3_{cold} power management states. System software has the option to place the bridge into the D3/L2 power management state. This process is started in the bridge by setting the PWR_STATE field in the power management control and status register to 11b. By following the procedure outlined in the *PCI Express Card Electromechanical Specification*, the bridge may be transitioned to either the D3_{hot} or D3_{cold} states to reduce system power.

A downstream PCI bus device may assert $\overline{\text{PME}}$ to initiate the power management state transition from D3/L2 back to D0/L0. As a PCI Express to PCI bus translation bridge, the XIO2000A contains the functionality to detect a secondary bus $\overline{\text{PME}}$ event and to generate an upstream PCI Express $\overline{\text{WAKE}}$ or beacon signal. After the bridge enters the D3/L2 power management state and $\overline{\text{PERST}}$ is asserted, the detection of a $\overline{\text{PME}}$ event is forwarded to the PCI Express interface by asserting $\overline{\text{WAKE}}$ or generating a beacon signal. $\overline{\text{WAKE}}$ is always asserted by the bridge. For a beacon signal to be generated, bit 10 (BEACON_ENABLE) in the general control register must be asserted. $\overline{\text{WAKE}}$ and beacon remain active until $\overline{\text{PERST}}$ is deasserted.

A $V_{\text{DD}_33_AUX}$ power terminal, coupled with internal circuits that combine main power and V_{AUX} power, supplies power to the logic that controls power management state transitions from D3_{cold} back to D0/L0. Internal “sticky” logic maintains not only the content of specific bridge PCI register bits, but also information about the operational states of the bridge including state machine context and other internal mechanisms. $\overline{\text{PERST}}$ has no effect on the internal “sticky” logic.

8.2 Active State Power Management Information

The PCI Express interface on the XIO2000A can automatically reduce power when there is no queued bus activity. Once this feature is enabled by software, the XIO2000A device automatically transitions into and out of a low power state. The bridge supports both the L0's and L1 active state power management (ASPM) requirements.

In the PCI Express link capabilities registers, two 3-bit exit latency fields specify the latency time required for the Bridge to transition from either the L0 or L1 state back to the L0 state. In the PCI Express device capabilities register, two 3-bit acceptable latency fields specify the maximum latency time that the Bridge will tolerate for the attached upstream PCI Express device to transition from either the L0's or L1 state back to the L0 state. The acceptable latency fields are an indirect measure of the Bridge's internal buffering.

Power management software uses the reported acceptable latency number to compare against the exit latencies reported by all components physically located on the PCI-Express link between the Bridge and the Root Complex to determine whether ASPM entry can be used with no significant impact to system performance.

8.3 PCI Bus Power Override Information

System software has the ability to manually reduce power on the secondary PCI bus using the bridge's power override feature. During system initialization, XIO2000A configuration registers must be loaded with system specific power information and power override instructions. After this initial setup, the PCI Express set slot power limit message may be used to either enable or disable the power override feature.

During system initialization the following configuration register fields are loaded. These fields are loaded by either the BIOS or serial EEPROM.

1. The general control register contains MIN_POWER_SCALE and MIN_POWER_VALUE fields that are loaded with the power information associated with the bridge and all downstream PCI bus devices.
2. The general control register contains a POWER_OVRD field that is loaded with the secondary PCI bus power override option.
3. If the power override option associated with disabling secondary clocks is selected, the clock mask register should be initialized.

After the previously described initialization procedure, the PCI Express set slot power limit message may be used to either enable or disable the power override feature. If the scale and value power information in the PCI Express message is less than the general control register SCALE and VALUE fields, then the power override feature is enabled. If the scale and value power information in the PCI Express message is equal to or greater than the SCALE and VALUE fields, then the power override feature is disabled.

8.4 $\overline{\text{CLKRUN}}$ Information

By implementing the $\overline{\text{CLKRUN}}$ feature, when the PCI bus is inactive, the bridge automatically stops the PCI clocks to reduce system power. The bridge supports the clock run protocol as specified in the *PCI Mobile Design Guide* and assumes the role of the central resource master.

When $\overline{\text{PERST}}$ is deasserted, the logic state of terminal B15 (CLKRUN_EN) is checked. If B15 is connected to V_{DD_33} , the clock run feature is enabled. Terminal T05 (GPIO0) becomes the $\overline{\text{CLKRUN}}$ signal.

An external pullup resistor to V_{DD_33} is required on terminal T05 (GPIO0) to keep the $\overline{\text{CLKRUN}}$ signal from floating. The value of this pullup resistor must be large enough to assure a logic low when the weakest driver attached to the $\overline{\text{CLKRUN}}$ signal is active. The $\overline{\text{CLKRUN}}$ driver in the bridge is 4 mA. The minimum recommended pullup resistor value is 1.65 k Ω . This resistor value de-rates the $\overline{\text{CLKRUN}}$ driver maximum current sinking requirement by 50 percent to reduce system power.

Additional detail related to the $\overline{\text{CLKRUN}}$ feature is provided in the XIO2000A Data Manual.

8.5 PCI Bus Clock Power and EMI Considerations

After an XIO2000A power-up sequence, all PCI bus clocks are enabled and toggling. The system designer should consider both the power and EMI implications associated with this power-up default mode.

This clock default mode was chosen to ensure that all PCI devices attached to the secondary bus are reset according to PCI bus specification requirements. Immediately after a system power-up, there are several options for disabling unused PCI bus clocks, thus reducing both system power and EMI.

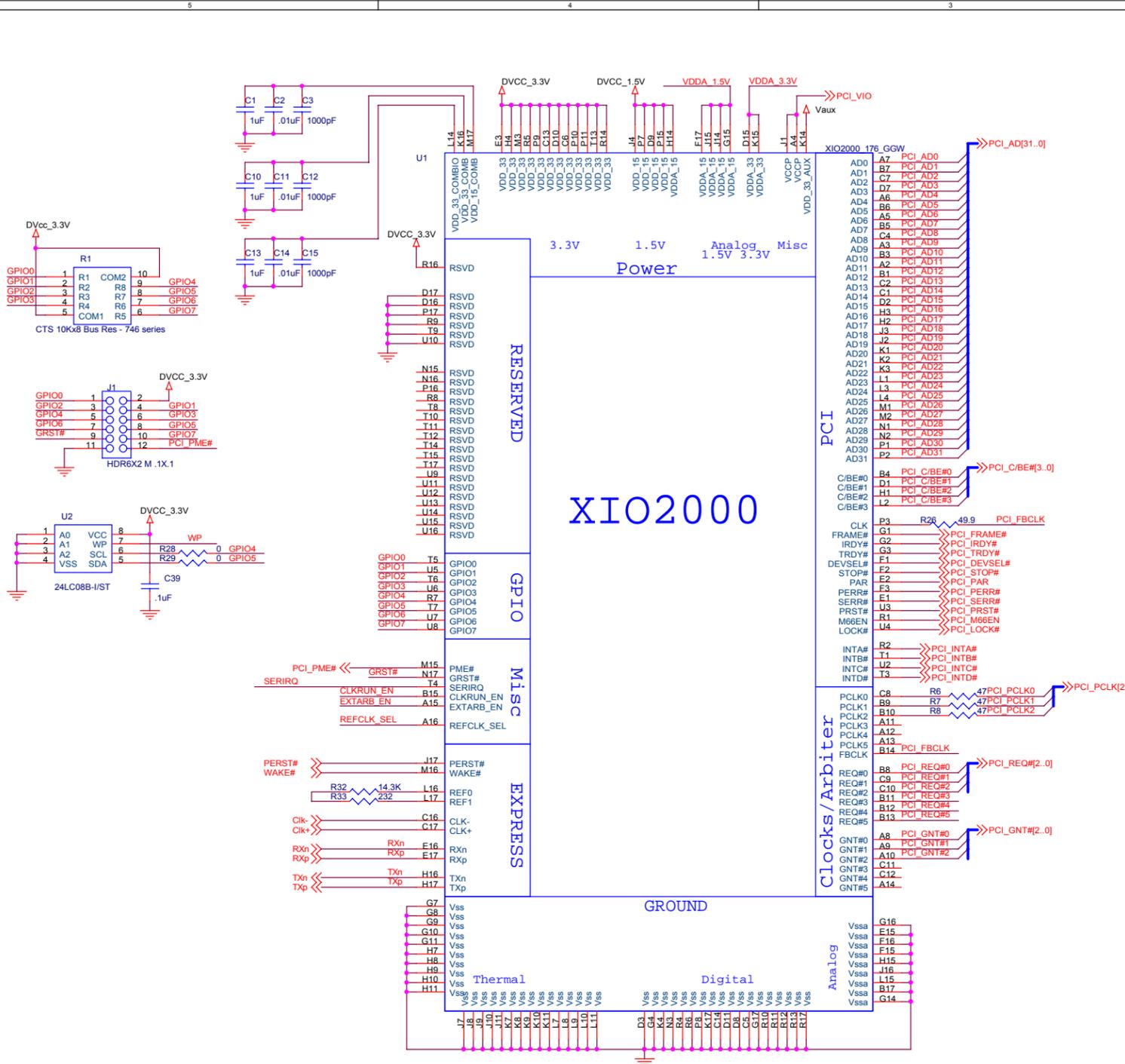
In the Classic PCI Configuration Register Space at offset D8h is the Clock Control Register. Bits 6:0 in this register control enabling or disabling the CLKOUT[6:0] terminals on the XIO2000A device. These bits may be written from either the serial EEPROM or through the BIOS. Disabling all unused PCI bus clocks is highly recommended.

NOTE: The CLKOUT[6] terminal is normally used as the PCI bus feedback clock for the XIO2000A. Disabling this clock is not recommended because this stops the operation of the XIO2000A's PCI bus interface logic.

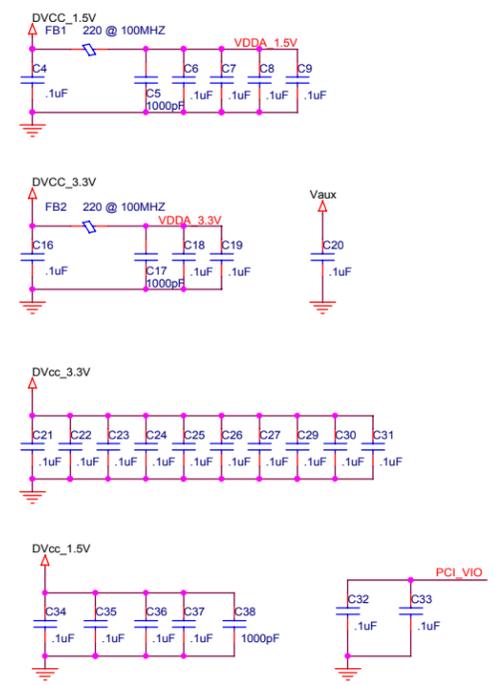
If the system contains multiple PCI bus add-in card slots, the decision to enable or disable each clock should be controlled by the BIOS. If the BIOS queries each add-in slot behind the XIO2000A, a device ID and vendor ID response indicates the presence of an add-in card. An FFFF FFFFh response indicates that no device is present and the PCI bus clock associated with that add-in slot should be disabled.

9 Reference Schematics GZZ/ZZZ Package

The following schematics show the most basic implementation of the XIO2000A possible. These schematics provide minimum bridge functionality.



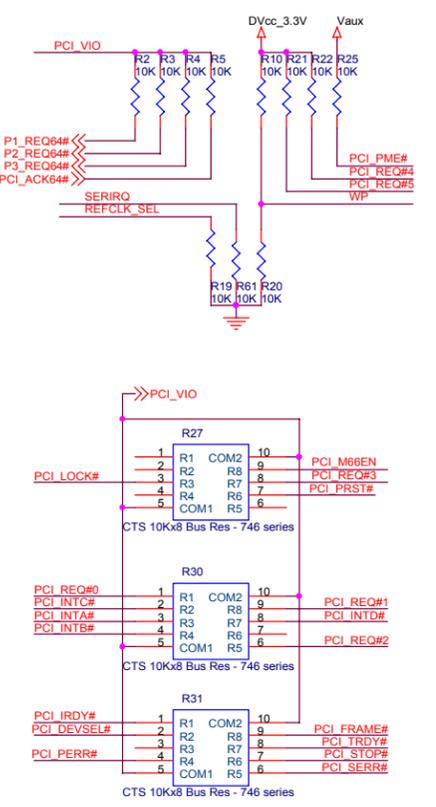
Bridge Power Filtering/Decoupling

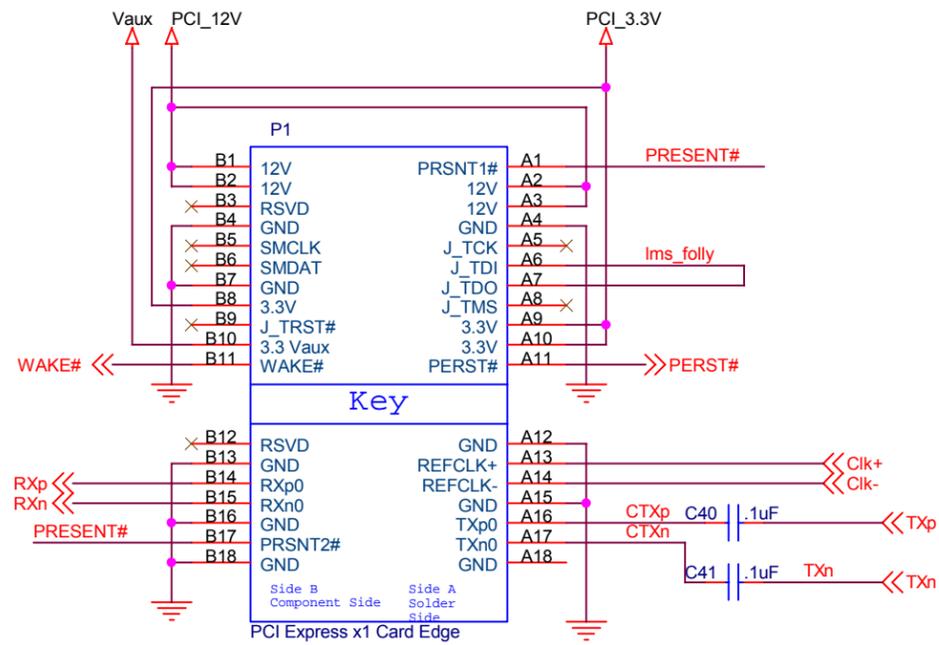


NOTE: C38 should go directly under the pin H14 on U1

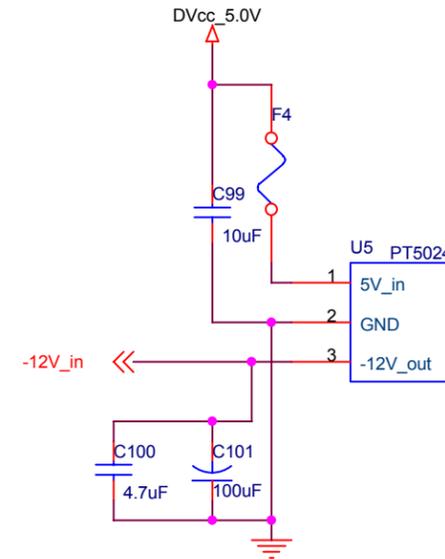
NOTE: In actual EVM FB1 and FB2 are L1 and L2. Inductors have been replaced with ferrites. Ferrites have minimal impact on jitter but dramatically improve EMI characteristics.

Pull Ups/Pull Downs

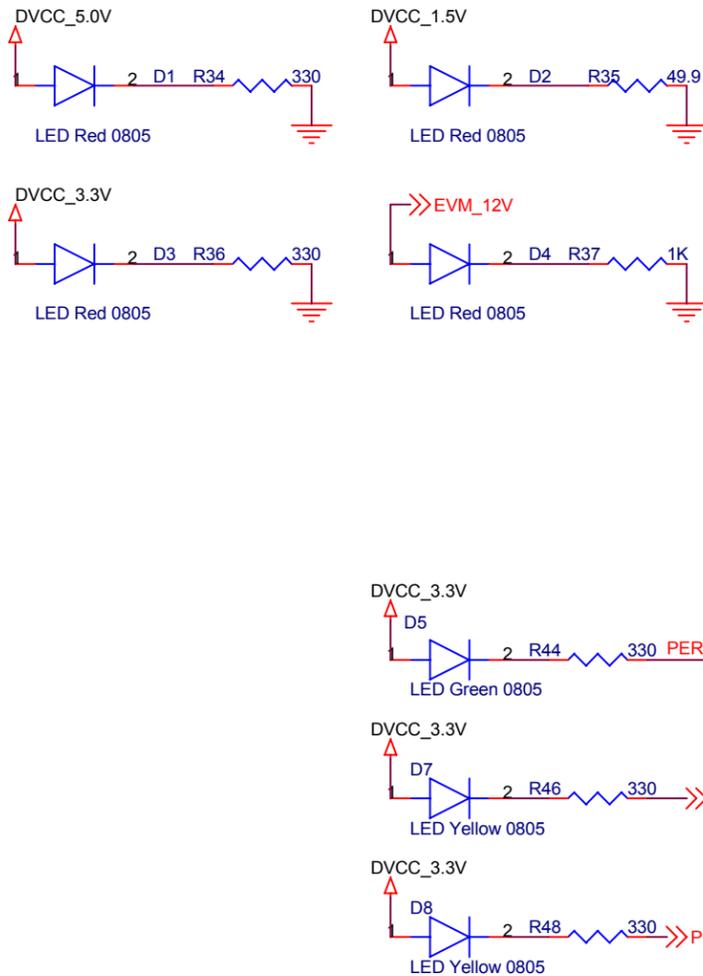




-12V Inverting Regulator (for PCI Slots)

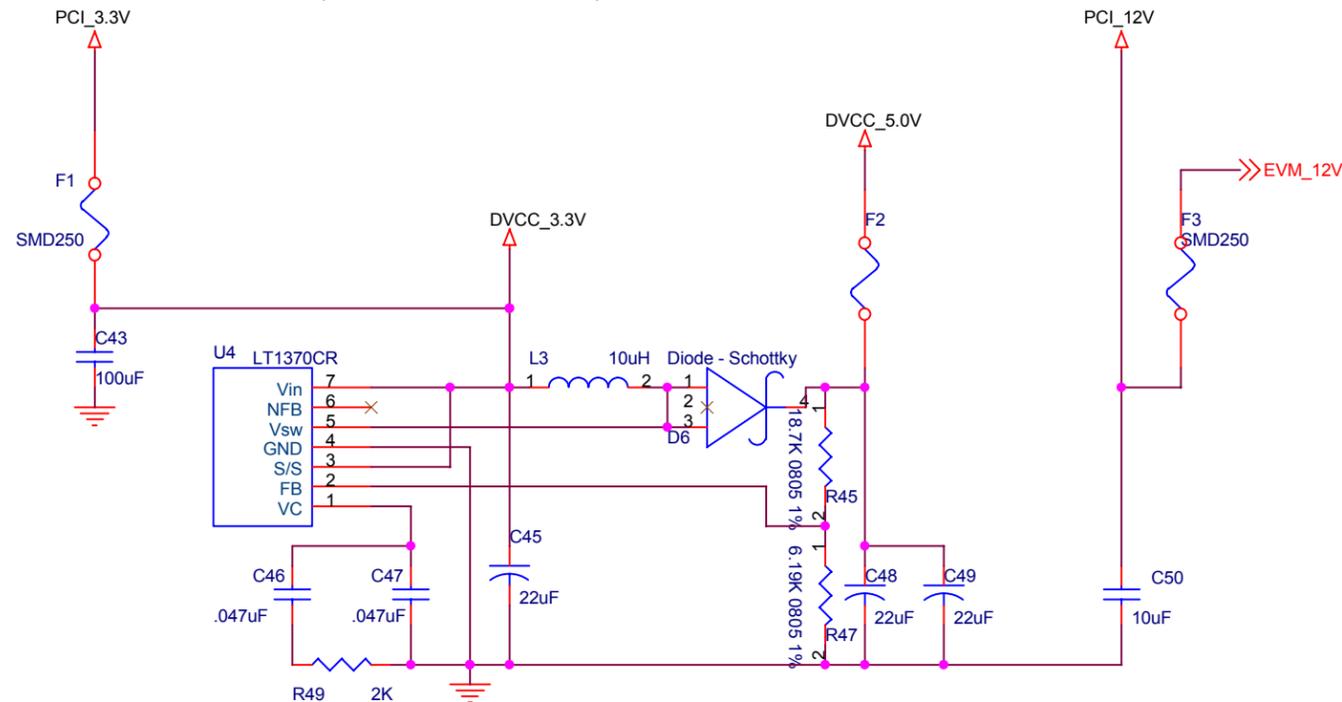


LEDs

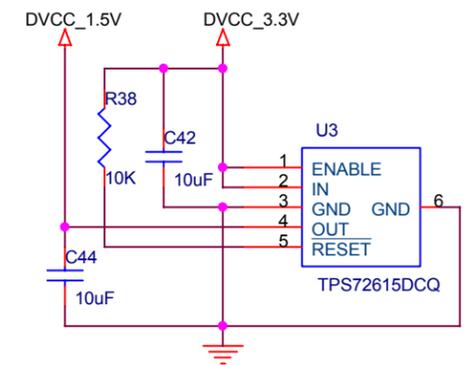


Power

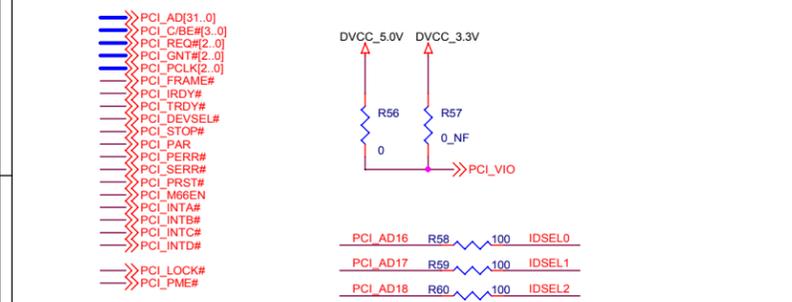
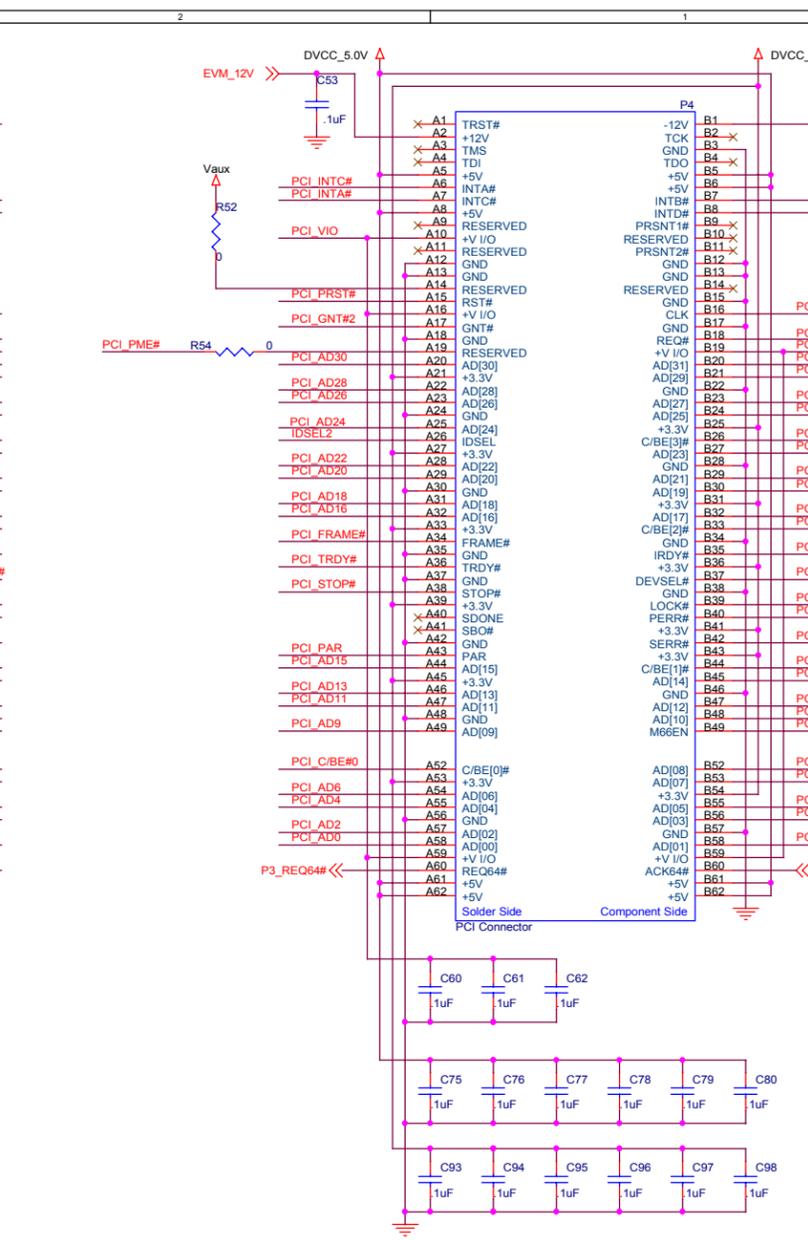
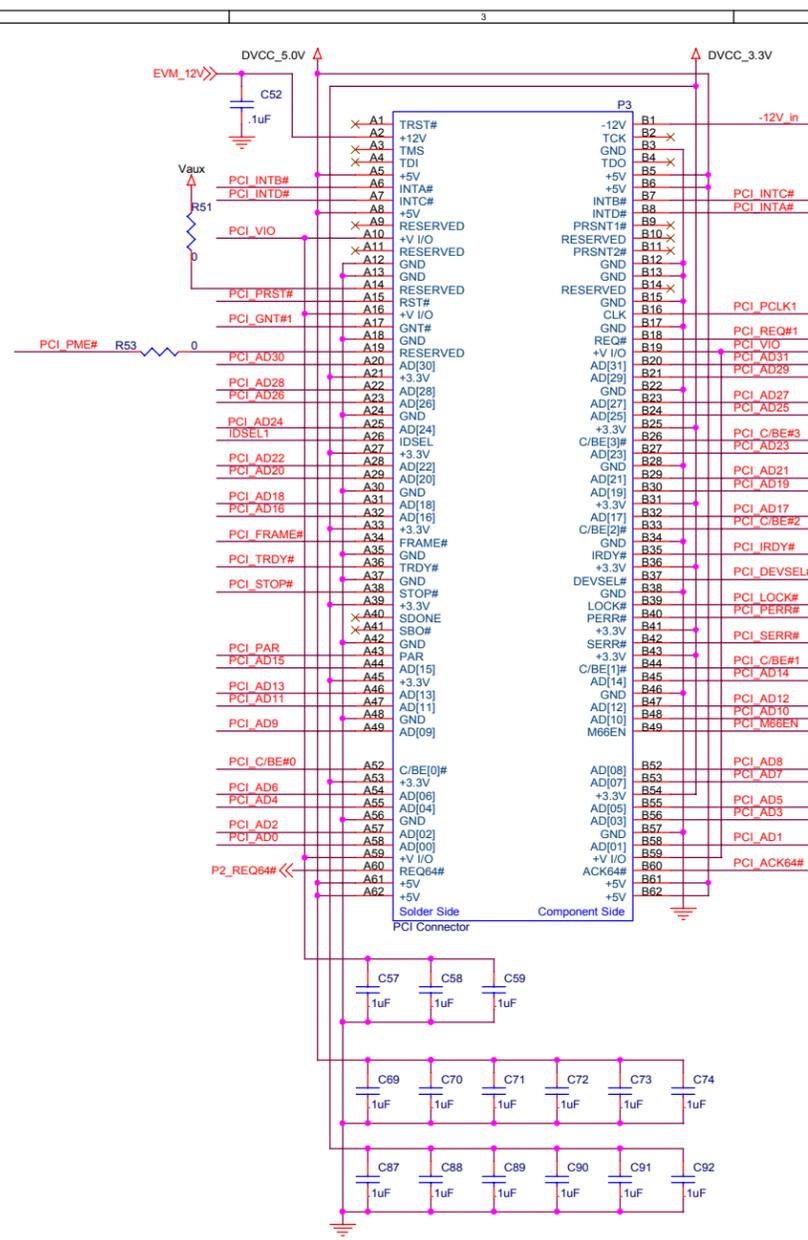
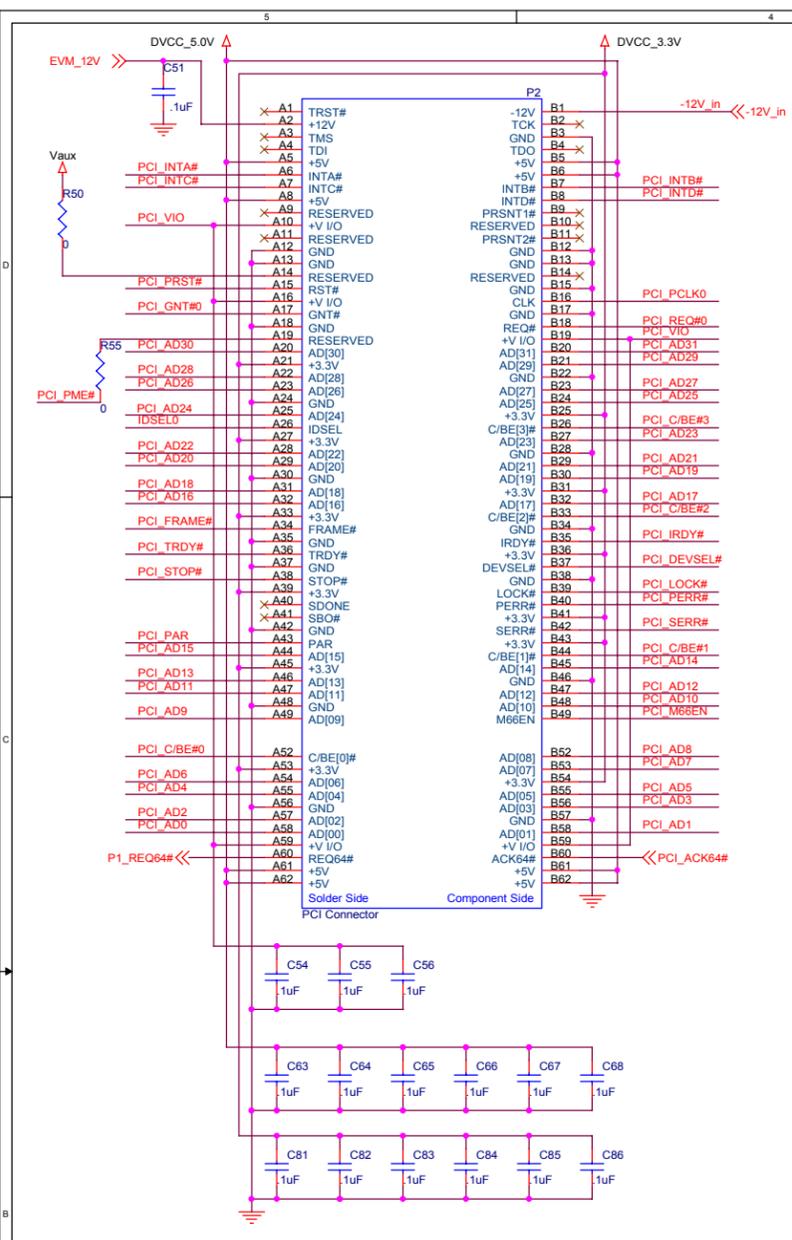
5V Step-Up Regulator (for PCI Slots)



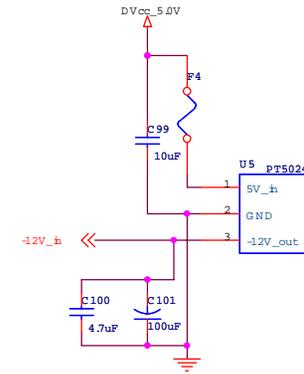
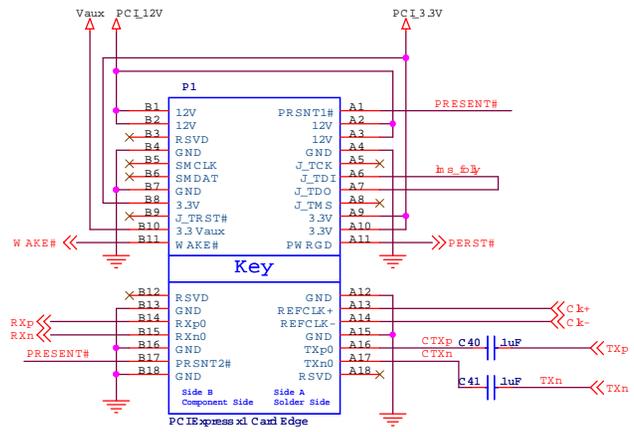
1.5V Regulator



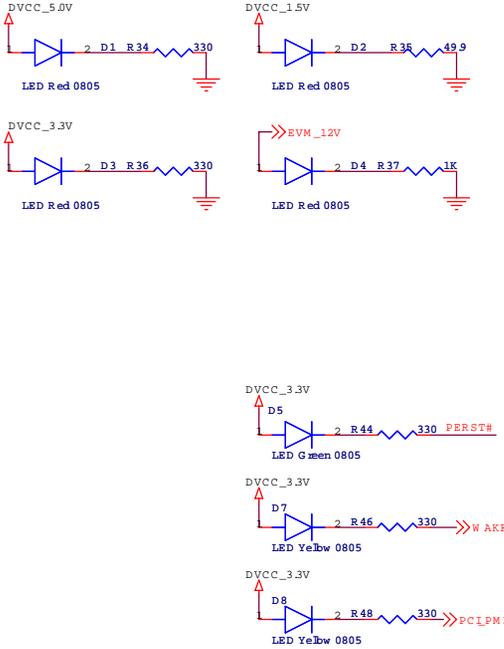
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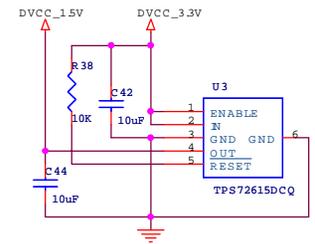
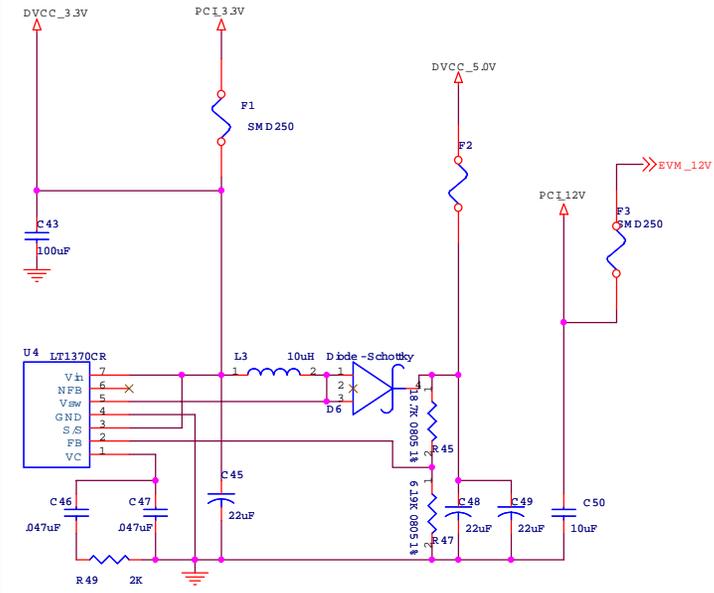
10 Reference Schematics ZHH Package



LEDs



Power



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Date:	Wednesday, June 20, 2007	Sheet	3 of 4

11 Reference Documents

1. PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0
2. PCI Express Base Specification, Revision 1.0a
3. PCI Express Card Electromechanical Specification, Revision 1.0a
4. PCI Local Bus Specification, Revision 2.3
5. PCI-to-PCI Bridge Architecture Specification, Revision 1.2
6. PCI Bus Power Management Interface Specification, Revision 1.1 or 1.2
7. PCI Mobile Design Guide, Revision 1.1
8. Serialized IRQ Support for PCI Systems, Revision 6.0
9. Express Card Standard, Release 1.0

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