

LMV721-N/LMV722 10MHz, Low Noise, Low Voltage, and Low Power Operational Amplifier

Check for Samples: [LMV721-N](#), [LMV722-N](#)

FEATURES

- (For Typical, 5 V Supply Values; Unless Otherwise Noted)
- Ensured 2.2V and 5.0V Performance
- Low Supply Current LMV721-N/2 930 μ A/Amplifier at 2.2V
- High Unity-Gain Bandwidth 10MHz
- Rail-to-Rail Output Swing
 - at 600 Ω Load 120mV from Either Rail at 2.2V
 - at 2k Ω Load 50mV from Either Rail at 2.2V
- Input Common Mode Voltage Range Includes Ground
- Silicon Dust, SC70-5 Package 2.0x2.0x1.0 mm
- Input Voltage Noise 9 nV/ $\sqrt{\text{Hz}}$ at f = 1KHz

APPLICATIONS

- Cellular an Cordless Phones
- Active Filter and Buffers
- Laptops and PDAs
- Battery Powered Electronics

Typical Application

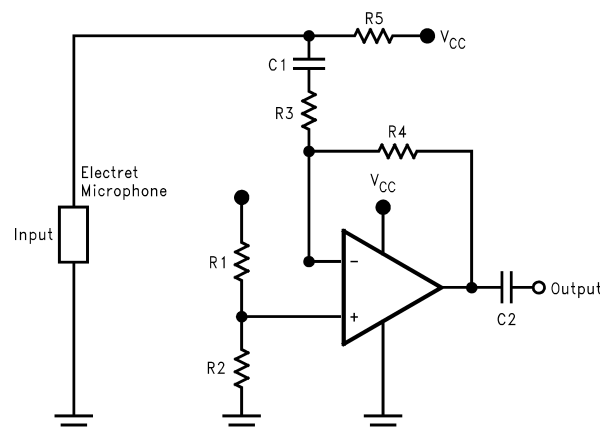


Figure 1. A Battery Powered Microphone Preamplifier



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1999–2013, Texas Instruments Incorporated

Absolute Maximum Ratings ⁽¹⁾⁽²⁾

ESD Tolerance ⁽³⁾	
Human Body Model	2000V
Machine Model	100V
Differential Input Voltage	± Supply Voltage
Supply Voltage ($V^+ - V^-$)	6V
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Storage Temp. Range	-65°C to 150°C
Junction Temperature ⁽⁴⁾	150°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Human body model, 1.5 k Ω in series with 100 pF. Machine model, 200 Ω in series with 100 pF.
- (4) The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Operating Ratings ⁽¹⁾

Supply Voltage	2.2V to 5.5V
Temperature Range	-40°C $\leq T_J \leq$ 85°C
Thermal Resistance (θ_{JA})	
Silicon Dust SC70-5 Pkg	440°C/W
Tiny SOT-23 package	265 °C/W
SOIC package, 8-pin Surface Mount	190°C/W
VSSOP package, 8-Pin Mini Surface Mount	235 °C/W
SOIC package, 14-Pin Surface Mount	145°C/W

- (1) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 30 mA over long term may adversely affect reliability.

2.2V DC Electrical Characteristics

Unless otherwise specified, all limits specified for $T_J = 25^\circ\text{C}$. $V^+ = 2.2\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V^+/2$, $V_O = V^+/2$ and $R_L > 1\text{M}\Omega$.

Boldface limits apply at the temperature extremes.

Parameter		Test Conditions	Typ ⁽¹⁾	Limit ⁽²⁾	Units
V_{OS}	Input Offset Voltage		0.02	3 3.5	mV max
TCV_{OS}	Input Offset Voltage Average Drift		0.6		$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current		260		nA
I_{OS}	Input Offset Current		25		nA
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{CM} \leq 1.3\text{V}$	88	70 64	dB min
PSRR	Power Supply Rejection Ratio	$2.2\text{V} \leq V^+ \leq 5\text{V}$, $V_O = 0$, $V_{CM} = 0$	90	70 64	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR \geq 50dB	-0.30		V
			1.3		V
A_V	Large Signal Voltage Gain	$R_L = 600\Omega$ $V_O = 0.75\text{V}$ to 2.00V	81	75 60	dB min
		$R_L = 2\text{k}\Omega$ $V_O = 0.50\text{V}$ to 2.10V	84	75 60	dB min

(1) Typical Values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

2.2V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for $T_J = 25^\circ\text{C}$. $V^+ = 2.2\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V^+/2$, $V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$.

Boldface limits apply at the temperature extremes.

Parameter		Test Conditions	Typ ⁽¹⁾	Limit ⁽²⁾	Units
V_O	Output Swing	$R_L = 600\Omega$ to $V^+/2$	2.125	2.090 2.065	V min
			0.071	0.120 0.145	V max
		$R_L = 2\text{k}\Omega$ to $V^+/2$	2.177	2.150 2.125	V min
			0.056	0.080 0.105	V max
I_O	Output Current	Sourcing, $V_O = 0\text{V}$ $V_{IN}(\text{diff}) = \pm 0.5\text{V}$	14.9	10.0 5.0	mA min
		Sinking, $V_O = 2.2\text{V}$ $V_{IN}(\text{diff}) = \pm 0.5\text{V}$	17.6	10.0 5.0	mA min
I_S	Supply Current	LMV721-N	0.93	1.2 1.5	mA max
		LMV722	1.81	2.2 2.6	

2.2V AC Electrical Characteristics

Unless otherwise specified, all limits specified for $T_J = 25^\circ\text{C}$. $V^+ = 2.2\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V^+/2$, $V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$.

Boldface limits apply at the temperature extremes.

Parameter		Test Conditions	Typ ⁽¹⁾	Units
SR	Slew Rate	⁽²⁾	4.9	V/ μs
GBW	Gain-Bandwidth Product		10	MHz
Φ_m	Phase Margin		67.4	Deg
G_m	Gain Margin		-9.8	dB
e_n	Input-Referred Voltage Noise	$f = 1\text{ kHz}$	9	nV/ $\sqrt{\text{Hz}}$
i_n	Input-Referred Current Noise	$f = 1\text{ kHz}$	0.3	pA/ $\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	$f = 1\text{ kHz}$ $A_V = 1$ $R_L = 600\Omega$, $V_O = 500\text{ mV}_{PP}$	0.004	%

(1) Typical Values represent the most likely parametric norm.

(2) Connected as voltage follower with 1V step input. Number specified is the slower of the positive and negative slew rate.

5V DC Electrical Characteristics

Unless otherwise specified, all limits specified for $T_J = 25^\circ\text{C}$. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V^+/2$, $V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$.

Boldface limits apply at the temperature extremes.

Parameter		Test Conditions	Typ ⁽¹⁾	Limit ⁽²⁾	Units
V_{OS}	Input Offset Voltage		-0.08	3 3.5	mV max
TCV_{OS}	Input Offset Voltage Average Drift		0.6		$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current		260		nA
I_{OS}	Input Offset Current		25		nA
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{CM} \leq 4.1\text{V}$	89	70 64	dB min
PSRR	Power Supply Rejection Ratio	$2.2\text{V} \leq V^+ \leq 5.0\text{V}$, $V_O = 0$ $V_{CM} = 0$	90	70 64	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR $\geq 50\text{dB}$	-0.30		V
			4.1		V

(1) Typical Values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

5V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for $T_J = 25^\circ\text{C}$. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V^+/2$, $V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$.

Boldface limits apply at the temperature extremes.

Parameter		Test Conditions	Typ ⁽¹⁾	Limit ⁽²⁾	Units
A_V	Large Signal Voltage Gain	$R_L = 600\Omega$ $V_O = 0.75\text{V to } 4.80\text{V}$	87	80 70	dB min
		$R_L = 2\text{k}\Omega$, $V_O = 0.70\text{V to } 4.90\text{V}$,	94	85 70	dB min
V_O	Output Swing	$R_L = 600\Omega$ to $V^+/2$	4.882	4.840 4.815	V min
			0.134	0.190 0.215	V max
		$R_L = 2\text{k}\Omega$ to $V^+/2$	4.952	4.930 4.905	V min
			0.076	0.110 0.135	V max
I_O	Output Current	Sourcing, $V_O = 0\text{V}$ $V_{IN}(\text{diff}) = \pm 0.5\text{V}$	52.6	25.0 12.0	mA min
		Sinking, $V_O = 5\text{V}$ $V_{IN}(\text{diff}) = \pm 0.5\text{V}$	23.7	15.0 8.5	mA min
I_S	Supply Current	LMV721-N	1.03	1.4 1.7	mA max
		LMV722	2.01	2.4 2.8	

5V AC Electrical Characteristics

Unless otherwise specified, all limits specified for $T_J = 25^\circ\text{C}$. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V^+/2$, $V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$.

Boldface limits apply at the temperature extremes.

Parameter		Test Conditions	Typ ⁽¹⁾	Units
SR	Slew Rate	(2)	5.25	V/ μs
GBW	Gain-Bandwidth Product		10.0	MHz
Φ_m	Phase Margin		72	Deg
G_m	Gain Margin		-11	dB
e_n	Input-Related Voltage Noise	$f = 1\text{ kHz}$	8.5	nV/ $\sqrt{\text{Hz}}$
i_n	Input-Referred Current Noise	$f = 1\text{ kHz}$	0.2	pa/ $\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	$f = 1\text{ kHz}$, $A_V = 1$ $R_L = 600\Omega$, $V_O = 1\text{ V}_{PP}$	0.001	%

(1) Typical Values represent the most likely parametric norm.

(2) Connected as voltage follower with 1V step input. Number specified is the slower of the positive and negative slew rate.

Typical Performance Characteristics

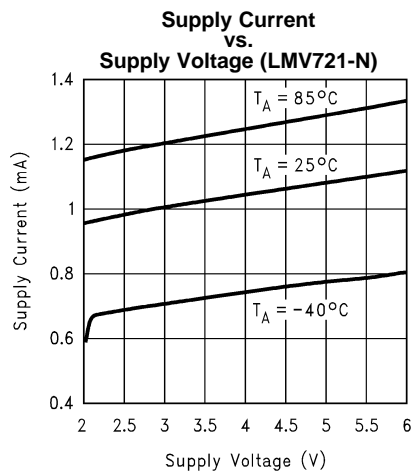


Figure 2.

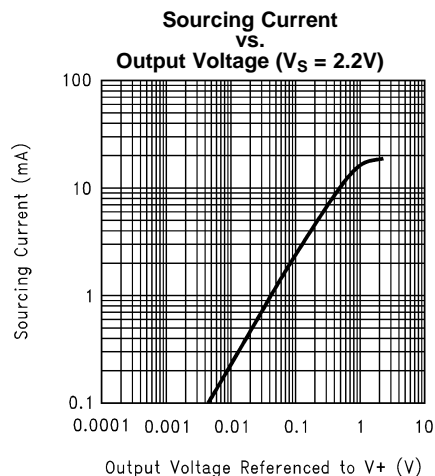


Figure 3.

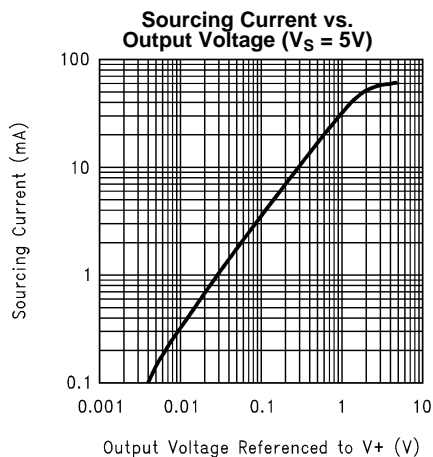


Figure 4.

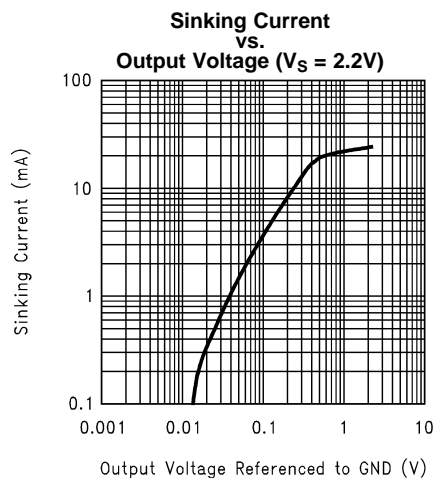


Figure 5.

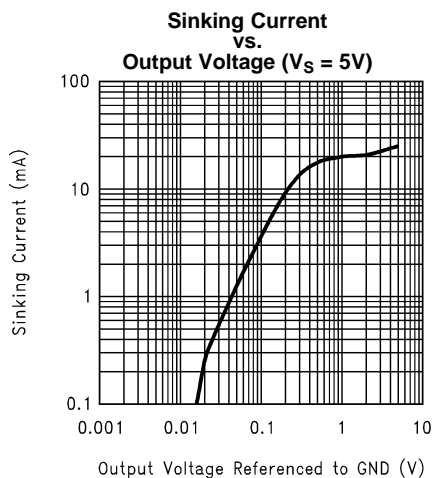


Figure 6.

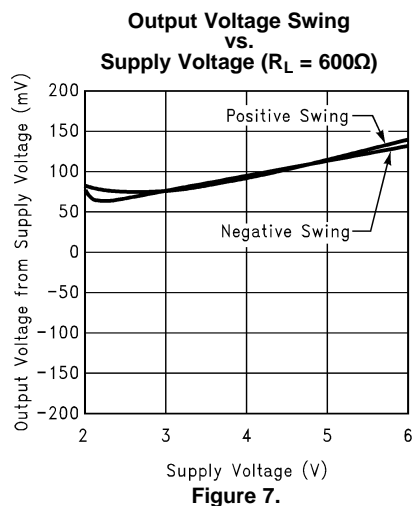
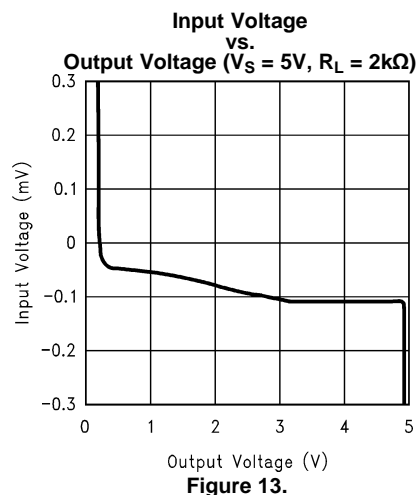
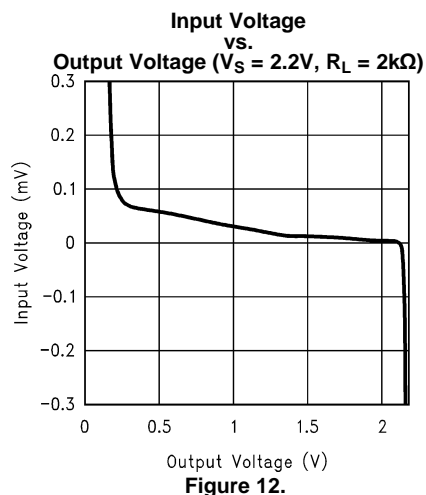
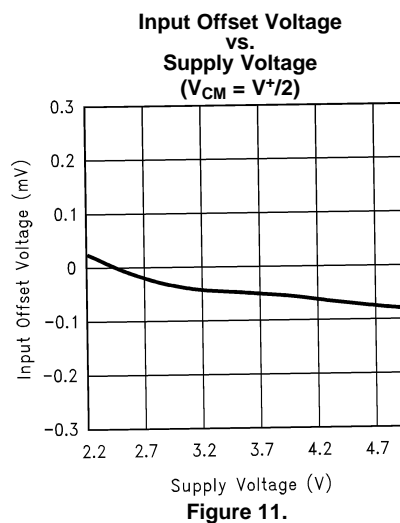
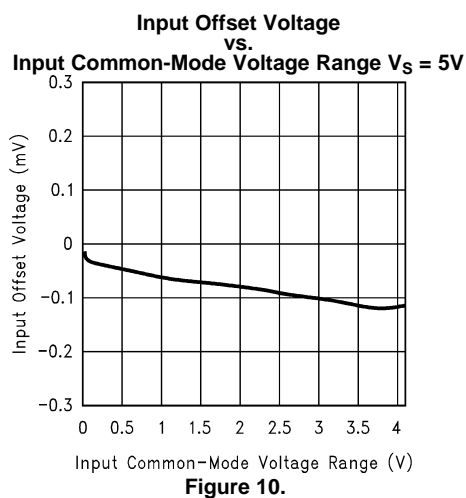
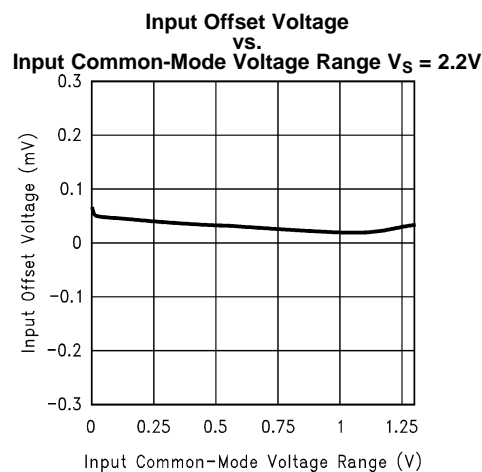
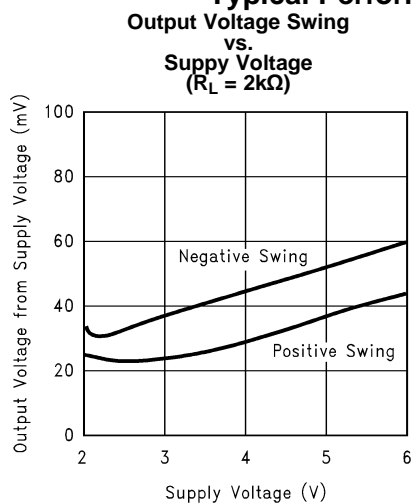


Figure 7.

Typical Performance Characteristics (continued)



Typical Performance Characteristics (continued)

**Input Voltage Noise
vs.
Frequency**

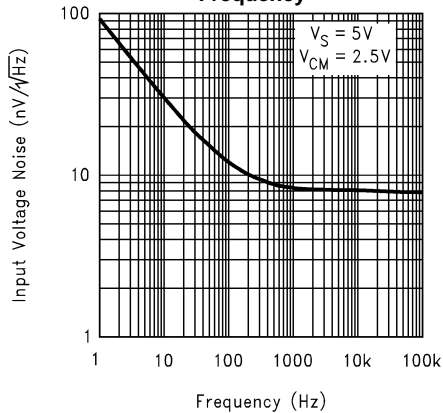


Figure 14.

**Input Current Noise
vs.
Frequency**

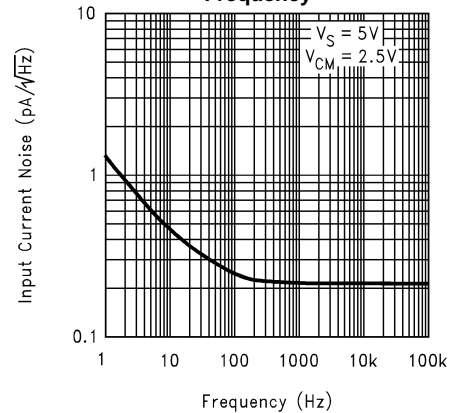


Figure 15.

**+PSRR
vs.
Frequency**

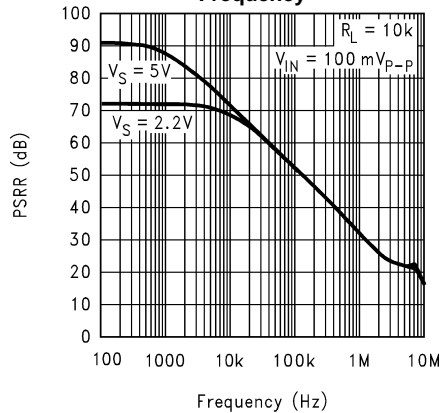


Figure 16.

**-PSRR
vs.
Frequency**

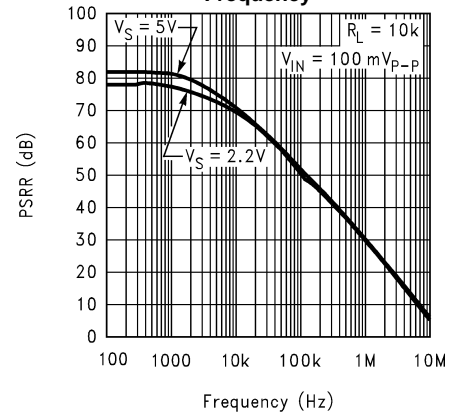


Figure 17.

**CMRR
vs.
Frequency**

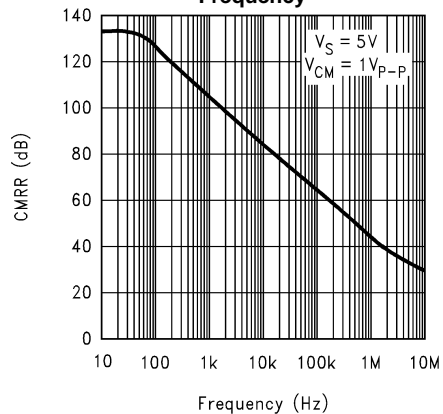


Figure 18.

**Gain and Phase Margin
vs.
Frequency
($V_S = 2.2V$, $R_L = 600\Omega$)**

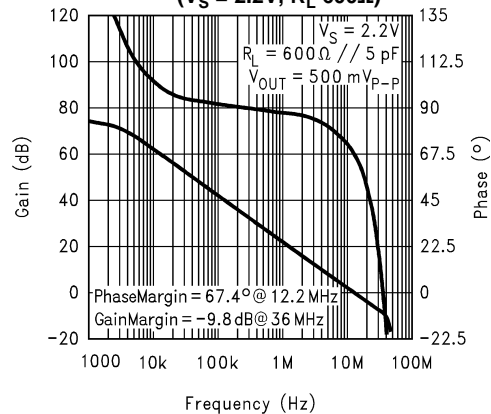
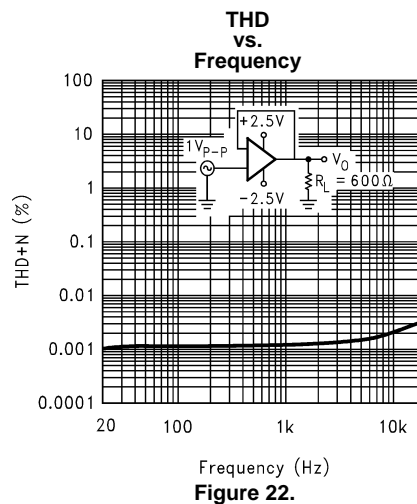
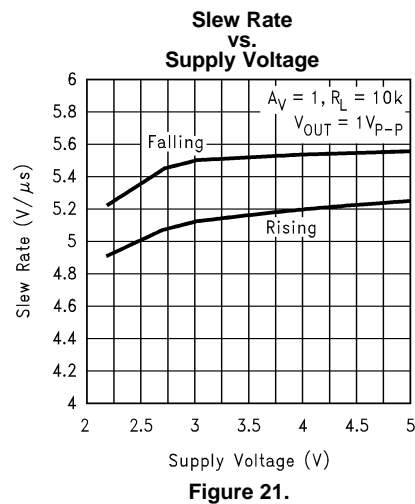
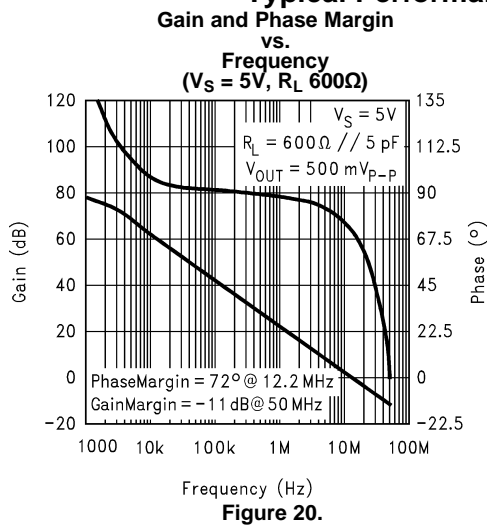


Figure 19.

Typical Performance Characteristics (continued)



APPLICATION NOTES

BENEFITS OF THE LMV721-N/722 SIZE

The small footprints of the LMV721-N/722 packages save space on printed circuit boards, and enable the design of smaller electronic products, such as cellular phones, pagers, or other portable systems. The low profile of the LMV721-N/722 make them possible to use in PCMCIA type III cards.

Signal Integrity Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the LMV721-N/722 can be placed closer to the signal source, reducing noise pickup and increasing signal integrity.

Simplified Board Layout These products help you to avoid using long pc traces in your pc board layout. This means that no additional components, such as capacitors and resistors, are needed to filter out the unwanted signals due to the interference between the long pc traces.

Low Supply Current These devices will help you to maximize battery life. They are ideal for battery powered systems.

Low Supply Voltage TI provides ensured performance at 2.2V and 5V. These specifications ensure operation throughout the battery lifetime.

Rail-to-Rail Output Rail-to-rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

Input Includes Ground Allows direct sensing near GND in single supply operation.

Protection should be provided to prevent the input voltages from going negative more than -0.3V (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

CAPACITIVE LOAD TOLERANCE

The LMV721-N/722 can directly drive 4700pF in unity-gain without oscillation. The unity-gain follower is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers. The combination of the amplifier's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation. To drive a heavier capacitive load, circuit in [Figure 23](#) can be used.

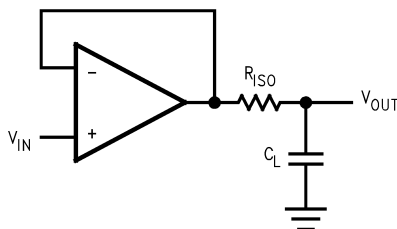


Figure 23. Indirectly Driving A capacitive Load Using Resistive Isolation

In [Figure 23](#), the isolation resistor R_{ISO} and the load capacitor C_L form a pole to increase stability by adding more phase margin to the overall system. the desired performance depends on the value of R_{ISO} . The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. [Figure 24](#) is an output waveform of [Figure 23](#) using $100\text{k}\Omega$ for R_{ISO} and $2000\mu\text{F}$ for C_L .

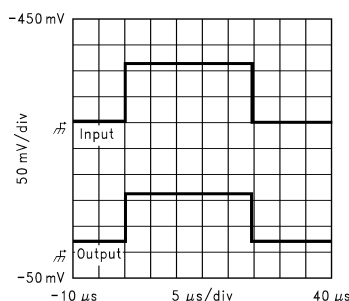


Figure 24. Pulse Response of the LMV721-N Circuit in Figure 23

The circuit in Figure 25 is an improvement to the one in Figure 23 because it provides DC accuracy as well as AC stability. If there were a load resistor in Figure 23, the output would be voltage divided by R_{ISO} and the load resistor. Instead, in Figure 25, R_F provides the DC accuracy by using feed-forward techniques to connect V_{IN} to R_L . Caution is needed in choosing the value of R_F due to the input bias current of the LMV721-N/722. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop. Increased capacitive drive is possible by increasing the value of C_F . This in turn will slow down the pulse response.

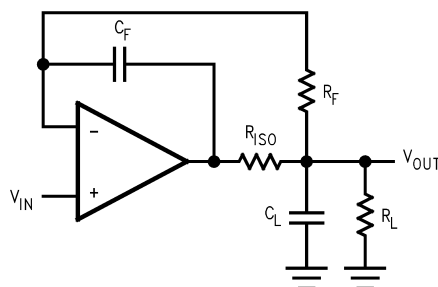


Figure 25. Indirectly Driving A Capacitive Load with DC Accuracy

INPUT BIAS CURRENT CANCELLATION

The LMV721-N/722 family has a bipolar input stage. The typical input bias current of LMV721-N/722 is 260nA with 5V supply. Thus a 100kΩ input resistor will cause 26mV of error voltage. By balancing the resistor values at both inverting and non-inverting inputs, the error caused by the amplifier's input bias current will be reduced. The circuit in Figure 26 shows how to cancel the error caused by input bias current.

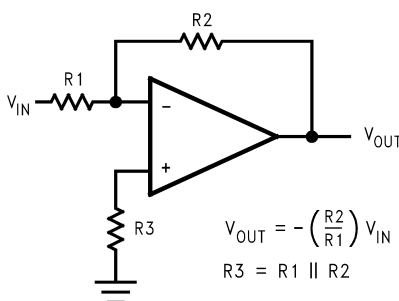


Figure 26. Cancelling the Error Caused by Input Bias Current

TYPICAL SINGLE-SUPPLY APPLICATION CIRCUITS

Difference Amplifier

The difference amplifier allows the subtraction of two voltages or, as a special case, the cancellation of a signal common to two inputs. It is useful as a computational amplifier, in making a differential to single-ended conversion or in rejecting a common mode signal.

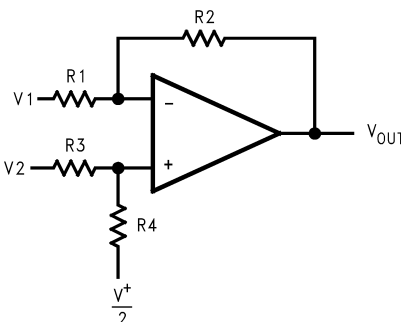


Figure 27. Difference Application

$$V_{OUT} = \left(\frac{R1+R2}{R3+R4} \right) \frac{R4}{R1} V_2 - \frac{R2}{R1} V_1 + \left(\frac{R1+R2}{R3+R4} \right) \frac{R3}{R1} \cdot \frac{V^+}{2}$$

for $R1 = R3$ and $R2 = R4$

$$V_{OUT} = \frac{R2}{R1} (V_2 - V_1) + \frac{V^+}{2}$$

(1)

(2)

Instrumentation Circuits

The input impedance of the previous difference amplifier is set by the resistor R_1 , R_2 , R_3 and R_4 . To eliminate the problems of low input impedance, one way is to use a voltage follower ahead of each input as shown in the following two instrumentation amplifiers.

Three-op-amp Instrumentation Amplifier

The LMV721-N/722 can be used to build a three-op-amp instrumentation amplifier as shown in [Figure 28](#)

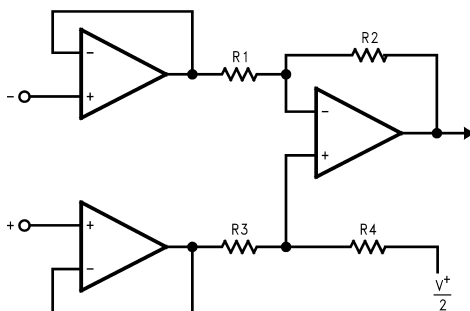


Figure 28. Three-op-amp Instrumentation Amplifier

The first stage of this instrumentation amplifier is a differential-input, differential-output amplifier, with two voltage followers. These two voltage followers assure that the input impedance is over 100MΩ. The gain of this instrumentation amplifier is set by the ratio of R_2/R_1 . R_3 should equal R_1 and R_4 equal R_2 . Matching of R_3 to R_1 and R_4 to R_2 affects the CMRR. For good CMRR over temperature, low drift resistors should be used. Making R_4 slightly smaller than R_2 and adding a trim pot equal to twice the difference between R_2 and R_4 will allow the CMRR to be adjusted for optimum.

Two-op-amp Instrumentation Amplifier

A two-op-amp instrumentation amplifier can also be used to make a high-input impedance DC differential amplifier (Figure 29). As in the two-op-amp circuit, this instrumentation amplifier requires precise resistor matching for good CMRR. R_4 should equal to R_1 and R_3 should equal R_2 .

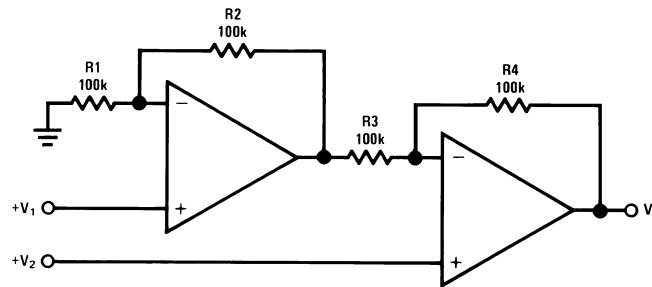


Figure 29. Two-op-amp Instrumentation Amplifier

$$V_O = \left(1 + \frac{R_4}{R_3}\right)(V_2 - V_1), \text{ where } R_1 = R_4 \text{ and } R_2 = R_3$$

$$\text{As shown: } V_O = 2(V_2 - V_1) \quad (3)$$

Single-Supply Inverting Amplifier

There may be cases where the input signal going into the amplifier is negative. Because the amplifier is operating in single supply voltage, a voltage divider using R_3 and R_4 is implemented to bias the amplifier so the input signal is within the input common-common voltage range of the amplifier. The capacitor C_1 is placed between the inverting input and resistor R_1 to block the DC signal going into the AC signal source, V_{IN} . The values of R_1 and C_1 affect the cutoff frequency, $f_c = \frac{1}{2\pi R_1 C_1}$.

As a result, the output signal is centered around mid-supply (if the voltage divider provides $V^+/2$ at the non-inverting input). The output can swing to both rails, maximizing the signal-to-noise ratio in a low voltage system.

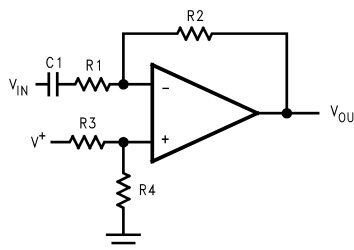


Figure 30. Single-Supply Inverting Amplifier

$$V_{OUT} = -\frac{R_2}{R_1} V_{IN} \quad (4)$$

Active Filter

Simple Low-Pass Active Filter

The simple low-pass filter is shown in Figure 31. Its low-pass frequency gain ($\omega \rightarrow 0$) is defined by $-R_3/R_1$. This allows low-frequency gains other than unity to be obtained. The filter has a -20dB/decade roll-off after its corner frequency f_c . R_2 should be chosen equal to the parallel combination of R_1 and R_3 to minimize error due to bias current. The frequency response of the filter is shown in Figure 32.

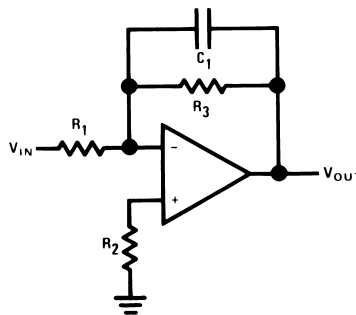


Figure 31. Simple Low-Pass Active Filter

$$A_L = -\frac{R_3}{R_1}$$

$$f_c = \frac{1}{2\pi R_3 C_1}$$

$$R_2 = R_1 \parallel R_3$$

(5)

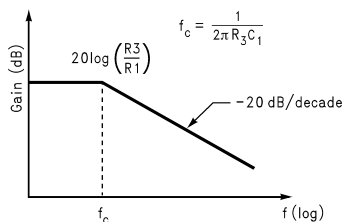


Figure 32. Frequency Response of Simple Low-pass Active Filter in Figure 31

Note that the single-op-amp active filters are used in to the applications that require low quality factor, $Q(\leq 10)$, low frequency ($\leq 5\text{KHz}$), and low gain (≤ 10), or a small value for the product of gain times $Q(\leq 100)$. The op amp should have an open loop voltage gain at the highest frequency of interest at least 50 times larger than the gain of the filter at this frequency. In addition, the selected op amp should have a slew rate that meets the following requirement:

$$\text{Slew Rate} \geq 0.5 \times (\omega_H V_{OPP}) \times 10^{-6} \text{V}/\mu\text{sec}$$

where

- ω_H is the highest frequency of interest
- V_{OPP} is the output peak-to-peak voltage

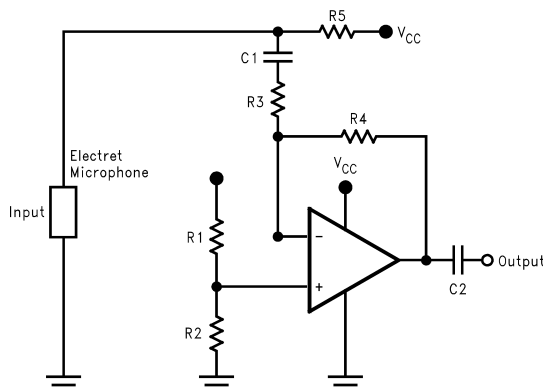


Figure 33. A Battery Powered Microphone Preamplifier

Here is a LMV721-N used as a microphone preamplifier. Since the LMV721-N is a low noise and low power op amp, it makes it an ideal candidate as a battery powered microphone preamplifier. The LMV721-N is connected in an inverting configuration. Resistors, $R_1 = R_2 = 4.7\text{k}\Omega$, sets the reference half way between $V_{CC} = 3\text{V}$ and ground. Thus, this configures the op amp for single supply use. The gain of the preamplifier, which is 50 (34dB), is set by resistors $R_3 = 10\text{k}\Omega$ and $R_4 = 500\text{k}\Omega$. The gain bandwidth product for the LMV721-N is 10 MHz. This is sufficient for most audio application since the audio range is typically from 20 Hz to 20kHz. A resistor $R_5 = 5\text{k}\Omega$ is used to bias the electret microphone. Capacitors $C_1 = C_2 = 4.7\mu\text{F}$ placed at the input and output of the op amp to block out the DC voltage offset.

Connection Diagrams

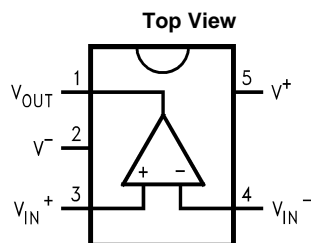


Figure 34. 5-Pin SC70 and SOT-23 Packages
See Package Numbers DCK0005A AND DBV0005A

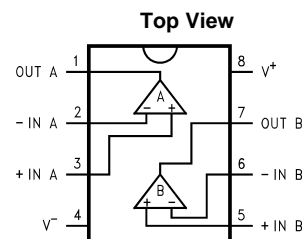


Figure 35. 8-Pin SOIC and VSSOP Packages
See Package Numbers D0008A and DGK0008A

REVISION HISTORY

Changes from Revision G (March 2013) to Revision H

Page

- Changed layout of National Data Sheet to TI format [14](#)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV721M5	LIFEBUY	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	A30A	
LMV721M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A30A	Samples
LMV721M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A30A	Samples
LMV721M7	LIFEBUY	SC70	DCK	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	A20	
LMV721M7/NOPB	ACTIVE	SC70	DCK	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A20	Samples
LMV721M7X/NOPB	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A20	Samples
LMV722M	LIFEBUY	SOIC	D	8	95	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	LMV 722M	
LMV722M/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMV 722M	Samples
LMV722MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	V722	Samples
LMV722MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	V722	Samples
LMV722MX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMV 722M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- ⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- ⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- ⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- ⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMV722-N :

- Automotive : [LMV722-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV721M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV721M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV721M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV721M7	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV721M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV721M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV722MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV722MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV722MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV721M5	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV721M5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV721M5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMV721M7	SC70	DCK	5	1000	208.0	191.0	35.0
LMV721M7/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0
LMV721M7X/NOPB	SC70	DCK	5	3000	208.0	191.0	35.0
LMV722MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMV722MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV722MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LMV722M	D	SOIC	8	95	495	8	4064	3.05
LMV722M	D	SOIC	8	95	495	8	4064	3.05
LMV722M/NOPB	D	SOIC	8	95	495	8	4064	3.05

DGK0008A**PACKAGE OUTLINE****VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

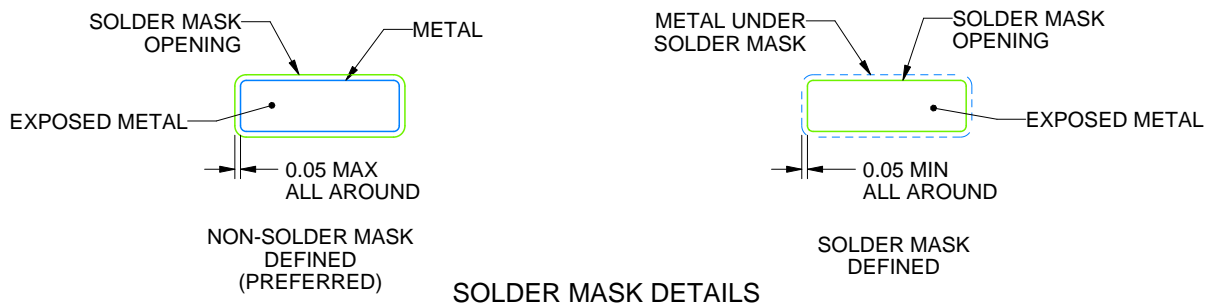
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

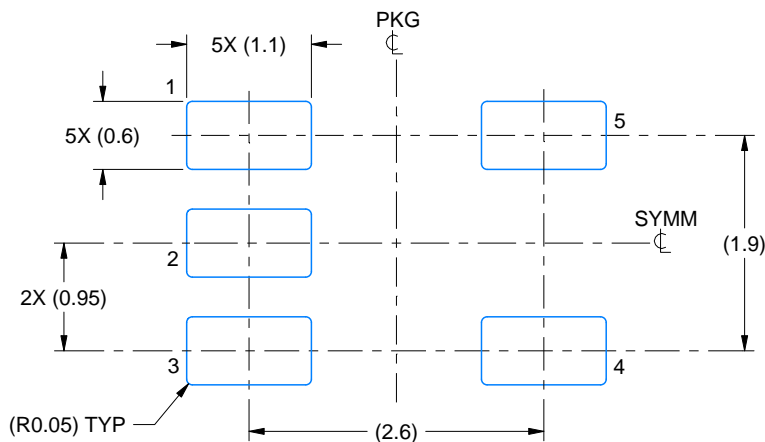
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

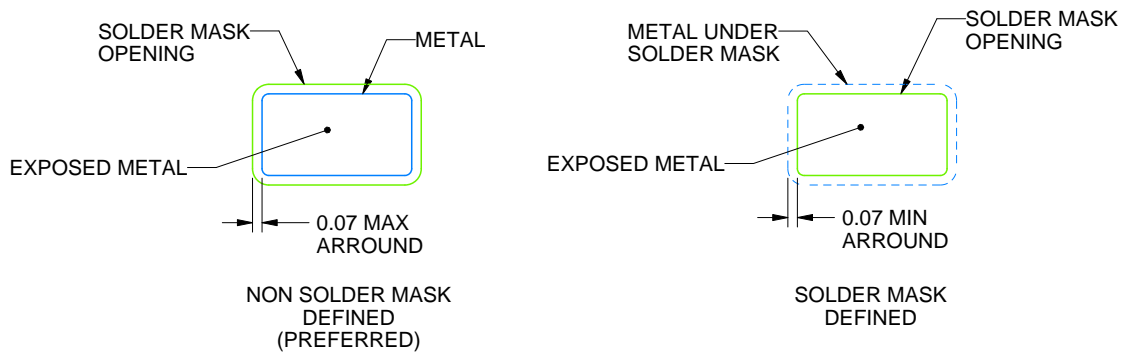
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



SOT - 1.1 max height

PIN 1 INDEX AREA

1.8

1.4

1.1

B

A

1

2X 0.65

1.3

2

NOTE 4

(0.15)

1.3

2.15

1.85

(0.1)

3

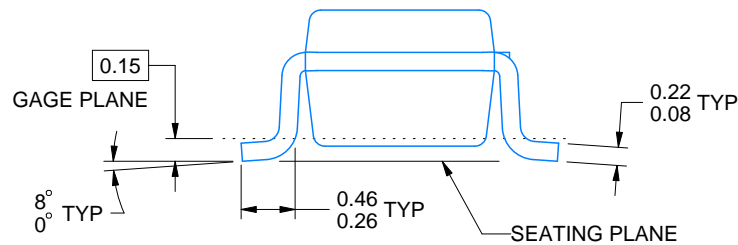
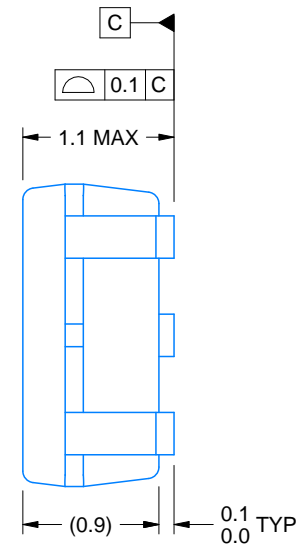
4

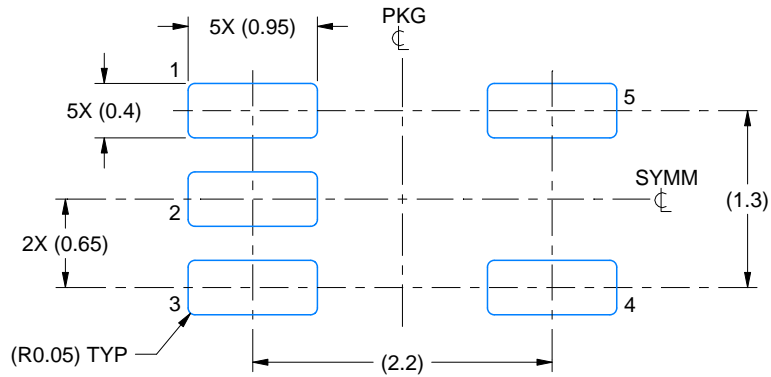
5

5X 0.33
0.15

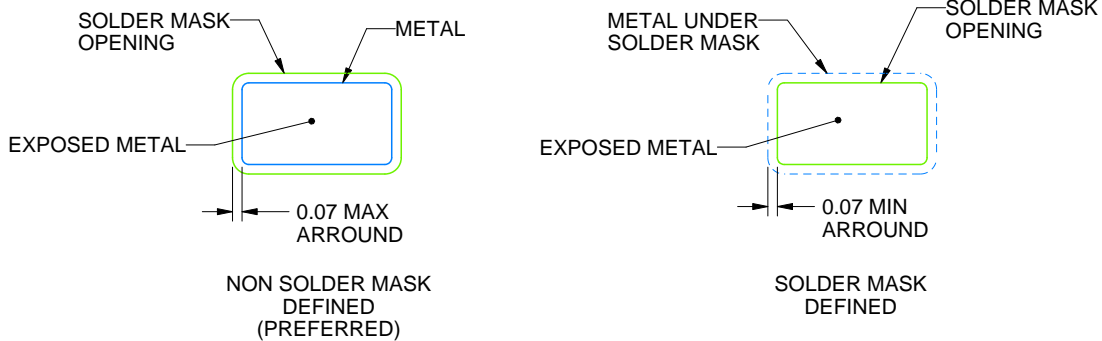
\oplus	0.1	M	C	A	B
----------	-----	---	---	---	---

NOTE 5





LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

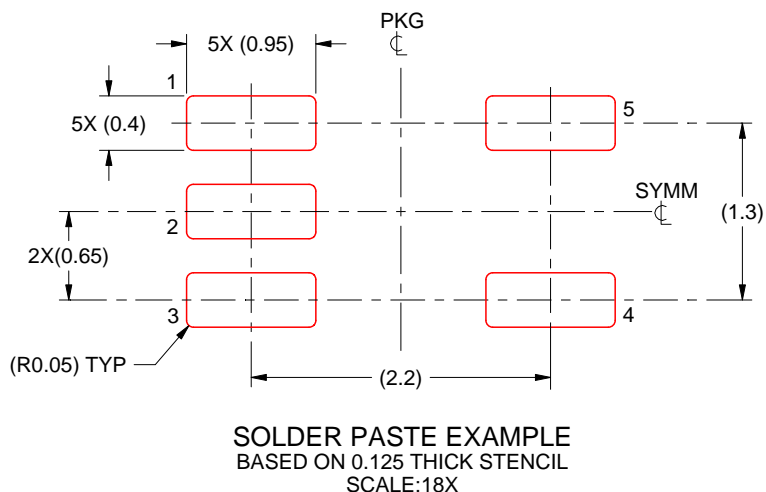


SOLDER MASK DETAILS

4214834/D 07/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



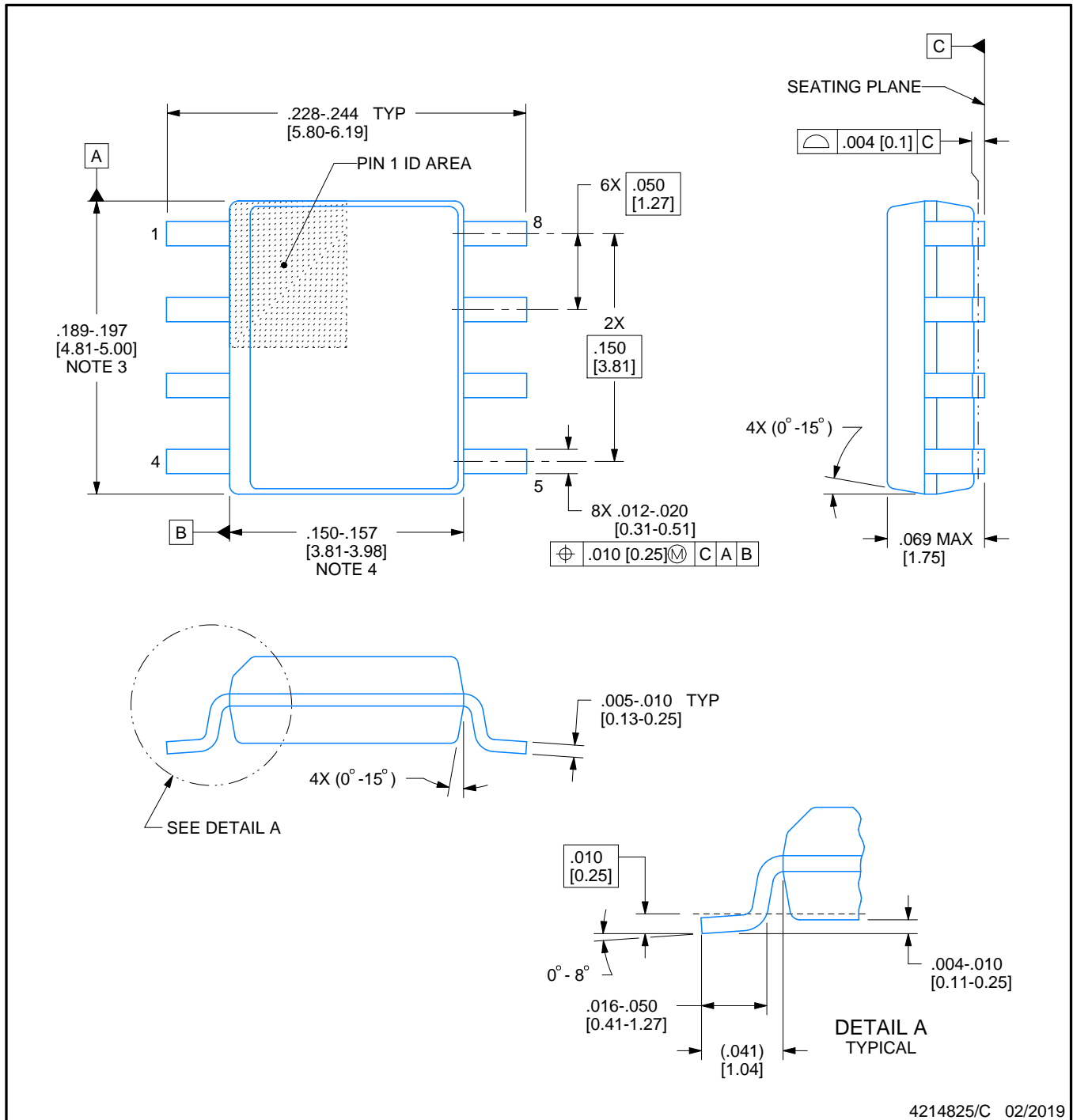
4214834/D 07/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D0008A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

D0008A

SOIC - 1.75 mm max height

Technical drawing of a mechanical part showing front and side views with dimensions and tolerances.

Front View (Left):

- Overall width: $8X (.061)$ [1.55]
- Overall height: $6X (.050)$ [1.27]
- Section line 1 is located at the top edge.
- Four rectangular features are arranged vertically, separated by dashed lines.

Side View (Right):

- Overall width: $(.213)$ [5.4]
- Section line 8 is located at the top edge.
- Four rectangular features are arranged vertically, separated by dashed lines.
- Feature 5 is indicated by a dimension line and the text $(R.002)$ TYP [0.05].

Annotations:

- SYMM** (Symmetry) is indicated on both the front and side views.
- SEE DETAILS** is indicated with an arrow pointing to the top edge of the side view.

4214825/C 02/2019

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated