# MC74HC4020A

# 14-Stage Binary Ripple Counter

## High−Performance Silicon−Gate CMOS

The MC74C4020A is identical in pinout to the standard CMOS MC14020B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of 14 master−slave flip−flops with 12 stages brought out to pins. The output of each flip−flop feeds the next and the frequency at each output is half of that of the preceding one. Reset is asynchronous and active−high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the HC4020A for some designs.

### Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With JEDEC Standard No. 7A Requirements
- Chip Complexity: 398 FETs or 99.5 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

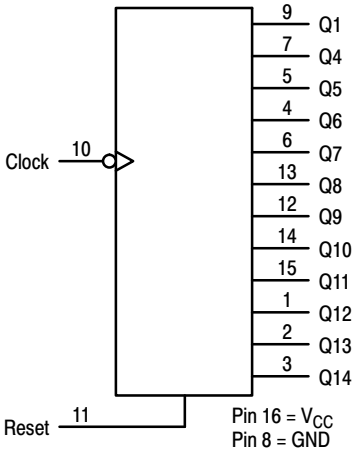
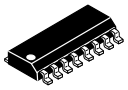


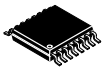

**Figure 1. Logic Diagram**

**ON Semiconductor®**

**http://onsemi.com**

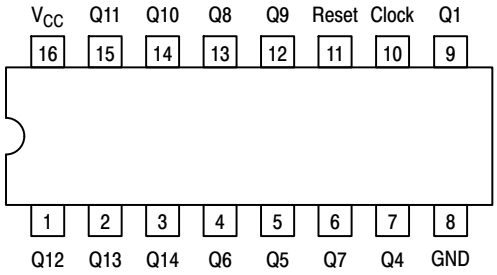


**SOIC−16**
**D SUFFIX**
**CASE 751B**



**TSSOP−16**
**DT SUFFIX**
**CASE 948F**

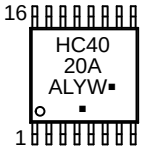
### PIN ASSIGNMENT




**16−Lead Package** (Top View)

### MARKING DIAGRAMS

**SOIC−16**




**TSSOP−16**

| | | |
|---|---|---|
| A | = | Assembly Location |
| L, WL | = | Wafer Lot |
| Y, YY | = | Year |
| W, WW | = | Work Week |
| G or ▪ | = | Pb−Free Package |

(Note: Microdot may be in either location)

### FUNCTION TABLE

| Clock | Reset | Output State |
|---|---|---|
| ⌐ | L | No Change |
| ¬ | L | Advance to Next State |
| X | H | All Outputs Are Low |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

© Semiconductor Components Industries, LLC, 2014

## MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | –0.5 to +7.0 | V |
| $V_{in}$ | DC Input Voltage (Referenced to GND) | –0.5 to $V_{CC}$ + 0.5 | V |
| $V_{out}$ | DC Output Voltage (Referenced to GND) | –0.5 to $V_{CC}$ + 0.5 | V |
| $I_{in}$ | DC Input Current, per Pin | ±20 | mA |
| $I_{out}$ | DC Output Current, per Pin | ±25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ±50 | mA |
| $P_D$ | Power Dissipation in Still Air SOIC Package† | 500 | mW |
| | TSSOP Package† | 450 | |
| $T_{stg}$ | Storage Temperature Range | –65 to + 150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds SOIC or TSSOP Package | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: –7 mW/°C from 65° to 125°C
TSSOP Package: −6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | | 2.0 | 6.0 | V |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature Range, All Package Types | | –55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise/Fall Time (Figure 2) | $V_{CC}$ = 2.0 V | 0 | 1000 | ns |
| | | $V_{CC}$ = 3.0 V | 0 | 600 | |
| | | $V_{CC}$ = 4.5 V | 0 | 500 | |
| | | $V_{CC}$ = 6.0 V | 0 | 400 | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Condition | $V_{CC}$ V | Guaranteed Limit −55 to 25°C | Guaranteed Limit ≤85°C | Guaranteed Limit ≤125°C | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High−Level Input Voltage | $V_{out}$ = 0.1V or $V_{CC}$ −0.1V<br>$\|I_{out}\| \le 20\mu A$ | 2.0 | 1.50 | 1.50 | 1.50 | V |
| | | | 3.0 | 2.10 | 2.10 | 2.10 | |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.20 | 4.20 | 4.20 | |
| $V_{IL}$ | Maximum Low−Level Input Voltage | $V_{out}$ = 0.1V or $V_{CC}$ − 0.1V<br>$\|I_{out}\| \le 20\mu A$ | 2.0 | 0.50 | 0.50 | 0.50 | V |
| | | | 3.0 | 0.90 | 0.90 | 0.90 | |
| | | | 4.5 | 1.35 | 1.35 | 1.35 | |
| | | | 6.0 | 1.80 | 1.80 | 1.80 | |
| $V_{OH}$ | Minimum High−Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\| \le 20\mu A$ | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | $V_{in}$ =$V_{IH}$ or $V_{IL}$ $\|I_{out}\| \le 2.4mA$ | 3.0 | 2.48 | 2.34 | 2.20 | |
| | | $\|I_{out}\| \le 4.0mA$ | 4.5 | 3.98 | 3.84 | 3.70 | |
| | | $\|I_{out}\| \le 5.2mA$ | 6.0 | 5.48 | 5.34 | 5.20 | |
| $V_{OL}$ | Maximum Low−Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\| \le 20\mu A$ | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$ $\|I_{out}\| \le 2.4mA$ | 3.0 | 0.26 | 0.33 | 0.40 | |
| | | $\|I_{out}\| \le 4.0mA$ | 4.5 | 0.26 | 0.33 | 0.40 | |
| | | $\|I_{out}\| \le 5.2mA$ | 6.0 | 0.26 | 0.33 | 0.40 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in}$ = $V_{CC}$ or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in}$ = $V_{CC}$ or GND<br>$I_{out}$ = 0μA | 6.0 | 4 | 40 | 160 | μA |

**AC CHARACTERISTICS** ($C_L$ = 50 pF, Input $t_r = t_f$ = 6 ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | −55 to 25°C | ≤85°C | ≤125°C | |
| $f_{max}$ | Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 5) | 2.0<br>3.0<br>4.5<br>6.0 | 10<br>15<br>30<br>50 | 9.0<br>14<br>28<br>50 | 8.0<br>12<br>25<br>40 | MHz |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Clock to Q1* (Figures 4 and 5) | 2.0<br>3.0<br>4.5<br>6.0 | 96<br>63<br>31<br>25 | 106<br>71<br>36<br>30 | 115<br>88<br>40<br>35 | ns |
| $t_{PHL}$ | Maximum Propagation Delay, Reset to Any Q (Figures 3 and 5) | 2.0<br>3.0<br>4.5<br>6.0 | 65<br>30<br>30<br>26 | 72<br>36<br>35<br>32 | 90<br>40<br>40<br>35 | ns |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Qn to Qn+1 (Figures 4 and 5) | 2.0<br>3.0<br>4.5<br>6.0 | 69<br>40<br>17<br>14 | 80<br>45<br>21<br>15 | 90<br>50<br>28<br>22 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, Any Output (Figures 2 and 5) | 2.0<br>3.0<br>4.5<br>6.0 | 75<br>27<br>15<br>13 | 95<br>32<br>19<br>15 | 110<br>36<br>22<br>19 | ns |
| $C_{in}$ | Maximum Input Capacitance | | 10 | 10 | 10 | pF |

* For $T_A$ = 25°C and $C_L$ = 50 pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:
$V_{CC}$ = 2.0 V: $t_P$ = [93.7 + 59.3 (n−1)] ns
$V_{CC}$ = 3.0 V: $t_P$ = [61.5 + 34.4 (n−1)] ns
$V_{CC}$ = 4.5 V: $t_P$ = [30.25 + 14.6 (n−1)] ns
$V_{CC}$ = 6.0 V: $t_P$ = [24.4 + 12 (n−1)] ns

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Package)* | 38 | pF |

**TIMING REQUIREMENTS** (Input $t_r = t_f$ = 6 ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | −55 to 25°C | ≤85°C | ≤125°C | |
| $t_{rec}$ | Minimum Recovery Time, Reset Inactive to Clock (Figure 3) | 2.0<br>3.0<br>4.5<br>6.0 | 30<br>20<br>5<br>4 | 40<br>25<br>8<br>6 | 50<br>30<br>12<br>9 | ns |
| $t_w$ | Minimum Pulse Width, Clock (Figure 2) | 2.0<br>3.0<br>4.5<br>6.0 | 70<br>40<br>15<br>13 | 80<br>45<br>19<br>16 | 90<br>50<br>24<br>20 | ns |
| $t_w$ | Minimum Pulse Width, Reset (Figure 3) | 2.0<br>3.0<br>4.5<br>6.0 | 70<br>40<br>15<br>13 | 80<br>45<br>19<br>16 | 90<br>50<br>24<br>20 | ns |
| $t_r$, $t_f$ | Maximum Input Rise and Fall Times (Figure 2) | 2.0<br>3.0<br>4.5<br>6.0 | 1000<br>800<br>500<br>400 | 1000<br>800<br>500<br>400 | 1000<br>800<br>500<br>400 | ns |

## PIN DESCRIPTIONS

### INPUTS

**Clock (Pin 10)**

Negative−edge triggering clock input. A high−to−low transition on this input advances the state of the counter.

**Reset (Pin 11)**

Active−high reset. A high level applied to this input asynchronously resets the counter to its zero state, thus forcing all Q outputs low.

### OUTPUTS

**Q1, Q4—Q14 (Pins 9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3)**

Active−high outputs. Each Qn output divides the Clock input frequency by $2^N$.

## SWITCHING WAVEFORMS

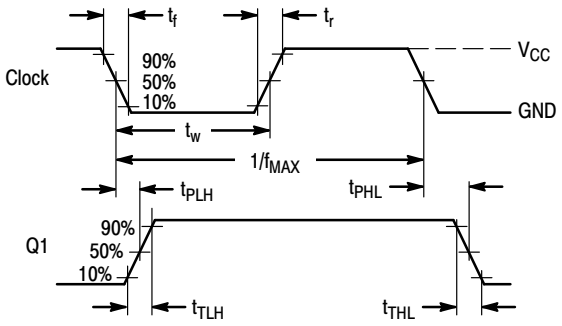



**Figure 2.**

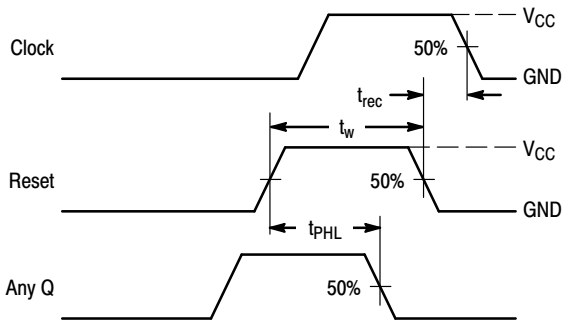



**Figure 3.**

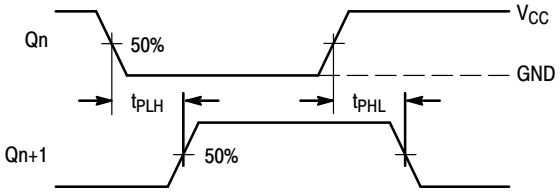
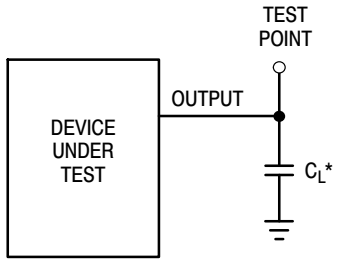



**Figure 4.**




*Includes all probe and jig capacitance

**Figure 5. Test Circuit**

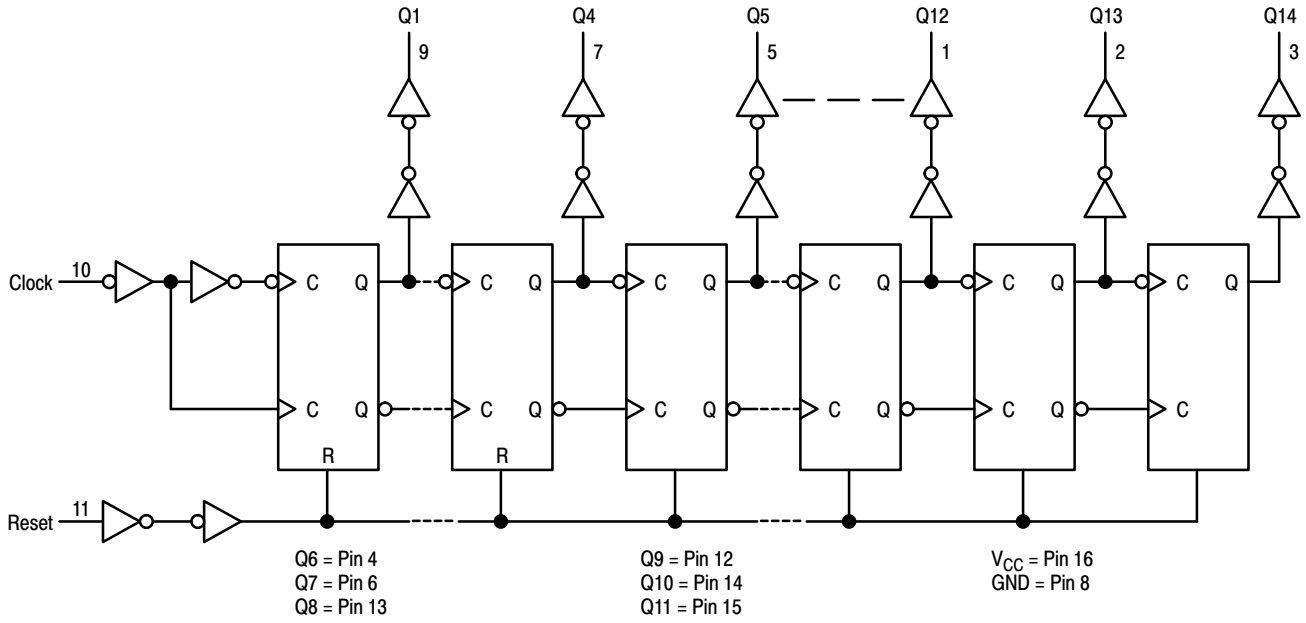



**Figure 6. Expanded Logic Diagram**

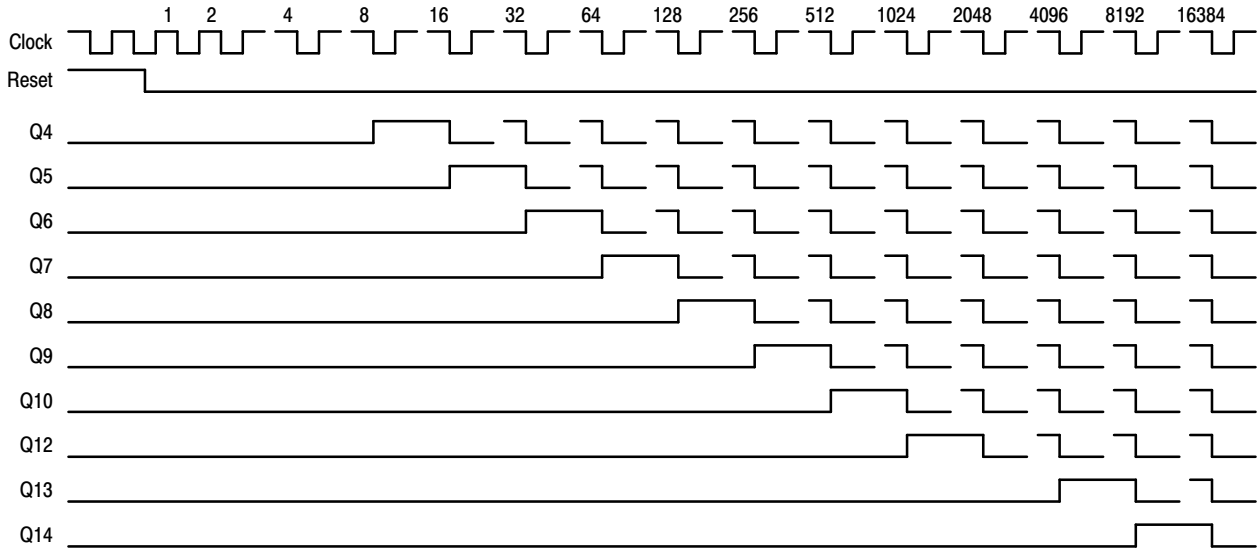



**Figure 7. Timing Diagram**

## APPLICATIONS INFORMATION

### Time−Base Generator

A 60Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the input of the MC54/74HC14A, Schmitt-trigger inverter. The HC14A squares−up the input waveform and feeds the HC4020A. Selecting outputs Q5, Q10, Q11, and Q12 causes a reset every 3600 clocks. The HC20 decodes the counter outputs, produces a single (narrow) output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.

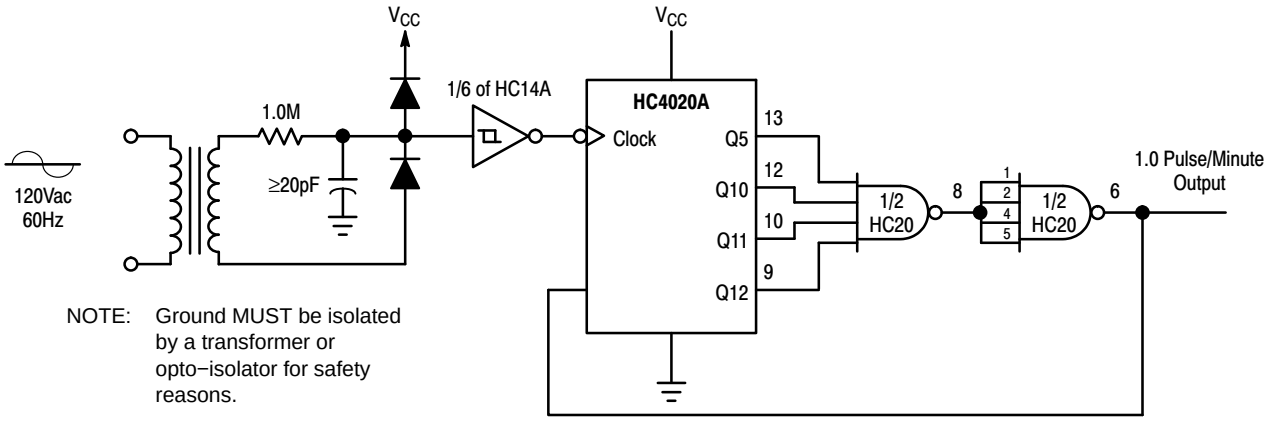



**Figure 8. Time−Base Generator**

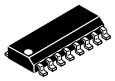
### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC74HC4020ADG | SOIC−16 (Pb−Free) | 48 Units / Rail |
| MC74HC4020ADR2G | SOIC−16 (Pb−Free) | 2500 / Tape & Reel |
| MC74HC4020ADTR2G | TSSOP−16 (Pb−Free) | 2500 / Tape & Reel |
| NLV74HC4020ADTR2G* | TSSOP−16 (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

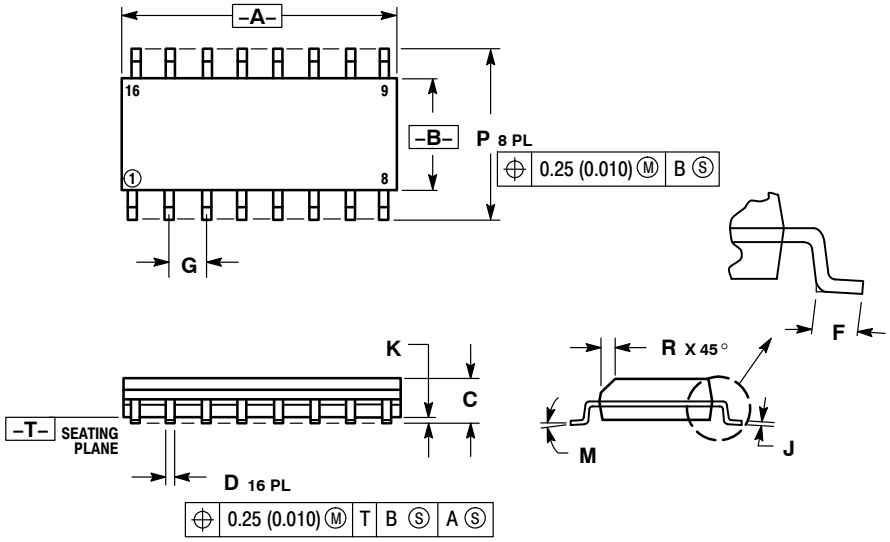
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS



SCALE 1:1

**SOIC−16**
CASE 751B−05
ISSUE K

DATE 29 DEC 2006




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

| STYLE 1: | |
|---|---|
| PIN 1. | COLLECTOR |
| 2. | BASE |
| 3. | EMITTER |
| 4. | NO CONNECTION |
| 5. | EMITTER |
| 6. | BASE |
| 7. | COLLECTOR |
| 8. | COLLECTOR |
| 9. | BASE |
| 10. | EMITTER |
| 11. | NO CONNECTION |
| 12. | EMITTER |
| 13. | BASE |
| 14. | COLLECTOR |
| 15. | EMITTER |
| 16. | COLLECTOR |

| STYLE 2: | |
|---|---|
| PIN 1. | CATHODE |
| 2. | ANODE |
| 3. | NO CONNECTION |
| 4. | CATHODE |
| 5. | CATHODE |
| 6. | NO CONNECTION |
| 7. | ANODE |
| 8. | CATHODE |
| 9. | CATHODE |
| 10. | ANODE |
| 11. | NO CONNECTION |
| 12. | CATHODE |
| 13. | CATHODE |
| 14. | NO CONNECTION |
| 15. | ANODE |
| 16. | CATHODE |

| STYLE 3: | |
|---|---|
| PIN 1. | COLLECTOR, DYE #1 |
| 2. | BASE, #1 |
| 3. | EMITTER, #1 |
| 4. | COLLECTOR, #1 |
| 5. | COLLECTOR, #2 |
| 6. | BASE, #2 |
| 7. | EMITTER, #2 |
| 8. | COLLECTOR, #2 |
| 9. | COLLECTOR, #3 |
| 10. | BASE, #3 |
| 11. | EMITTER, #3 |
| 12. | COLLECTOR, #3 |
| 13. | COLLECTOR, #4 |
| 14. | BASE, #4 |
| 15. | EMITTER, #4 |
| 16. | COLLECTOR, #4 |

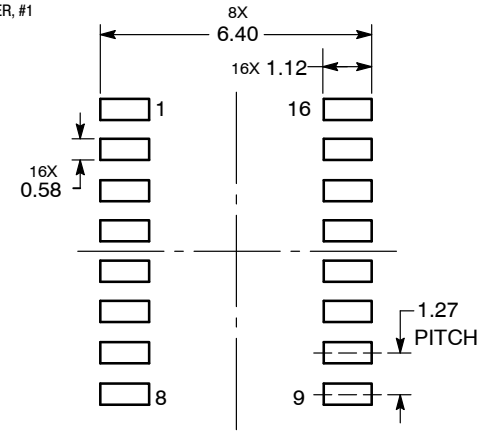
| STYLE 4: | |
|---|---|
| PIN 1. | COLLECTOR, DYE #1 |
| 2. | COLLECTOR, #1 |
| 3. | COLLECTOR, #2 |
| 4. | COLLECTOR, #2 |
| 5. | COLLECTOR, #3 |
| 6. | COLLECTOR, #3 |
| 7. | COLLECTOR, #4 |
| 8. | COLLECTOR, #4 |
| 9. | BASE, #4 |
| 10. | EMITTER, #4 |
| 11. | BASE, #3 |
| 12. | EMITTER, #3 |
| 13. | BASE, #2 |
| 14. | EMITTER, #2 |
| 15. | BASE, #1 |
| 16. | EMITTER, #1 |

| STYLE 5: | |
|---|---|
| PIN 1. | DRAIN, DYE #1 |
| 2. | DRAIN, #1 |
| 3. | DRAIN, #2 |
| 4. | DRAIN, #2 |
| 5. | DRAIN, #3 |
| 6. | DRAIN, #3 |
| 7. | DRAIN, #4 |
| 8. | DRAIN, #4 |
| 9. | GATE, #4 |
| 10. | SOURCE, #4 |
| 11. | GATE, #3 |
| 12. | SOURCE, #3 |
| 13. | GATE, #2 |
| 14. | SOURCE, #2 |
| 15. | GATE, #1 |
| 16. | SOURCE, #1 |

| STYLE 6: | |
|---|---|
| PIN 1. | CATHODE |
| 2. | CATHODE |
| 3. | CATHODE |
| 4. | CATHODE |
| 5. | CATHODE |
| 6. | CATHODE |
| 7. | CATHODE |
| 8. | CATHODE |
| 9. | ANODE |
| 10. | ANODE |
| 11. | ANODE |
| 12. | ANODE |
| 13. | ANODE |
| 14. | ANODE |
| 15. | ANODE |
| 16. | ANODE |

| STYLE 7: | |
|---|---|
| PIN 1. | SOURCE N-CH |
| 2. | COMMON DRAIN (OUTPUT) |
| 3. | COMMON DRAIN (OUTPUT) |
| 4. | GATE P-CH |
| 5. | COMMON DRAIN (OUTPUT) |
| 6. | COMMON DRAIN (OUTPUT) |
| 7. | COMMON DRAIN (OUTPUT) |
| 8. | SOURCE P-CH |
| 9. | SOURCE P-CH |
| 10. | COMMON DRAIN (OUTPUT) |
| 11. | COMMON DRAIN (OUTPUT) |
| 12. | COMMON DRAIN (OUTPUT) |
| 13. | GATE N-CH |
| 14. | COMMON DRAIN (OUTPUT) |
| 15. | COMMON DRAIN (OUTPUT) |
| 16. | SOURCE N-CH |

### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| DOCUMENT NUMBER: | 98ASB42566B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
|---|---|---|
| DESCRIPTION: | SOIC−16 | PAGE 1 OF 1 |

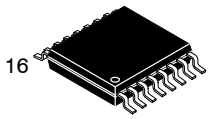
**onsemi** and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

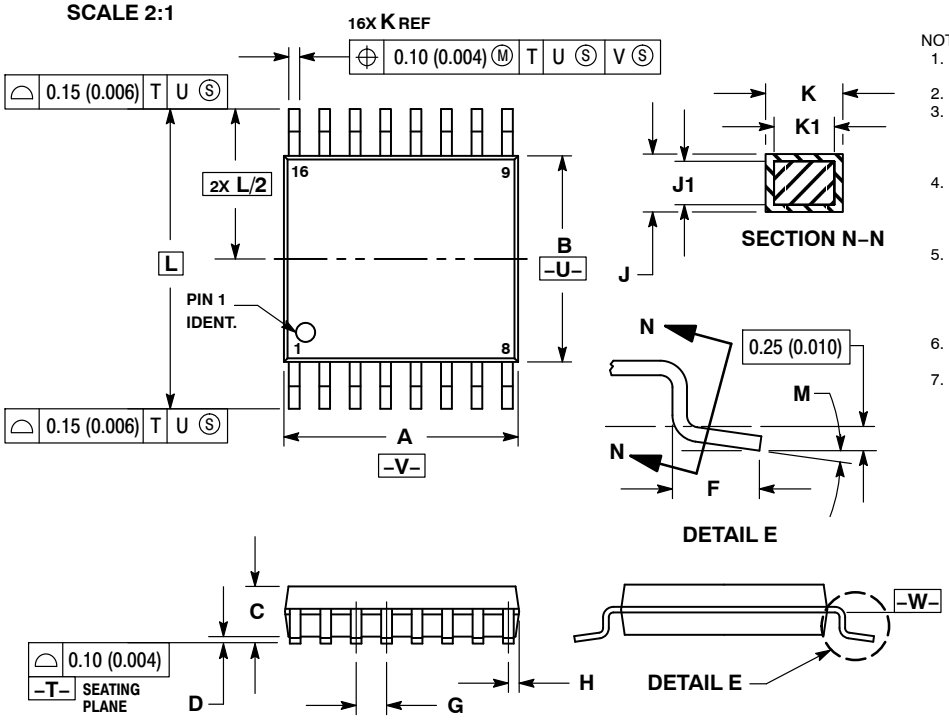
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**TSSOP−16 WB**
CASE 948F
ISSUE B

DATE 19 OCT 2006



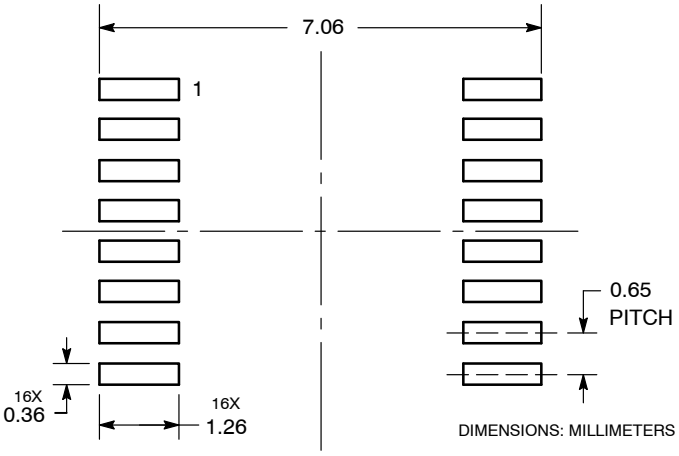

**SCALE 2:1**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

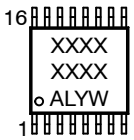
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

### RECOMMENDED SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




| | |
|---|---|
| XXXX | = Specific Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| G or ▪ | = Pb−Free Package |

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98ASH70247A** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. | |
| **DESCRIPTION:** | **TSSOP−16** | | **PAGE 1 OF 1** |

**onsemi** and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

**onsemi**, ONSEMI , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at**
www.onsemi.com/support/sales