

Octal 3-State Noninverting D Flip-Flop

High-Performance Silicon-Gate CMOS

MC74HC574A, MC74HCT574A

The MC74HC574A/MC74HCT574A is identical in pinout to the LS574. The MC74HC574A inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs. The MC74HCT574A may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

Data meeting the set-up time is clocked to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled.

The HC574A/HCT574A is identical in function to the HC374A/HCT374A but has the flip-flop inputs on the opposite side of the package from the outputs to facilitate PC board layout.

Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V (HC), 4.5 to 5.5 V (HCT)
- Low Input Current: 1.0 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 286 FETs or 71.5 Equivalent Gates
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

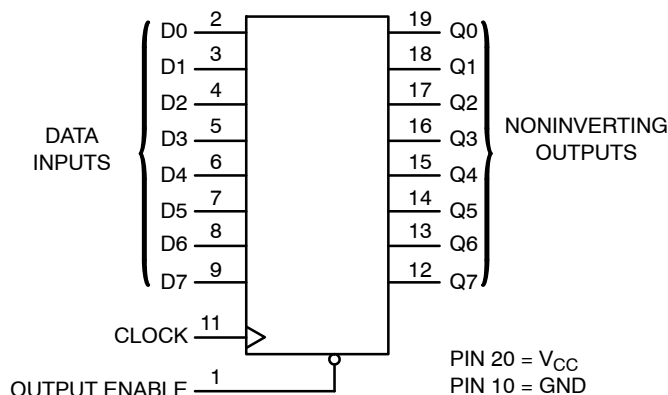
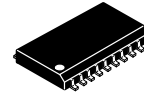


Figure 1. Logic Diagram

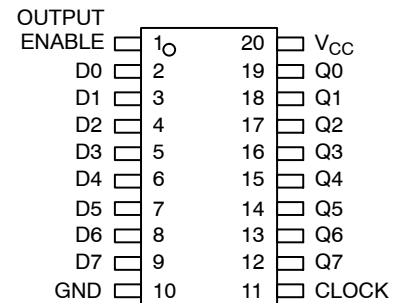


SOIC-20
DW SUFFIX
CASE 751D

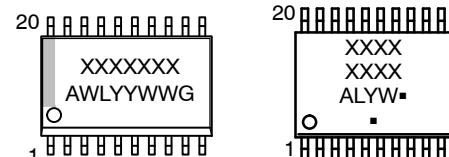


TSSOP-20
DT SUFFIX
CASE 948E

PIN ASSIGNMENT



MARKING DIAGRAMS



SOIC-20

XXXXXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

TSSOP-20

(Note: Microdot may be in either location)

FUNCTION TABLE

Inputs			Output
OE	Clock	D	Q
L	↗	H	H
L	↗	L	L
L	L, H, ↗	X	No Change
H	X	X	Z

X = Don't Care

Z = High Impedance

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

MC74HC574A, MC74HCT574A

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	−0.5 to +6.5	V
V _{IN}	DC Input Voltage	−0.5 to V _{CC} +0.5	V
V _{OUT}	DC Output Voltage	−0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Diode Current, per Pin	±20	mA
I _{OUT}	DC Input Diode Current, Per Pin	±35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
I _{IK}	Input Clamp Current (V _{IN} < 0 or V _{IN} > V _{CC})	±20	mA
I _{OK}	Output Clamp Current (V _{OUT} < 0 or V _{OUT} > V _{CC})	±20	mA
T _{STG}	Storage Temperature Range	−65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 secs	260	°C
T _J	Junction Temperature Under Bias	+150	°C
θ _{JA}	Thermal Resistance (Note 1) SOIC−20W WQFN20 QFN20 TSSOP−20	96 99 111 150	°C/W
P _D	Power Dissipation in Still Air at 25°C SOIC−20W WQFN20 QFN20 TSSOP−20	1302 1256 1127 833	mW
MSL	Moisture Sensitivity	Level 1	–
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	–
V _{ESD}	ESD Withstand Voltage (Note 2) Human Body Model Charged Device Model	> 4000 > 1000	V
I _{LATCHUP}	Latchup Performance (Note 3)	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.
3. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
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MC74HC

V _{CC}	DC Supply Voltage	2.0	6.0	V	
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Note 4)	0	V _{CC}	V	
T _A	Operating Free–Air Temperature	–55	+125	°C	
t _r , t _f	Input Rise or Fall Time	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

MC74HCT

V_{CC}	DC Supply Voltage	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Note 4)	0	V_{CC}	V
T_A	Operating Free-Air Temperature	-55	+125	°C
t_r, t_f	Input Rise or Fall Time	0	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

MC74HC574A, MC74HCT574A

DC ELECTRICAL CHARACTERISTICS (MC74HC574A)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				-55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V I _{out} ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} I _{out} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} I _{out} ≤ 2.4 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	V
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	6.0	±0.5	±5.0	±10	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	4.0	40	160	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

MC74HC574A, MC74HCT574A

AC ELECTRICAL CHARACTERISTICS (MC74HC574A)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55 to 25°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 3)	2.0 3.0 4.5 6.0	6.0 15 30 35	4.8 10 24 28	4.0 8.0 20 24	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q (Figures 2 and 3)	2.0 3.0 4.5 6.0	160 105 32 27	200 145 40 34	240 190 48 41	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 4)	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 4)	2.0 3.0 4.5 6.0	140 90 28 24	175 120 35 30	210 140 42 36	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, any Output (Figures 2 and 3)	2.0 3.0 4.5 6.0	60 27 12 10	75 32 15 13	90 36 18 15	ns
C _{in}	Maximum Input Capacitance		10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance, Output in High-Impedance State		15	15	15	pF

C _{PD}	Power Dissipation Capacitance (Per Enabled Output)*	Typical @ 25°C, V _{CC} = 5.0 V	pF
		24	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS (MC74HC574A)

Symbol	Parameter	Figure	V _{CC} V	Guaranteed Limit						Unit
				−55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
t _{su}	Minimum Setup Time, Data to Clock	5	2.0 3.0 4.6 6.0	50 40 10 9.0		65 50 13 11		75 60 15 13		ns
t _h	Minimum Hold Time, Clock to Data	5	2.0 3.0 4.5 6.0	5.0 5.0 5.0 5.0		5.0 5.0 5.0 5.0		5.0 5.0 5.0 5.0		ns
t _w	Minimum Pulse Width, Clock	3	2.0 3.0 4.5 6.0	75 60 15 13		95 80 19 16		110 90 22 19		ns
t _r , t _f	Maximum Input Rise and Fall Times	3	2.0 3.0 4.5 6.0		1000 800 500 400		1000 800 500 400		1000 800 500 400	ns

MC74HC574A, MC74HCT574A

DC ELECTRICAL CHARACTERISTICS (MC74HCT574A)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High–Level Input Voltage	V _{out} = 0.1 V or V _{CC} – 0.1 V I _{out} ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V _{IL}	Maximum Low–Level Input Voltage	V _{out} = 0.1 V or V _{CC} – 0.1 V I _{out} ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V _{OH}	Minimum High–Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA	4.5	3.98	3.84	3.7	
V _{OL}	Maximum Low–Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA	4.5	0.26	0.33	0.4	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	5.5	4.0	40	160	μA
I _{OZ}	Maximum Three–State Leakage Current	V _{in} = V _{IL} or V _{IH} (Note 1) V _{out} = V _{CC} or GND	5.5	–0.5	–5.0	–10	μA

ΔI _{CC}	Additional Quiescent Supply Current	V _{in} = 2.4 V, Any One Input V _{in} = V _{CC} or GND, Other Inputs I _{out} = 0 μA	5.5	≥ –55°C	25°C to 125°C		mA
				2.9	2.4		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Output in high-impedance state.

MC74HC574A, MC74HCT574A

AC ELECTRICAL CHARACTERISTICS (MC74HCT574A)

Symbol	Parameter	Guaranteed Limit			Unit
		-55 to 25°C	≤ 85°C	≤ 125°C	
f _{MAX}	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 3)	30	24	20	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q (Figures 2 and 3)	30	38	45	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 4)	28	35	42	ns
t _{PZH} , t _{PZL}	Maximum Propagation Delay Time, Output Enable to Q (Figures 2 and 4)	28	35	42	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 3)	12	15	18	ns
C _{in}	Maximum Input Capacitance	10	10	10	pF

C _{PD}	Power Dissipation Capacitance (Per Flip-Flop)*	Typical @ 25°C, V _{CC} = 5.0 V	pF
		58	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS (MC74HCT574A)

Symbol	Parameter	Figure	Guaranteed Limit						Unit
			−55 to 25°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
t _{su}	Minimum Setup Time, Data to Clock	5	10		13		15		ns
t _h	Minimum Hold Time, Clock to Data	5	5.0		5.0		5.0		ns
t _w	Minimum Pulse Width, Clock	3	15		19		22		ns
t _r , t _f	Maximum Input Rise and Fall Times	3		500		500		500	ns

MC74HC574A, MC74HCT574A

SWITCHING WAVEFORMS

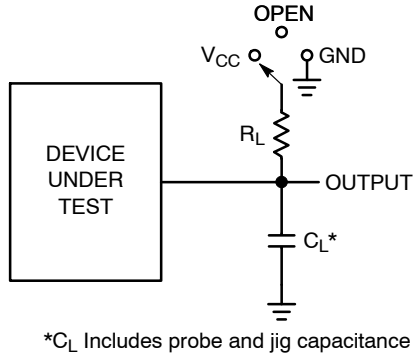


Figure 2. Test Circuit

Test	Switch Position	C _L	R _L
t _{PLH} / t _{PHL}	Open	50 pF	1 kΩ
t _{PLZ} / t _{PZL}	V _{CC}		
t _{PHZ} / t _{PZH}	GND		

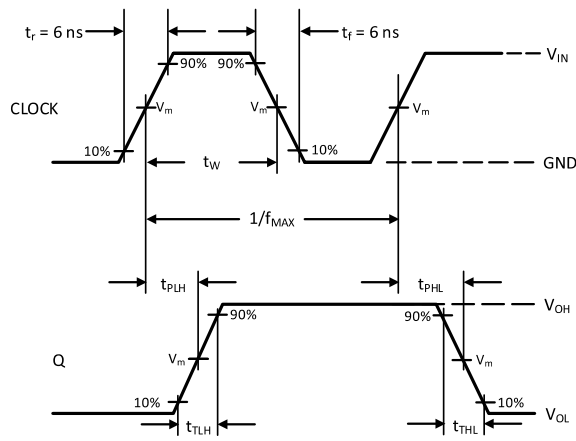


Figure 3.

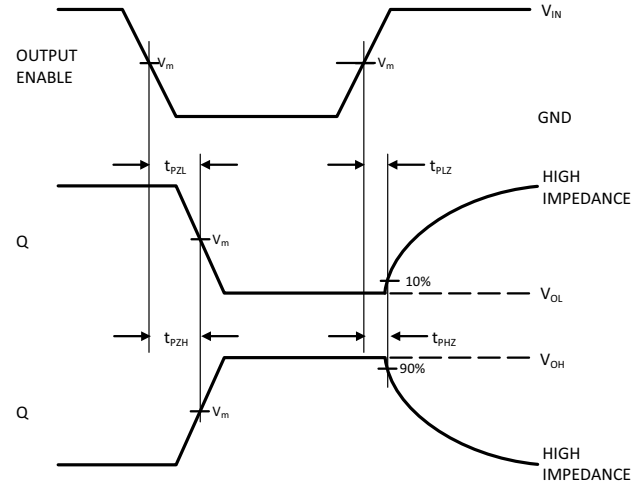


Figure 4.

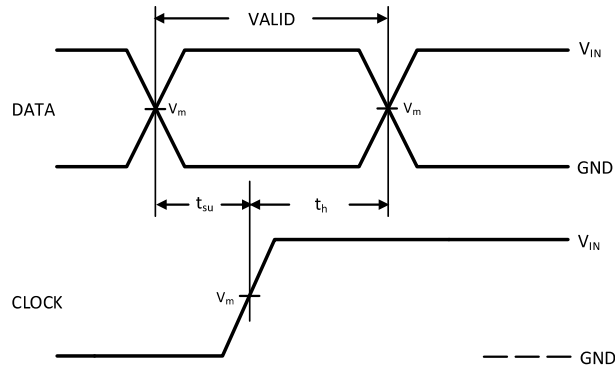


Figure 5.

Device	V _{IN} , V	V _m , V
MC74HC574A	V _{CC}	50% x V _{CC}
MC74HCT574A	3 V	1.3 V

MC74HC574A, MC74HCT574A

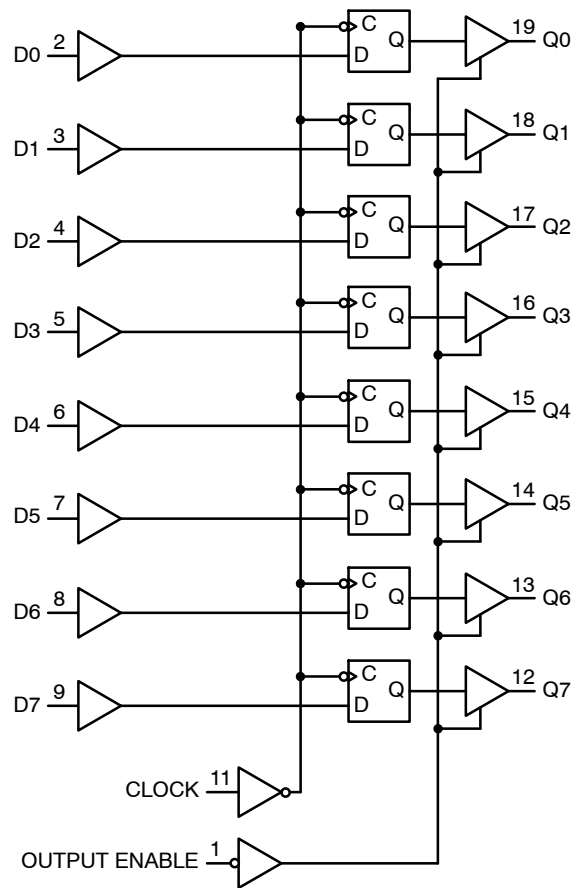


Figure 6. Expanded Logic Diagram

ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
MC74HC574ADWG	HC574A	SOIC-20 Wide	38 Units / Rail
MC74HC574ADWR2G	HC574A	SOIC-20 Wide	1000 Units / Tape & Reel
MC74HC574ADWR2G-Q*	HC574A	SOIC-20 Wide	1000 Units / Tape & Reel
MC74HC574ADTR2G	HC 574A	TSSOP-20	2500 Units / Tape & Reel
MC74HC574ADTR2G-Q*	HC 574A	TSSOP-20	2500 Units / Tape & Reel
MC74HCT574ADWG	HCT574A	SOIC-20 Wide	38 Units / Rail
MC74HCT574ADWR2G	HCT574A	SOIC-20 Wide	1000 Units / Tape & Reel
MC74HCT574ADWR2G-Q*	HCT574A	SOIC-20 Wide	1000 Units / Tape & Reel
MC74HCT574ADTR2G	HCT 574A	TSSOP-20	2500 Units / Tape & Reel
MC74HCT574ADTR2G-Q*	HCT 574A	TSSOP-20	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

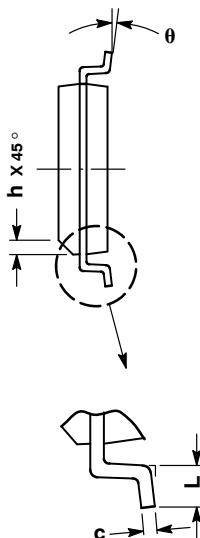
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

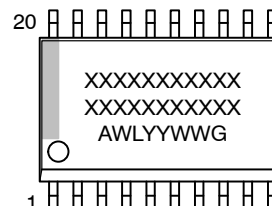


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®

ON



SCALE 2:1

TSSOP-20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC MARKING DIAGRAM*



- A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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DESCRIPTION: TSSOP-20 WB

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