

MC74LVX240

Octal Bus Buffer

Inverting With 5V-Tolerant Inputs

The MC74LVX240 is an advanced high speed CMOS inverting 3-state octal bus buffer and has two active low output enables. It is also designed to work with 3-state memory address drivers, etc. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

Features

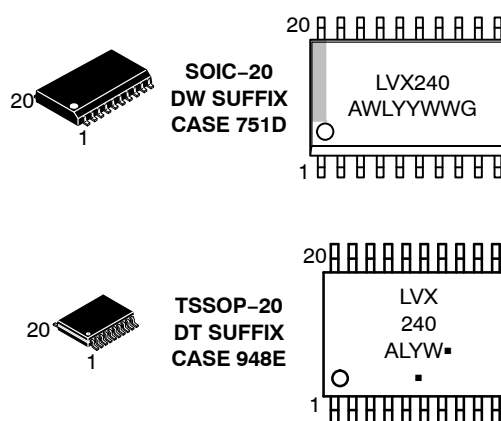
- High Speed: $t_{PD} = 4.3$ ns (Typ) at $V_{CC} = 3.3$ V
- Low Power Dissipation: $I_{CC} = 4$ μ A (Max) at $T_A = 25^\circ\text{C}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: $V_{OLP} = 0.8$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
 - Human Body Model > 2000 V;
 - Machine Model > 200 V
- These Devices are Pb-Free and are RoHS Compliant



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MARKING DIAGRAMS



LVX240 = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC74LVX240

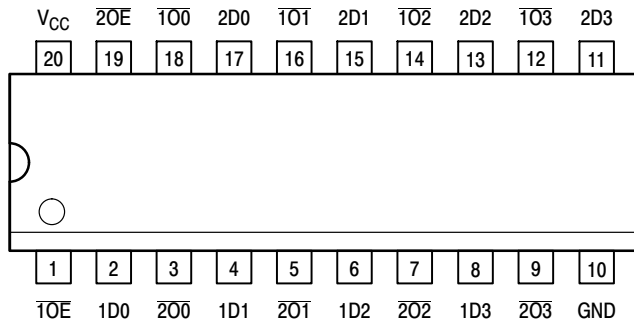


Figure 1. 20-Lead Pinout (Top View)

PIN NAMES

Pins	Function
$\overline{1OE}$, $\overline{2OE}$	Output Enable Inputs
$1Dn$, $2Dn$	Data Inputs
$\overline{1On}$, $\overline{2On}$	3-State Outputs

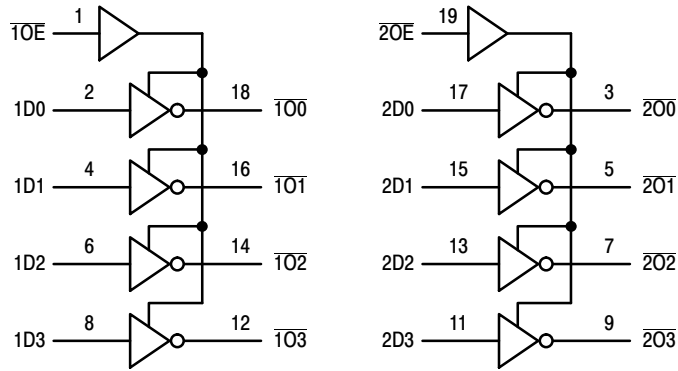


Figure 2. Logic Diagram

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{1OE}$, $\overline{2OE}$	$1Dn$, $2Dn$	$\overline{1On}$, $\overline{2On}$
L	L	H
L	H	L
H	X	Z

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74LVX240DWR2G	SOIC-20 (Pb-Free)	1000 / Tape & Reel
MC74LVX240DTR2G	TSSOP-20 (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	−0.5 to +7.0	V
V _{in}	DC Input Voltage	−0.5 to +7.0	V
V _{out}	DC Output Voltage	−0.5 to V _{CC} +0.5	V
I _{IK}	Input Diode Current	−20	mA
I _{OK}	Output Diode Current	±20	mA
I _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation	180	mW
T _{stg}	Storage Temperature	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	3.6	V
V _{in}	DC Input Voltage	0	5.5	V
V _{out}	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	−40	+85	°C
Δt/ΔV	Input Rise and Fall Time	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} V	T _A = 25°C			T _A = −40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V _{IL}	Low-Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V _{OH}	High-Level Output Voltage (V _{in} = V _{IH} or V _{IL})	I _{OH} = −50μA I _{OH} = −50μA I _{OH} = −4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V _{OL}	Low-Level Output Voltage (V _{in} = V _{IH} or V _{IL})	I _{OL} = 50μA I _{OL} = 50μA I _{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I _{in}	Input Leakage Current	V _{in} = 5.5V or GND	3.6			±0.1		±1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	3.6			±0.2 5		±2.5	μA
I _{CC}	Quiescent Supply Current	V _{in} = V _{CC} or GND	3.6			4.0		40.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
t_{PLH} , t_{PHL}	Propagation Delay Input to Output	$V_{CC} = 2.7\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		5.7 8.2	10.1 13.6	1.0 1.0	12.5 16.0	ns
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		4.3 6.8	6.2 9.7	1.0 1.0	7.5 11.0	
t_{PZL} , t_{PZH}	Output Enable Time to High and Low Level	$V_{CC} = 2.7\text{V}$ $R_L = 1\text{k}\Omega$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		7.1 9.6	13.8 17.3	1.0 1.0	16.5 20.0	ns
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $R_L = 1\text{k}\Omega$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		5.5 8.0	8.8 12.3	1.0 1.0	10.5 14.0	
t_{PLZ} , t_{PHZ}	Output Disable Time From High and Low Level	$V_{CC} = 2.7\text{V}$ $R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$		11.6	16.0	1.0	19.0	ns
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$		9.7	11.4	1.0	13.0	
t_{OSHL} , t_{OSLH}	Output-to-Output Skew (Note 1)	$V_{CC} = 2.7\text{V}$ $C_L = 50\text{pF}$			1.5		1.5	ns
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 50\text{pF}$			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
		Min	Typ	Max	Min	Max	
C_{in}	Input Capacitance		4	10		10	pF
C_{out}	Maximum Three-State Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 2)		19				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$, $C_L = 50\text{pF}$, $V_{CC} = 3.3\text{V}$, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-0.5	-0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

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SWITCHING WAVEFORMS

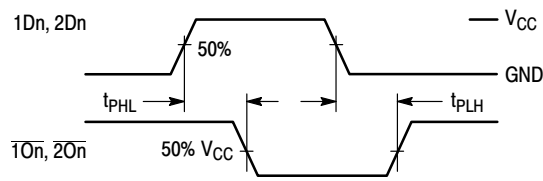


Figure 3.

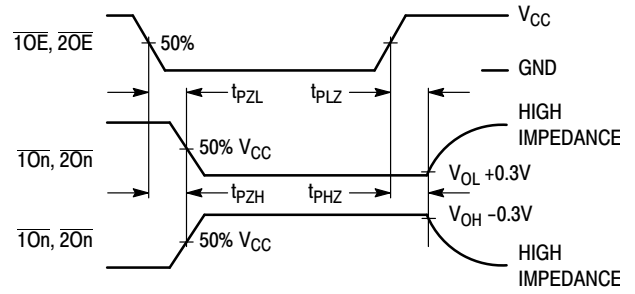
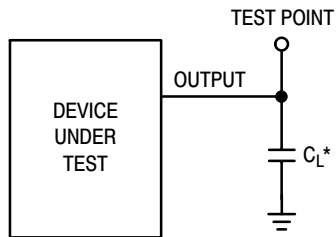


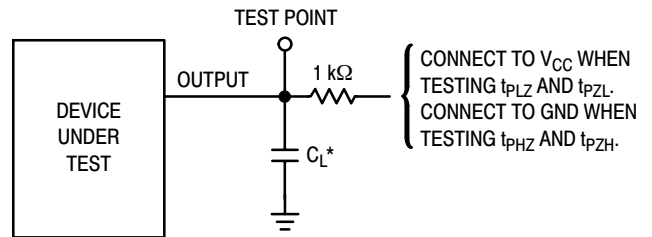
Figure 4.

TEST CIRCUITS



*Includes all probe and jig capacitance

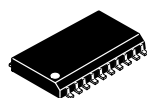
Figure 5. Propagation Delay Test Circuit



*Includes all probe and jig capacitance

Figure 6. Three-State Test Circuit

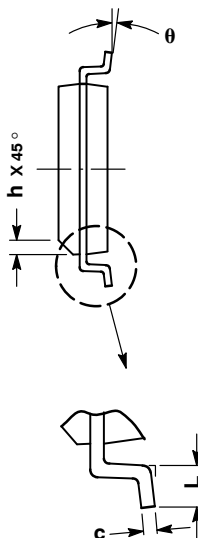
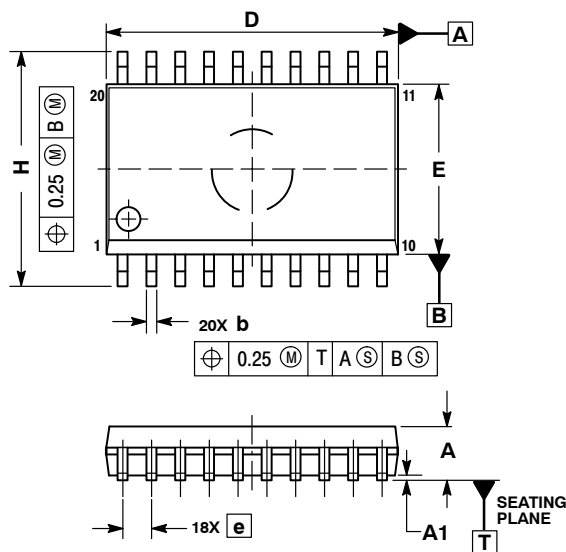
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

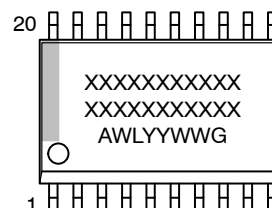


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

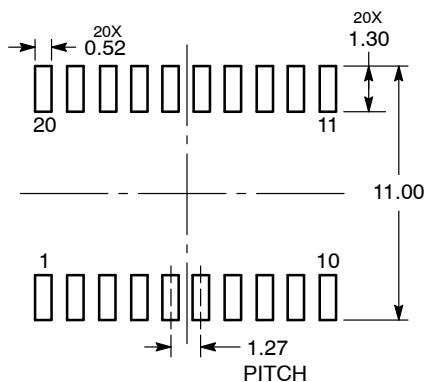
DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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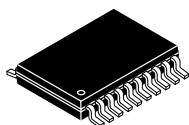
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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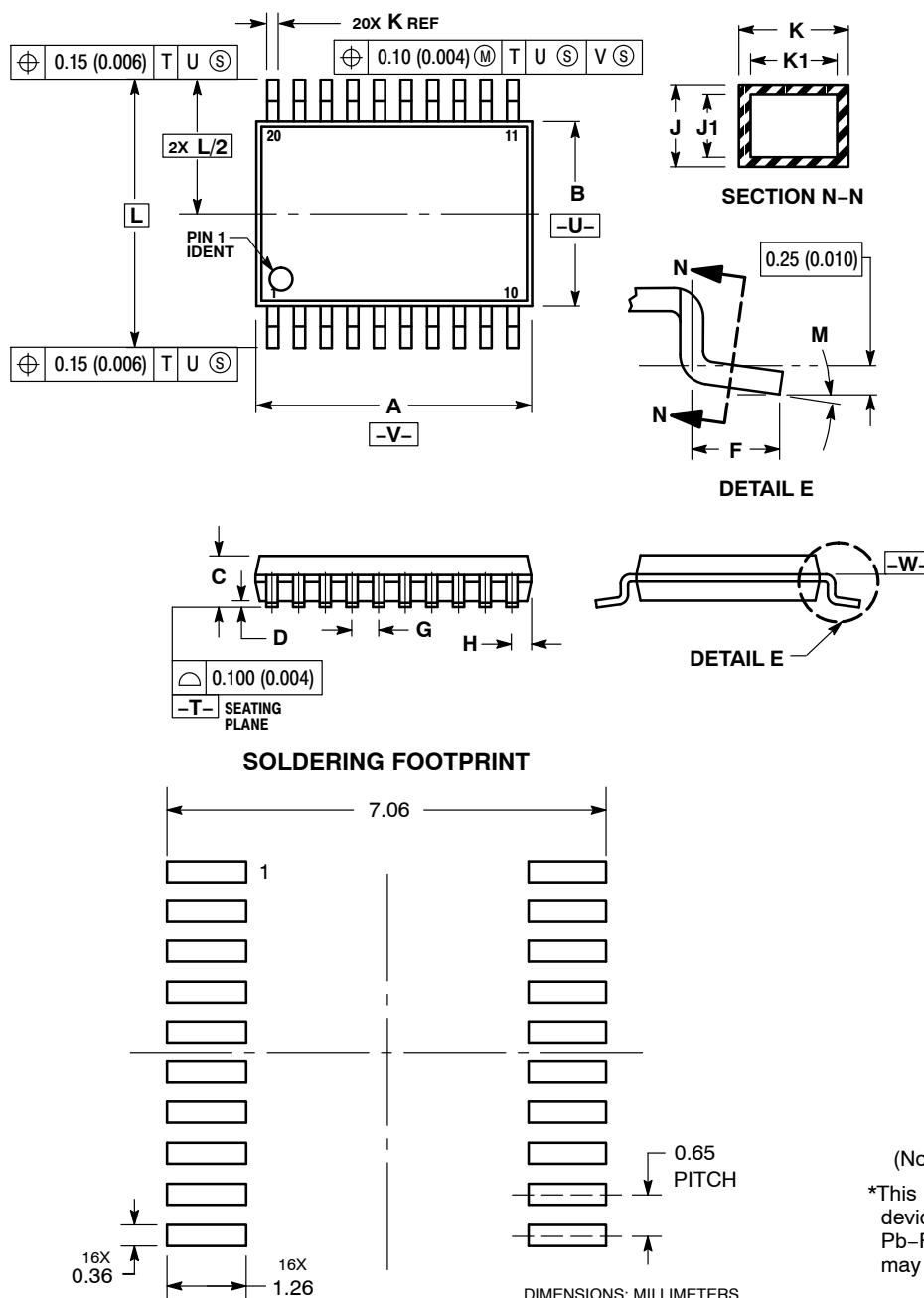
ON



SCALE 2:1

TSSOP-20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

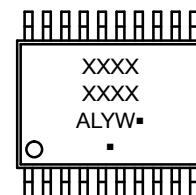


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC MARKING DIAGRAM*



- A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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