# Octal Bus Buffer

## Inverting

# MC74VHC540

The MC74VHC540 is an advanced high speed CMOS inverting octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC540 features inputs and outputs on opposite sides of the package and two AND−ed active−low output enables. When either $\overline{OE1}$ or $\overline{OE2}$ are high, the terminal outputs are in the high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 5.5 V, allowing the interface of 5.0 V systems to 3.0 V systems.

### Features

- High Speed: $t_{PD}$ = 3.7 ns (Typ) at $V_{CC}$ = 5.0 V
- Low Power Dissipation: $I_{CC}$ = 4.0 μA (Max) at $T_A$ = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% $V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: $V_{OLP}$ = 1.2 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 100 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 124 FETs or 31 Equivalent Gates
- These Devices are Pb−Free and are RoHS Compliant

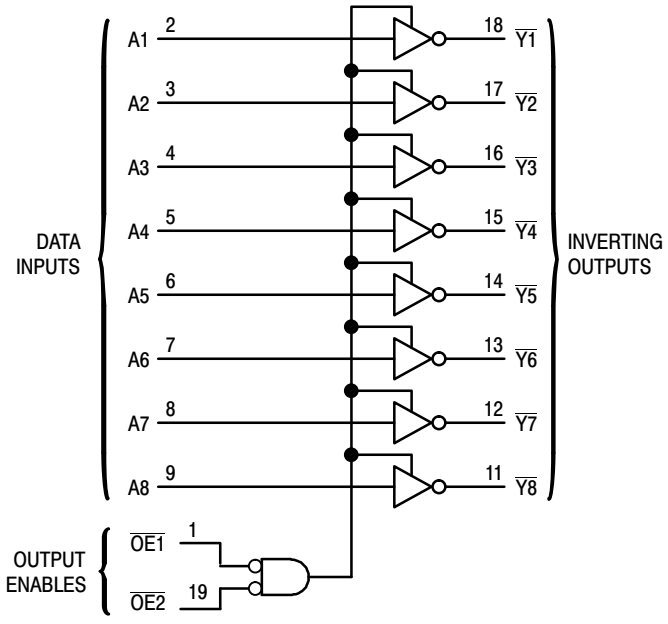
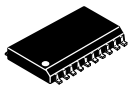
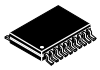



**Figure 1. Logic Diagram**

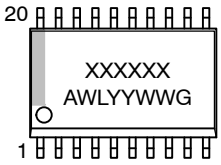


**SOIC−20**
**DW SUFFIX**
**CASE 751D**

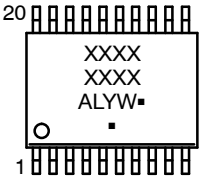


**TSSOP−20**
**DT SUFFIX**
**CASE 948E**

### MARKING DIAGRAMS




**SOIC−20**

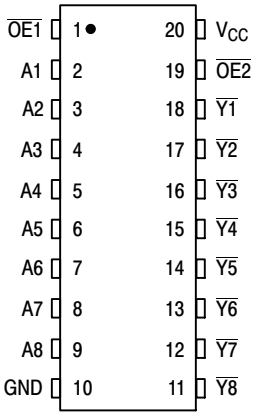



**TSSOP−20**

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

### PIN ASSIGNMENT




### FUNCTION TABLE

| Inputs | | | Output $\overline{Y}$ |
|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | A | |
| L | L | L | H |
| L | L | H | L |
| H | X | X | Z |
| X | H | X | Z |

### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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## MAXIMUM RATINGS

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | −0.5 to +6.5 | V |
| $V_{IN}$ | DC Input Voltage | | −0.5 to +6.5 | V |
| $V_{OUT}$ | DC Output Voltage | | −0.5 to $V_{CC}$+0.5 | V |
| $I_{IN}$ | DC Input Current, per Pin | | ±20 | mA |
| $I_{OUT}$ | DC Output Current, Per Pin | | ±25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | | ±75 | mA |
| $I_{IK}$ | Input Clamp Current | | −20 | mA |
| $I_{OK}$ | Output Clamp Current | | ±20 | mA |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 secs | | 260 | °C |
| $T_J$ | Junction Temperature Under Bias | | +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Note 1) | SOIC−20W<br>TSSOP−20 | 96<br>150 | °C/W |
| $P_D$ | Power Dissipation in Still Air at 25°C | SOIC−20W<br>TSSOP−20 | 1302<br>833 | mW |
| MSL | Moisture Sensitivity | | Level 1 | − |
| $F_R$ | Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.540 in | − |
| $V_{ESD}$ | ESD Withstand Voltage (Note 2) | Human Body Model<br>Charged Device Model | 2000<br>N/A | V |
| $I_{LATCHUP}$ | Latchup Performance (Note 3) | | ±100 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm−by−114 mm, 2−ounce copper trace no air flow per JESD51−7.
2. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.
3. Tested to EIA/JESD78 Class II.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | 2.0 | 5.5 | V |
| $V_{IN}$ | DC Input Voltage (Note 4) | | 0 | 5.5 | V |
| $V_{OUT}$ | DC Output Voltage (Note 4) | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature | | −55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise or Fall Rate | $V_{CC}$ = 3.0 V to 3.6 V<br>$V_{CC}$ = 4.5 V to 5.5 V | 0<br>0 | 100<br>20 | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS** (MC74VHC540)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | $T_A$ = 25°C | | | $T_A$ = − 55 to 125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $V_{IH}$ | Minimum High−Level Input Voltage | | 2.0<br>3.0 to 5.5 | 1.50<br>$V_{CC}$ x 0.7 | | | 1.50<br>$V_{CC}$ x 0.7 | | V |
| $V_{IL}$ | Maximum Low−Level Input Voltage | | 2.0<br>3.0 to 5.5 | | | 0.50<br>$V_{CC}$ x 0.3 | | 0.50<br>$V_{CC}$ x 0.3 | V |
| $V_{OH}$ | Minimum High−Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = − 50 μA | 2.0<br>3.0<br>4.5 | 1.9<br>2.9<br>4.4 | 2.0<br>3.0<br>4.5 | | 1.9<br>2.9<br>4.4 | | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = − 4 mA<br>$I_{OH}$ = − 8 mA | <br>3.0<br>4.5 | <br>2.58<br>3.94 | | | <br>2.48<br>3.80 | | |
| $V_{OL}$ | Maximum Low−Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OL}$ = 50 μA | 2.0<br>3.0<br>4.5 | | 0.0<br>0.0<br>0.0 | 0.1<br>0.1<br>0.1 | | 0.1<br>0.1<br>0.1 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OL}$ = 4 mA<br>$I_{OL}$ = 8 mA | <br>3.0<br>4.5 | | | <br>0.36<br>0.36 | | <br>0.44<br>0.44 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in}$ = 5.5 V or GND | 0 to 5.5 | | | ±0.1 | | ±1.0 | μA |
| $I_{OZ}$ | Maximum Three−State Leakage Current | $V_{in}$ = $V_{IL}$ or $V_{IH}$<br>$V_{out}$ = $V_{CC}$ or GND | 5.5 | | | ±0.25 | | ±2.5 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{in}$ = $V_{CC}$ or GND | 5.5 | | | 4.0 | | 40.0 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**AC ELECTRICAL CHARACTERISTICS** (MC74VHC540)

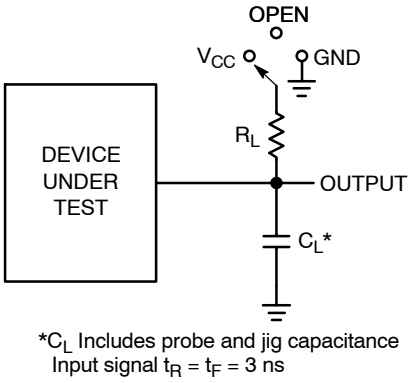
| Symbol | Parameter | Test Conditions | $T_A$ = 25°C | | | $T_A$ = − 55 to 125°C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, A to $\overline{Y}$ (Figures 1 and 3) | $V_{CC}$ = 3.3 ± 0.3 V $C_L$ = 15 pF | | 4.8 | 7.0 | 1.0 | 8.5 | ns |
| | | $C_L$ = 50 pF | | 7.3 | 10.5 | 1.0 | 12.0 | |
| | | $V_{CC}$ = 5.0 ± 0.5 V $C_L$ = 15 pF | | 3.7 | 5.0 | 1.0 | 6.0 | |
| | | $C_L$ = 50 pF | | 5.2 | 7.0 | 1.0 | 8.0 | |
| $t_{PZL}$, $t_{PZH}$ | Output Enable TIme, $\overline{OE}$n to $\overline{Y}$ (Figures 2 and 4) | $V_{CC}$ = 3.3 ± 0.3 V $C_L$ = 15 pF | | 6.8 | 10.5 | 1.0 | 12.5 | ns |
| | | $C_L$ = 50 pF | | 9.3 | 14.0 | 1.0 | 16.0 | |
| | | $V_{CC}$ = 5.0 ± 0.5 V $C_L$ = 15 pF | | 4.7 | 7.2 | 1.0 | 8.5 | |
| | | $C_L$ = 50 pF | | 6.2 | 9.2 | 1.0 | 10.5 | |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time, $\overline{OE}$n to $\overline{Y}$ (Figures 2 and 4) | $V_{CC}$ = 3.3 ± 0.3 V $C_L$ = 50 pF | | 11.2 | 15.4 | 1.0 | 17.5 | ns |
| | | $V_{CC}$ = 5.0 ± 0.5 V $C_L$ = 50 pF | | 6.0 | 8.8 | 1.0 | 10.0 | |
| $t_{OSLH}$, $t_{OSHL}$ | Output to Output Skew | $V_{CC}$ = 3.3 ± 0.3V $C_L$ = 50 pF (Note 5) | | | 1.5 | | | ns |
| | | $V_{CC}$ = 5.0 ± 0.5V $C_L$ = 50 pF (Note 5) | | | 1.0 | | | ns |
| $C_{in}$ | Maximum Input Capacitance | | | 4 | 10 | | 10 | pF |
| $C_{out}$ | Maximum Three−State Output Capacitance (Output in High Impedance State) | | | 6 | | | | pF |

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Note 6) | 17 | pF |

5. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
6. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). $C_{PD}$ is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

**NOISE CHARACTERISTICS** (MC74VHC540)

| Symbol | Parameter | $T_A$ = 25°C | | Unit |
|---|---|---|---|---|
| | | Typ | Max | |
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 0.9 | 1.2 | V |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | −0.9 | −1.2 | V |
| $V_{IHD}$ | Minimum High Level Dynamic Input Voltage | | 3.5 | V |
| $V_{ILD}$ | Maximum Low Level Dynamic Input Voltage | | 1.5 | V |




| Test | Switch Position | $C_L$ | $R_L$ |
|---|---|---|---|
| $t_{PLH}$ / $t_{PHL}$ | Open | See AC Characteristics Table | 1 kΩ |
| $t_{PLZ}$ / $t_{PZL}$ | $V_{CC}$ | | |
| $t_{PHZ}$ / $t_{PZH}$ | GND | | |

**Figure 2. Test Circuits**

## SWITCHING WAVEFORMS

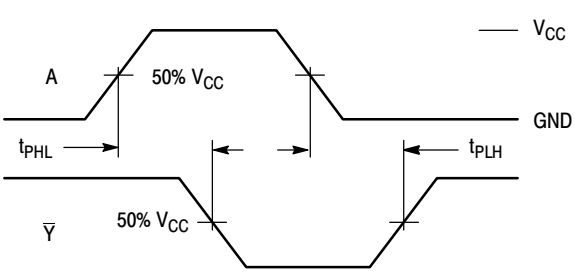



**Figure 3.**

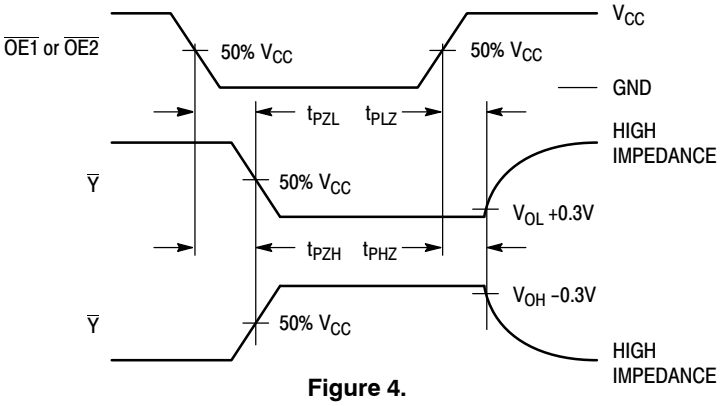



**Figure 4.**

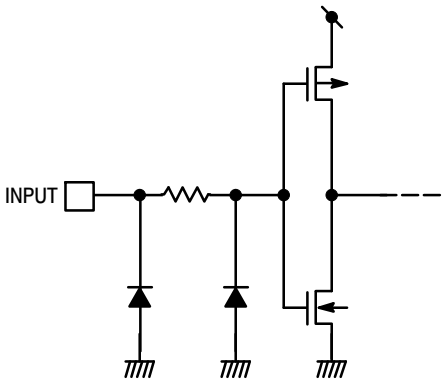



**Figure 5. Input Equivalent Circuit**

## ORDERING INFORMATION

| Device | Marking | Package | Shipping† |
|---|---|---|---|
| MC74VHC540DWR2G | VHC540G | SOIC−20 WB | 1000 / Tape & Reel |
| MC74VHC540DTR2G | VHC<br>540 | TSSOP−20 | 2500 / Tape & Reel |

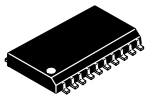
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

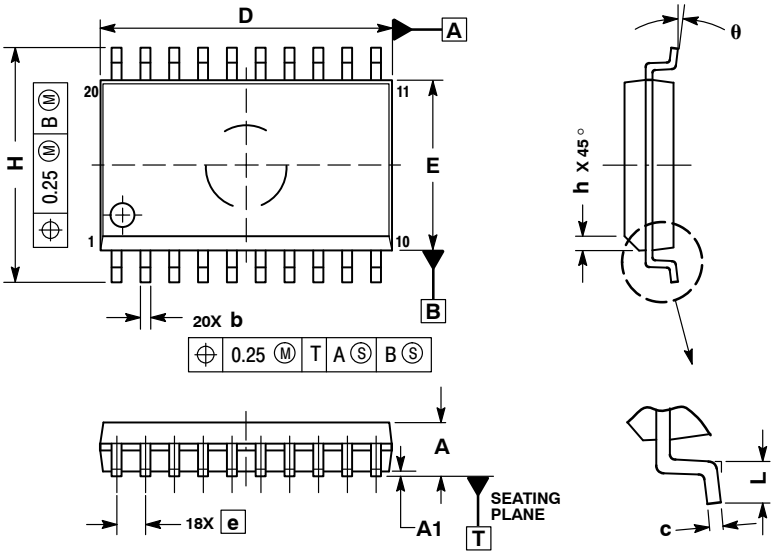
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**SOIC−20 WB**
CASE 751D−05
ISSUE H

DATE 22 APR 2015



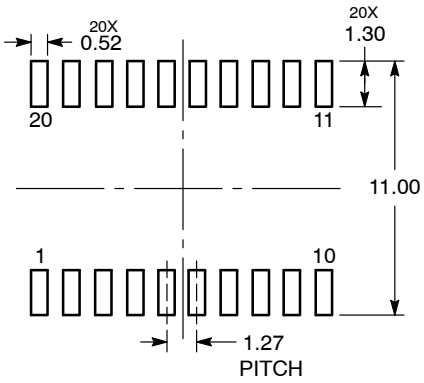
**SCALE 1:1**




NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

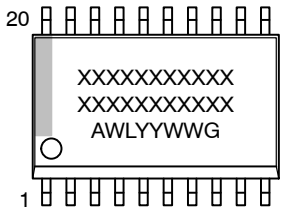
### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42343B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **SOIC−20 WB** | **PAGE 1 OF 1** |

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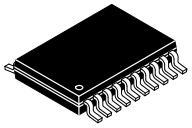
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

ON Semiconductor®

**TSSOP−20 WB**
CASE 948E
ISSUE D

DATE 17 FEB 2016



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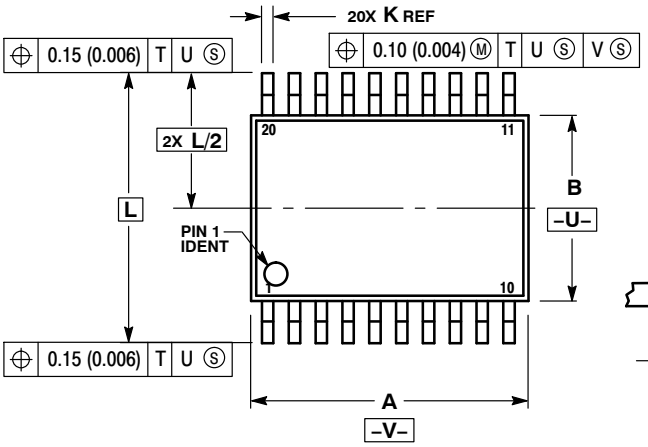
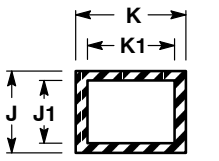
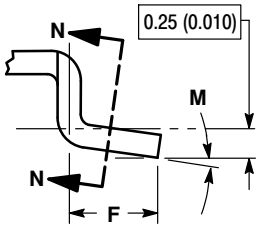
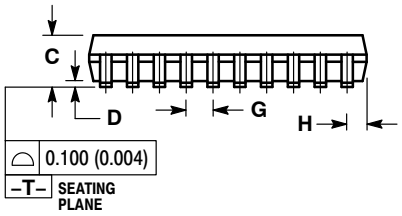


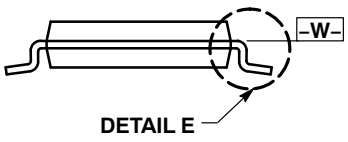




SECTION N−N




DETAIL E

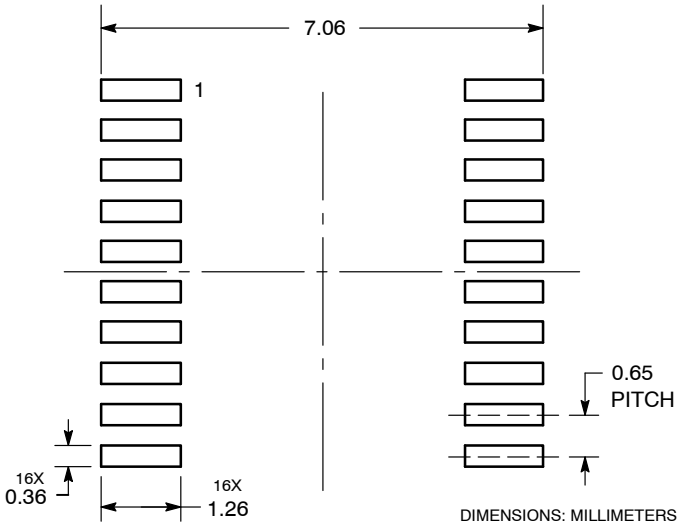



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

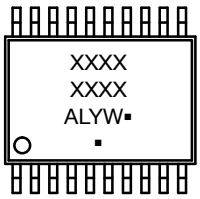
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

### SOLDERING FOOTPRINT




DIMENSIONS: MILLIMETERS

### GENERIC MARKING DIAGRAM*




A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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|---|---|---|
| DESCRIPTION: | TSSOP−20 WB | PAGE 1 OF 1 |

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