# **Quad 2-Channel Multiplexer** with 3-State Outputs

The MC74VHCT257A is an advanced high speed CMOS quad 2-channel multiplexer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

It consists of four 2-input digital multiplexers with common select (S) and enable  $(\overline{OE})$  inputs. When  $(\overline{OE})$  is held High, selection of data is inhibited and all the outputs go Low.

The select decoding determines whether the A or B inputs get routed to the corresponding Y outputs.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V because it has full 5.0 V CMOS level output swings.

The VHCT257A input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. The output structures also provide protection when  $V_{CC} = 0$  V. These input and output structures help prevent device destruction caused by supply voltage-input/output voltage mismatch, battery backup, hot insertion, etc.

The internal circuit is composed of three stages, including a buffered output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

## **Features**

- High Speed:  $t_{PD} = 4.1 \text{ ns (Typ)}$  at  $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 4.0 \mu A$  (Max) at  $T_A = 25$ °C
- TTL-Compatible Inputs:  $V_{IL} = 0.8 \text{ V}$ ;  $V_{IH} = 2.0 \text{ V}$
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise:  $V_{OLP} = 0.8 \text{ V (Max)}$
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:

Human Body Model > 2000 V; Machine Model > 200 V

• These Devices are Pb-Free and are RoHS Compliant



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## **MARKING DIAGRAMS**



SOIC-16 **D SUFFIX CASE 751B** 





WL, L

TSSOP-16 **DT SUFFIX** CASE 948F



 Assembly Location Wafer Lot

= Year WW. W = Work Week = Pb-Free Package

(Note: Microdot may be in either location)

## **FUNCTION TABLE**

Inp	Inputs				
ŌĒ	s	Outputs Y0 – Y3			
Н	Х	Z			
L	L	A0-A3			
L	Н	B0-B3			

A0 - A3, B0 - B3 = the levels of the respective Data-Word Inputs.

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

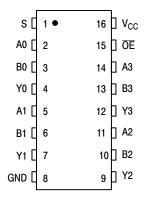


Figure 1. Pin Assignment

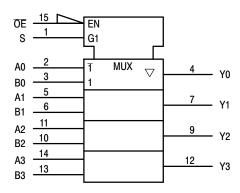


Figure 2. IEC Logic Symbol

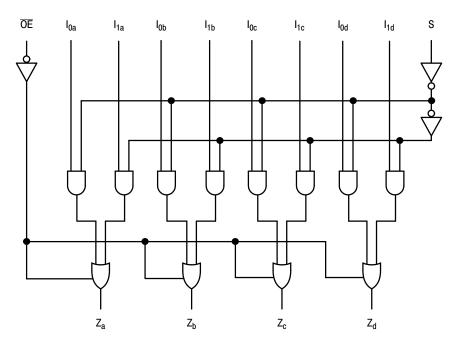


Figure 3. Expanded Logic Diagram

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

### **MAXIMUM RATINGS**

Symbol	Pa	Value	Unit	
V <sub>CC</sub>	Positive DC Supply Voltage		-0.5 to +7.0	V
V <sub>IN</sub>	Digital Input Voltage		-0.5 to +7.0	V
V <sub>OUT</sub>	DC Output Voltage	Output in 3–State High or Low State	−0.5 to +7.0 −0.5 to V <sub>CC</sub> +0.5	V
I <sub>IK</sub>	Input Diode Current		-20	mA
I <sub>OK</sub>	Output Diode Current		±20	mA
I <sub>OUT</sub>	DC Output Current, per Pin		±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins		±75	mA
P <sub>D</sub>	Power Dissipation in Still Air	SOIC TSSOP	200 180	mW
T <sub>STG</sub>	Storage Temperature Range		-65 to +150	°C
V <sub>ESD</sub>	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	>2000 >200 >2000	V
I <sub>LATCHUP</sub>	Latchup Performance Al	oove V <sub>CC</sub> and Below GND at 125°C (Note 4)	±300	mA
$\theta_{JA}$	Thermal Resistance, Junction-to-Ambie	ent SOIC TSSOP	143 164	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Tested to EIA/JESD22-A114-A
- 2. Tested to EIA/JESD22-A115-A
- 3. Tested to JESD22-C101-A
- 4. Tested to EIA/JESD78

## RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage		4.5	5.5	V
V <sub>IN</sub>	DC Input Voltage		0	5.5	V
V <sub>OUT</sub>	DC Output Voltage		0	5.5	V
T <sub>A</sub>	Operating Temperature Range, all Package Types		-55	125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise or Fall Time $V_{CC} = 5.0 \text{ V}$	<u>+</u> 0.5 V	0	20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction		
Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

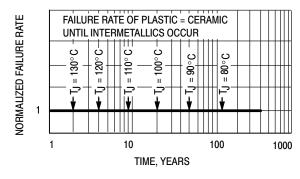


Figure 4. Failure Rate vs. Time Junction Temperature

## DC CHARACTERISTICS (Voltages Referenced to GND)

			V <sub>CC</sub>	T,	<sub>A</sub> = 25°	С	T <sub>A</sub> ≤	85°C	<b>-55°C</b> ≤ T	<sub>A</sub> ≤ 125°C	
Symbol	Parameter	Condition	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V <sub>IH</sub>	Minimum High-Level Input Voltage		4.5 to 5.5	2			2		2		V
V <sub>IL</sub>	Maximum Low-Level Input Voltage		4.5 to 5.5			0.8		0.8		0.8	V
V <sub>OH</sub>	Maximum High-Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu\text{A}$	4.5	3.94			3.8		3.66		V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -8 \text{ mA}$	4.5	3.94			3.8		3.66		
V <sub>OL</sub>	Maximum Low–Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50 \mu A$	4.5		0	0.1		0.1		0.1	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = 8 \text{ mA}$	4.5			0.36		0.44		0.52	
I <sub>IN</sub>	Input Leakage Current	$V_{IN} = 5.5 \text{ V or GND}$	0 to 5.5			±0.1		±1.0		±1.0	μΑ
I <sub>OZ</sub>	Maximum 3–State Leakage Current	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or GND}$	5.5			±0.2 5		±2.5		±2.5	μΑ
Ісст	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			1.35		1.5		1.65	mA
Icc	Additional Quiescent Supply Current (per pin)	$V_{IN} = V_{CC}$ or GND	5.5			4.0		40		40	μΑ
I <sub>OPD</sub>	Output Leakage Current	V <sub>OUT</sub> = 5.5 V	0			0.5		5		5	μΑ

## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ns}$ )

				T	<sub>A</sub> = 25°	С	<b>T</b> <sub>A</sub> = ≤	85°C	-55°C ≤ T	A ≤ 125°C	
Symbol	Parameter	Test Condi	tions	Min	Тур	Max	Min	Max	Min	Max	Unit
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A or B to Y	$V_{CC} = 3.3 \pm 0.3 \text{ V}$	$C_L = 15 pF$ $C_L = 50 pF$		5.8 8.3	9.3 12.8	1.0 1.0	11.0 14.5	1.0 1.0	11.0 14.5	ns
		$V_{CC} = 5.0 \pm 0.5 \text{ V}$	$C_L = 15 pF$ $C_L = 50 pF$		3.6 5.1	5.9 7.9	1.0 1.0	7.0 9.0	1.0 1.0	7.0 9.0	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, S to Y	$V_{CC} = 3.3 \pm 0.3 \text{ V}$	$C_L = 15 pF$ $C_L = 50 pF$		7.0 9.5	11.0 14.5	1.0 1.0	13.0 16.5	1.0 1.0	13.0 16.5	ns
		$V_{CC} = 5.0 \pm 0.5 \text{ V}$	$C_L = 15 pF$ $C_L = 50 pF$		4.0 5.5	6.8 8.8	1.0 1.0	8.0 10.0	1.0 1.0	8.0 10.0	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Output Enable, Time, OE to Y	$\begin{aligned} &V_{CC} = 3.3 \pm 0.3 \text{ V} \\ &R_L = 1 \text{ k}\Omega \end{aligned}$	C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		6.7 9.2	10.5 14.0	1.0 1.0	12.5 16.0	1.0 1.0	12.5 16.0	ns
		$V_{CC} = 5.0 \pm 0.5 \text{ V}$ $R_L = 1 \text{ k}\Omega$			3.6 5.1	6.8 11.0	1.0 12.0	8.0 10.0	1.0 1.0	8.0 12.0	
$t_{PLZ}, \ t_{PHZ}$	Maximum Output Disable, Time, OE to Y	$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $R_L = 1 \text{ k}\Omega$	C <sub>L</sub> = 50 pF		10.5	14.0	1.0	15.0	1.0	15.0	ns
		$V_{CC} = 5.0 \pm 0.5 \text{ V}$ $R_L = 1 \text{ k}\Omega$	$C_L = 50 pF$		9.5	12.0	1.0	13.0	1.0	13.0	
C <sub>IN</sub>	Maximum Input Capacitance				4	10		10		10	pF
				Typical @ 25°C, V <sub>CC</sub> = 5.0 V							
C	Power Dissipation Canasitan	oo (Noto E)						20			

C<sub>PD</sub> Power Dissipation Capacitance (Note 5)

5. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>. C<sub>PD</sub> is used to determine the no–load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

## **NOISE CHARACTERISTICS** (Input $t_r = t_f = 3.0 \text{ ns}$ , $C_L = 50 \text{ pF}$ , $V_{CC} = 5.0 \text{ V}$ )

		T <sub>A</sub> =	25°C	
Symbol	Characteristic		Max	Unit
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>		0.8	V
$V_{OLV}$	Quiet Output Minimum Dynamic V <sub>OL</sub>		- 0.8	V
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage		2.0	V
$V_{ILD}$	Maximum Low Level Dynamic Input Voltage		0.8	V

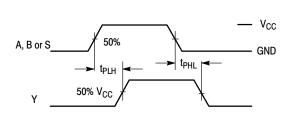


Figure 5. Switching Waveform

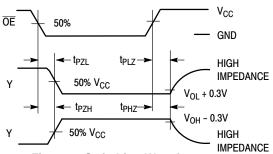
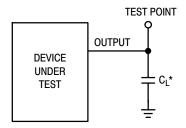


Figure 6. Switching Waveform



\*Includes all probe and jig capacitance Figure 7. Test Circuit

DEVICE UNDER TEST OUTPUT  $\begin{array}{c} & & & \\ &$ 

\*Includes all probe and jig capacitance

Figure 8. Test Circuit

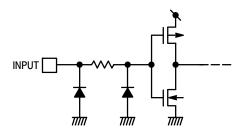


Figure 9. Input Equivalent Circuit

## **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
MC74VHCT257ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74VHCT257ADR2G	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74VHCT257ADTG	TSSOP-16 (Pb-Free)	96 Units / Rail
M74VHCT257ADTR2G	TSSOP-16 (Pb-Free)	2500 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



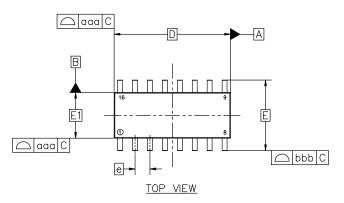


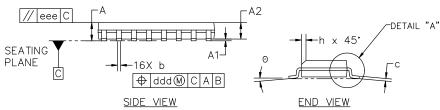
## SOIC-16 9.90x3.90x1.50 1.27P CASE 751B ISSUE L

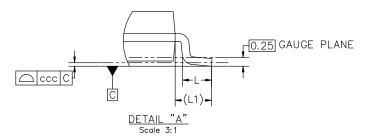
## **DATE 29 MAY 2024**

#### NOTES:

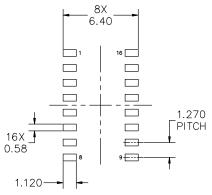
- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
- 2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
- 3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
- 4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
- 5. DIMENSION 6 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE 6 DIMENSION AT MAXIMUM MATERIAL CONDITION.







MILLIMETERS								
DIM	MIN NOM MAX							
А	1.35	1.55	1.75					
A1	0.00	0.05	0.10					
A2	1.35	1.50	1.65					
Ь	0.35	0.42	0.49					
С	0.19	0.22	0.25					
D		9.90 BSC						
E		6.00 BSC						
E1		3.90 BSC						
е		1.27 BSC						
h	0.25		0.50					
L	0.40	0.83	1.25					
L1		1.05 REF						
Θ	0.		7°					
TOLERAN	CE OF FO	RM AND	POSITION					
aaa	0.10							
bbb	0.20							
ccc	0.10							
ddd		0.25						
eee		0.10						



## RECOMMENDED MOUNTING FOOTPRINT

\*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE onsemi SOLDERING
AND MOUNTING TECHNIQUES REFERENCE
MANUAL, SOLDERRM/D

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DESCRIPTION:	SOIC-16 9.90X3.90X1.50 1	.27P	PAGE 1 OF 2

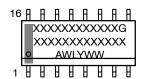
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## SOIC-16 9.90x3.90x1.50 1.27P CASE 751B ISSUE L

**DATE 29 MAY 2024** 

# GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code

A = Assembly Location

WL = Wafer Lot
 Y = Year
 WW = Work Week
 G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

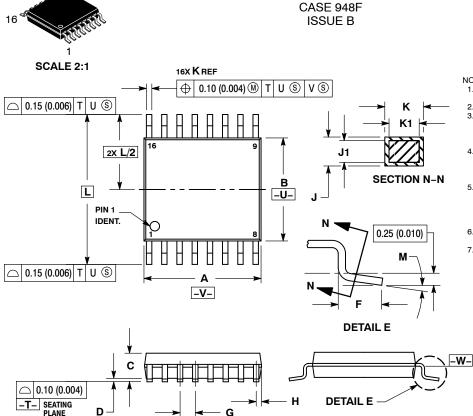
077/15/		077/15.0		071/15 0		T	
STYLE 1: PIN 1.	COLLECTOR	STYLE 2:	CATHODE	STYLE 3: PIN 1.		TYLE 4: PIN 1.	COLLECTOR DVF #1
PIN 1. 2.		PIN 1. 2.		PIN 1. 2.	COLLECTOR, DYE #1 BASE, #1	2.	
2. 3.	EMITTER	2. 3.	NO CONNECTION				
				3.		3.	
4.	NO CONNECTION	4.		4.		4.	
5.	EMITTER	5.		5.		5.	
6.	BASE	6.		6.		6.	
7.		7.			EMITTER, #2		COLLECTOR, #4
8.		8.		8.			COLLECTOR, #4
9.		9.			COLLECTOR, #3		BASE, #4
10.			ANODE		BASE, #3		EMITTER, #4
	NO CONNECTION	11.			EMITTER, #3		BASE, #3
	EMITTER		CATHODE		COLLECTOR, #3		EMITTER, #3
	BASE		CATHODE		COLLECTOR, #4		BASE, #2
	COLLECTOR	14.			BASE, #4		EMITTER, #2
15.			ANODE		EMITTER, #4		BASE, #1
16.	COLLECTOR	16.	CATHODE	16.	COLLECTOR, #4	16.	EMITTER, #1
STYLE 5:		STYLE 6:		STYLE 7:			
STYLE 5: PIN 1.	DRAIN, DYE #1	STYLE 6: PIN 1.	CATHODE	STYLE 7: PIN 1.	SOURCE N-CH		
	DRAIN, DYE #1 DRAIN, #1			PIN 1.	SOURCE N-CH COMMON DRAIN (OUTPUT)		
PIN 1.	,	PIN 1.	CATHODE	PIN 1.	COMMON DRAIN (OUTPUT)		
PIN 1. 2.	DRAIN, #1	PIN 1. 2.	CATHODE CATHODE	PIN 1. 2.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3.	DRAIN, #1 DRAIN, #2	PIN 1. 2. 3.	CATHODE CATHODE	PIN 1. 2. 3.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4.	DRAIN, #1 DRAIN, #2 DRAIN, #2	PIN 1. 2. 3. 4.	CATHODE CATHODE CATHODE CATHODE	PIN 1. 2. 3. 4.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3	PIN 1. 2. 3. 4. 5.	CATHODE CATHODE CATHODE CATHODE	PIN 1. 2. 3. 4. 5.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4	PIN 1. 2. 3. 4. 5.	CATHODE CATHODE CATHODE CATHODE CATHODE	PIN 1. 2. 3. 4. 5.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5. 6. 7.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3	PIN 1. 2. 3. 4. 5. 6.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE	PIN 1. 2. 3. 4. 5. 6.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH		
PIN 1. 2. 3. 4. 5. 6. 7.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4	PIN 1. 2. 3. 4. 5. 6. 7.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 SOURCE, #4	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 GATE, #4 SOURCE, #4 GATE, #3	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 SOURCE, #4	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE ANODE ANODE ANODE ANODE ANODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 GATE, #4 SOURCE, #4 GATE, #3 SOURCE, #3 GATE, #2	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE ANODE ANODE ANODE ANODE ANODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GOMMON DRAIN (OUTPUT) GATE N-CH		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 DRAIN, #4 GATE, #4 SOURCE, #4 GATE, #3 SOURCE, #3 GATE, #2 SOURCE, #2 SOURCE, #2	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) CATE N-CH COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 GATE, #4 SOURCE, #4 GATE, #3 SOURCE, #3 GATE, #2	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE N-CH COMMON DRAIN (OUTPUT)		

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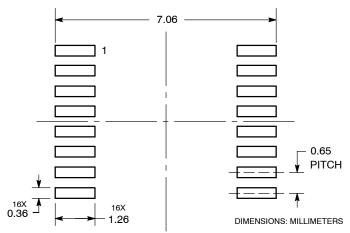
TSSOP-16 WB

#### NOTES

- DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT
- EXCEED 0.15 (0.006) PER SIDE.
  DIMENSION B DOES NOT INCLUDE
  INTERLEAD FLASH OR PROTRUSION.
- INTERLEAD FLASH OR PROTRUSION.
  INTERLEAD FLASH OR PROTRUSION SHALL
  NOT EXCEED 0.25 (0.010) PER SIDE.
  DIMENSION K DOES NOT INCLUDE DAMBAR
  PROTRUSION. ALLOWABILE DAMBAR
  PROTRUSION SHALL BE 0.08 (0.003) TOTAL
  IN EXCESS OF THE K DIMENSION AT
  MAXIMUM MATERIAL CONDITION.
  TERMINIAL NILMBERS ADE SUCIUMI ECIP.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
Н	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
М	0 °	8 °	0 °	8 °

## **RECOMMENDED** SOLDERING FOOTPRINT\*



<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## **GENERIC MARKING DIAGRAM\***



= Specific Device Code XXXX Α = Assembly Location

= Wafer Lot L = Year W = Work Week G or • = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present. Some products may not follow the Generic Marking.

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