# MC14532B

# **8-Bit Priority Encoder**

The MC14532B is constructed with complementary MOS (CMOS) enhancement mode devices. The primary function of a priority encoder is to provide a binary address for the active input with the highest priority. Eight data inputs (D0 thru D7) and an enable input (E<sub>in)</sub> are provided. Five outputs are available, three are address outputs (Q0 thru Q2), one group select (GS) and one enable output (E<sub>out</sub>).

### **Features**

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

### MAXIMUM RATINGS (Voltages Referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage Range	$V_{DD}$	-0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V <sub>in</sub> , V <sub>out</sub>	$-0.5$ to $V_{DD} + 0.5$	V
Input or Output Current (DC or Transient) per Pin	I <sub>in</sub> , I <sub>out</sub>	±10	mA
Power Dissipation, per Package (Note 1)	P <sub>D</sub>	500	mW
Ambient Temperature Range	T <sub>A</sub>	-55 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Lead Temperature (8 Sec Soldering)	TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Package: -7.0 mW/°C From 65°C To 125°C This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

### **TRUTH TABLE**

	Input								Outp	ut			
Ein	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E <sub>out</sub>
0	Χ	Χ	Χ	Χ	Х	Х	Χ	Х	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	Х	Χ	Х	Х	Х	Х	Х	1	1	1	1	0
1	0	1	Χ	Х	Х	Х	Х	Х	1	1	1	0	0
1	0	0	1	Х	Х	Х	Х	Х	1	1	0	1	0
1	0	0	0	1	Х	Х	Х	Х	1	1	0	0	0
1	0	0	0	0	1	Х	Χ	Х	1	0	1	1	0
1	0	0	0	0	0	1	Х	Χ	1	0	1	0	0
1	0	0	0	0	0	0	1	Х	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care



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SOIC-16 D SUFFIX CASE 751B

### **PIN ASSIGNMENT**

D4 [	1●	16	V <sub>DD</sub>
D5 [	2	15	] E <sub>out</sub>
D6 [	3	14	] gs
D7 [	4	13	] D3
E <sub>in</sub> [	5	12	D2
Q2 [	6	11	D1
Q1 [	7	10	] D0
v <sub>ss</sub> [	8	9	] Q0

### MARKING DIAGRAM



A = Assembly Location

WL = Wafer Lot
 YY, Y = Year
 WW = Work Week
 G = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

### MC14532B

#### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC14532BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14532BDR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
NLV14532BDR2G*	SOIC-16 (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# **ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

				- 5	5°C		25°C		12	5°C	
Characteristic		Symbol	V <sub>DD</sub> Vdc	Min	Max	Min	Typ (Note 2)	Max	Min	Max	Unit
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level	V <sub>OL</sub>	5.0 10 15	- - -	0.05 0.05 0.05	- - -	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
$V_{in} = 0 \text{ or } V_{DD}$	"1" Level	V <sub>OH</sub>	5.0 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.0 10 15	- - -	4.95 9.95 14.95	- - -	Vdc
Input Voltage $(V_O = 4.5 \text{ or } 0.5 \text{ Vdc})$ $(V_O = 9.0 \text{ or } 1.0 \text{ Vdc})$ $(V_O = 13.5 \text{ or } 1.5 \text{ Vdc})$	"0" Level	V <sub>IL</sub>	5.0 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.50 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	Vdc
$(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$ $(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$ $(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$	"1" Level	V <sub>IH</sub>	5.0 10 15	3.5 7.0 11	- - -	3.5 7.0 11	2.75 5.50 8.25	_ _ _	3.5 7.0 11	_ _ _	Vdc
Output Drive Current ( $V_{OH}$ = 2.5 Vdc) ( $V_{OH}$ = 4.6 Vdc) ( $V_{OH}$ = 9.5 Vdc) ( $V_{OH}$ = 13.5 Vdc)	Source	I <sub>OH</sub>	5.0 5.0 10 15	-3.0 -0.64 -1.6 -4.2	- - - -	-2.4 - 0.51 -1.3 -3.4	-4.2 -0.88 -2.25 -8.8	- - - -	-1.7 -0.36 -0.9 -2.4	- - - -	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	Sink	I <sub>OL</sub>	5.0 10 15	0.64 1.6 4.2	- - -	0.51 1.3 3.4	0.88 2.25 8.8	- - -	0.36 0.9 2.4	- - -	mAdc
Input Current		l <sub>in</sub>	15	-	±0.1	-	±0.00001	±0.1	_	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)		C <sub>in</sub>	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current (Per Package)		I <sub>DD</sub>	5.0 10 15	- - -	5.0 10 20	- - -	0.005 0.010 0.015	5.0 10 20	- - -	150 300 600	μAdc
Total Supply Current (Note (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, buffers switching)	. ,	Ι <sub>Τ</sub>	5.0 10 15			$I_{T} = (3$	.74 μA/kHz) .65 μA/kHz) .73 μA/kHz)	f + I <sub>DD</sub>	•	•	μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

- 3. The formulas given are for the typical characteristics only at 25°C.
  4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

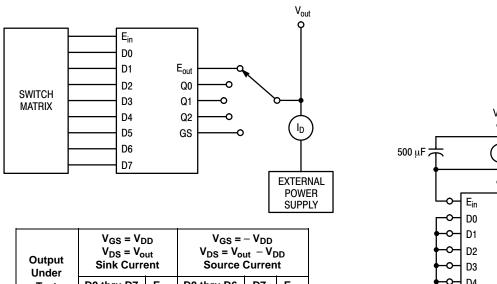
where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts, f in kHz is input frequency, and k = 0.005.

<sup>\*</sup>NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

# SWITCHING CHARACTERISTICS ( $C_L = 50 \text{ pF}, T_A = 25^{\circ}\text{C}$ ) (Note 5)

Characteristic	Symbol	V <sub>DD</sub>	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time $t_{TLH}$ , $t_{THL}$ = (1.5 ns/pF) $C_L$ + 25 ns $t_{TLH}$ , $t_{THL}$ = (0.75 ns/pF) $C_L$ + 12.5 ns $t_{TLH}$ , $t_{THL}$ = (0.55 ns/pF) $C_L$ + 9.5 ns	t <sub>TLH</sub> , t <sub>THL</sub>	5.0 10 15	- - -	100 50 40	200 100 80	ns
Propagation Delay Time — $E_{in}$ to $E_{out}$ $t_{PLH}$ , $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 120 ns $t_{PLH}$ , $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 77 ns $t_{PLH}$ , $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 55 ns	t <sub>PLH</sub> , t <sub>PHL</sub>	5.0 10 15	- - -	205 110 80	410 220 160	ns
Propagation Delay Time — $E_{in}$ to GS $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 90 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L 57 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 40 \text{ ns}$	t <sub>PLH</sub> , t <sub>PHL</sub>	5.0 10 15	- - -	175 90 65	350 180 130	ns
Propagation Delay Time — $E_{in}$ to $Q_n$ $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 195 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 107 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$	t <sub>PHL</sub> , t <sub>PLH</sub>	5.0 10 15	- - -	280 140 100	560 280 200	ns
$ \begin{array}{l} \text{Propagation Delay Time} & D_{n} \text{ to } Q_{n} \\ \text{t}_{PLH}, \text{t}_{PHL} = (1.7 \text{ ns/pF}) \text{ C}_{L} + 265 \text{ ns} \\ \text{t}_{PLH}, \text{t}_{PHL} = (0.66 \text{ ns/pF}) \text{ C}_{L} + 137 \text{ ns} \\ \text{t}_{PLH}, \text{t}_{PHL} = (0.5 \text{ ns/pF}) \text{ C}_{L} + 85 \text{ ns} \end{array} $	t <sub>PLH</sub> , t <sub>PHL</sub>	5.0 10 15	- - -	300 170 110	600 340 220	ns
Propagation Delay Time — $D_n$ to GS $t_{PLH}$ , $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 195 ns $t_{PLH}$ , $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 107 ns $t_{PLH}$ , $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 75 ns	t <sub>PLH</sub> , t <sub>PHL</sub>	5.0 10 15	- - -	280 140 100	560 280 200	ns

- 5. The formulas given are for the typical characteristics only at 25°C.
  6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



Output Under	V <sub>GS</sub> = V <sub>D</sub> V <sub>DS</sub> = V <sub>o</sub> Sink Curre	ut	V <sub>GS</sub> = - V <sub>DD</sub> V <sub>DS</sub> = V <sub>out</sub> - V <sub>DD</sub> Source Current		
Test	D0 thru D7	Ein	D0 thru D6	D7	Ein
E <sub>out</sub>	Х	0	0	0	1
Q0	X	0	0	1	1
Q1	X	0	0	1	1
Q2	X	0	0	1	1
GS	X	0	0	1	1

Figure 1. Typical Sink and Source **Current Characteristics** 

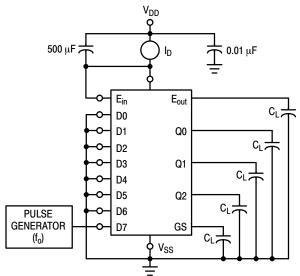
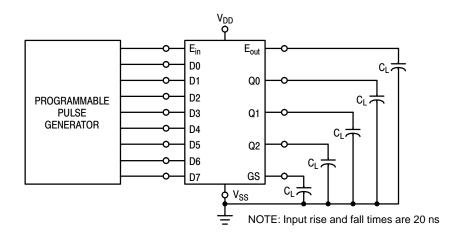


Figure 2. Typical Power Dissipation Test Circuit



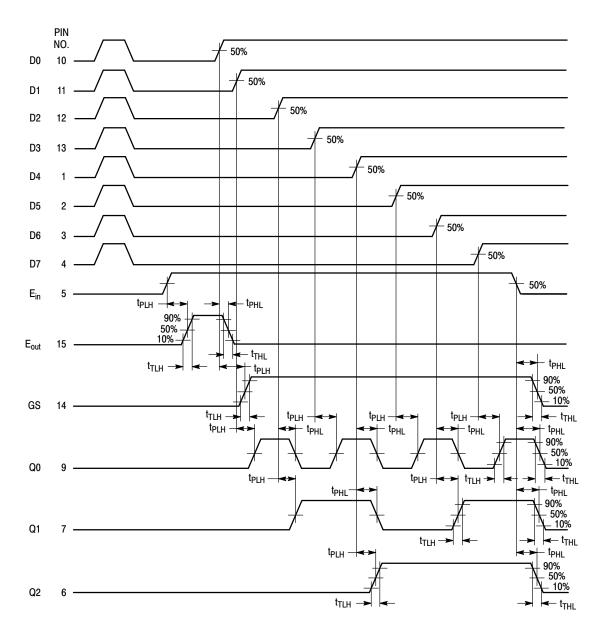


Figure 3. AC Test Circuit and Waveforms

# **LOGIC EQUATIONS**

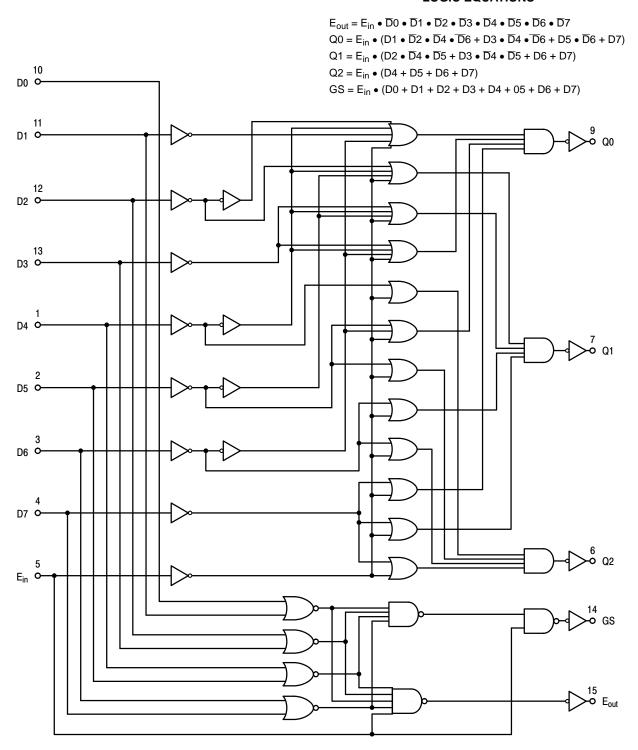


Figure 4. Logic Diagram (Positive Logic)

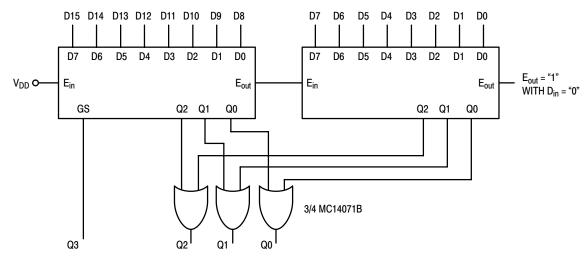


Figure 5. Two MC14532B's Cascaded for 4-Bit Output

# **DIGITAL TO ANALOG CONVERSION**

The digital eight—bit word to be converted is applied to the inputs of the MC14512 with the most significant bit at X7 and the least significant bit at X0. A clock input of up to 2.5 MHz (at  $V_{DD}=10$  V) is applied to the MC14520B. A compromise between  $I_{bias}$  for the MC1710 and  $\Delta R$  between N and P—channel outputs gives a value of R of 33 k $\Omega$ . In order to filter out the switching frequencies, RC should be about 1.0 ms (if  $R=33~k\Omega$ ,  $C\approx0.03~\mu F$ ). The analog 3.0 dB bandwidth would then be dc to 1.0 kHz.

### **ANALOG TO DIGITAL CONVERSION**

An analog signal is applied to the analog input of the MC1710. A digital eight—bit word known to represent a digitized level less than the analog input is applied to the MC14512 as in the D to A conversion. The word is incremented at rates sufficient to allow steady state to be reached between incrementations (i.e. 3.0 ms). The output of the MC1710 will change when the digital input represents the first digitized level above the analog input. This word is the digital representation of the analog word.

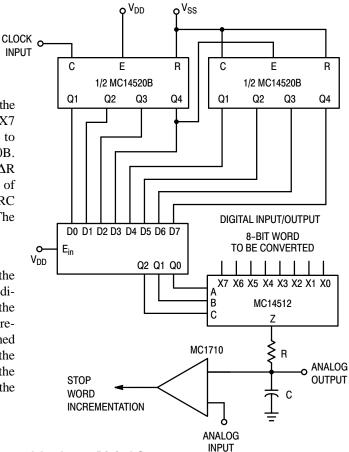


Figure 6. Digital to Analog and Analog to Digital Converter



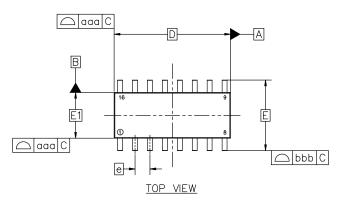


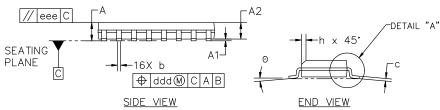
### SOIC-16 9.90x3.90x1.50 1.27P CASE 751B ISSUE L

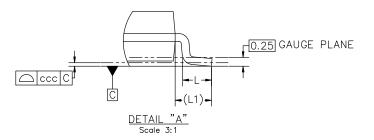
# **DATE 29 MAY 2024**

#### NOTES:

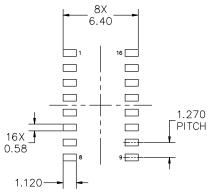
- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
- 2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
- 3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
- 4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
- 5. DIMENSION 6 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE 6 DIMENSION AT MAXIMUM MATERIAL CONDITION.







MILLIMETERS								
DIM	MIN	NOM	MAX					
А	1.35	1.55	1.75					
A1	0.00	0.05	0.10					
A2	1.35	1.50	1.65					
Ь	0.35	0.42	0.49					
С	0.19	0.22	0.25					
D		9.90 BSC						
E		6.00 BSC						
E1		3.90 BSC						
е		1.27 BSC						
h	0.25		0.50					
L	0.40	0.83	1.25					
L1		1.05 REF						
Θ	0.		7°					
TOLERAN	CE OF FO	RM AND	POSITION					
aaa	0.10							
bbb	0.20							
ccc	0.10							
ddd		0.25						
eee		0.10						



### RECOMMENDED MOUNTING FOOTPRINT

\*FOR ADDITIONAL INFORMATION ON OUR
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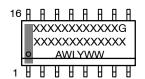
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### SOIC-16 9.90x3.90x1.50 1.27P CASE 751B ISSUE L

**DATE 29 MAY 2024** 

# GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code

A = Assembly Location

WL = Wafer Lot
 Y = Year
 WW = Work Week
 G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

077/15/		077/15.0		071/15 0		T.4.	
STYLE 1: PIN 1.	COLLECTOR	STYLE 2:	CATHODE	STYLE 3: PIN 1.		TYLE 4: PIN 1.	COLLECTOR DVF #1
PIN 1. 2.		PIN 1. 2.		PIN 1. 2.	COLLECTOR, DYE #1 BASE, #1	PIN 1. 2.	
2. 3.	EMITTER	2. 3.	NO CONNECTION				
				3.		3.	
4.	NO CONNECTION	4.		4.		4.	
5.	EMITTER	5.		5.		5.	
6.	BASE	6.		6.		6.	
7.		7.			EMITTER, #2		COLLECTOR, #4
8.		8.		8.			COLLECTOR, #4
9.		9.			COLLECTOR, #3		BASE, #4
10.			ANODE		BASE, #3		EMITTER, #4
	NO CONNECTION	11.			EMITTER, #3		BASE, #3
	EMITTER		CATHODE		COLLECTOR, #3		EMITTER, #3
	BASE		CATHODE		COLLECTOR, #4		BASE, #2
	COLLECTOR	14.			BASE, #4		EMITTER, #2
15.			ANODE		EMITTER, #4		BASE, #1
16.	COLLECTOR	16.	CATHODE	16.	COLLECTOR, #4	16.	EMITTER, #1
STYLE 5:		STYLE 6:		STYLE 7:			
STYLE 5: PIN 1.	DRAIN, DYE #1	STYLE 6: PIN 1.	CATHODE	STYLE 7: PIN 1.	SOURCE N-CH		
	DRAIN, DYE #1 DRAIN, #1			PIN 1.	SOURCE N-CH COMMON DRAIN (OUTPUT)		
PIN 1.	,	PIN 1.	CATHODE	PIN 1.	COMMON DRAIN (OUTPUT)		
PIN 1. 2.	DRAIN, #1	PIN 1. 2.	CATHODE CATHODE	PIN 1. 2.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3.	DRAIN, #1 DRAIN, #2	PIN 1. 2. 3.	CATHODE CATHODE	PIN 1. 2. 3.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4.	DRAIN, #1 DRAIN, #2 DRAIN, #2	PIN 1. 2. 3. 4.	CATHODE CATHODE CATHODE CATHODE	PIN 1. 2. 3. 4.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3	PIN 1. 2. 3. 4. 5.	CATHODE CATHODE CATHODE CATHODE	PIN 1. 2. 3. 4. 5.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4	PIN 1. 2. 3. 4. 5.	CATHODE CATHODE CATHODE CATHODE CATHODE	PIN 1. 2. 3. 4. 5.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5. 6. 7.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3	PIN 1. 2. 3. 4. 5. 6.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE	PIN 1. 2. 3. 4. 5. 6.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH		
PIN 1. 2. 3. 4. 5. 6. 7.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4	PIN 1. 2. 3. 4. 5. 6. 7.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 SOURCE, #4	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 GATE, #4 SOURCE, #4 GATE, #3	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 SOURCE, #4	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE ANODE ANODE ANODE ANODE ANODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 GATE, #4 SOURCE, #4 GATE, #3 SOURCE, #3 GATE, #2	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE ANODE ANODE ANODE ANODE ANODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GOMMON DRAIN (OUTPUT) GATE N-CH		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 DRAIN, #4 GATE, #4 SOURCE, #4 GATE, #3 SOURCE, #3 GATE, #2 SOURCE, #2 SOURCE, #2	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) CATE N-CH COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 GATE, #4 SOURCE, #4 GATE, #3 SOURCE, #3 GATE, #2	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE N-CH COMMON DRAIN (OUTPUT) GATE N-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		

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