3.6V to 35V Input 1ch Buck Controller

BD9845FV

General Description

BD9845FV is a switching regulator controller that uses pulse width modulation. This IC can be used for step-down DC/DC converter applications. BD9845FV is available in a compact package that is optimum for compact power supplies of many kinds of equipment.

Features

- Operates up to (V_{CC}=35V)
- Contains FET Driver Circuit (Step-Down Circuit 1 output).
- REG Output Circuit (2.5V) are contained.
- Built-In Over Current Protect
- Adjustable Soft Start and Pause Period.
- Three modes of Standby, Master, and Slave can be Switched. (I_{CCS} = 0 µA typ during standby)
- ON/OFF control is enabled independently for each channel. (DT terminal)

Applications

LCD, PDP, PC, AV, Printer, DVD, Projector TV, Fax, Copy Machine, Measuring Instrument, etc

Key Specifications

- Supply Voltage Range: 3.6V to 35V
- Error Amplifier Reference Voltage: 1.0V±1%
- Oscillation Frequency: 100kHz to 1500kHz
- Standby Current: 0µA(Typ)
- Operating Temperature Range: -40°C to +85°C

Package

W(Typ) x D(Typ) x H(Max)

SSOP-B14
5.00mm x 6.40mm x 1.35mm

Typical Application Circuit

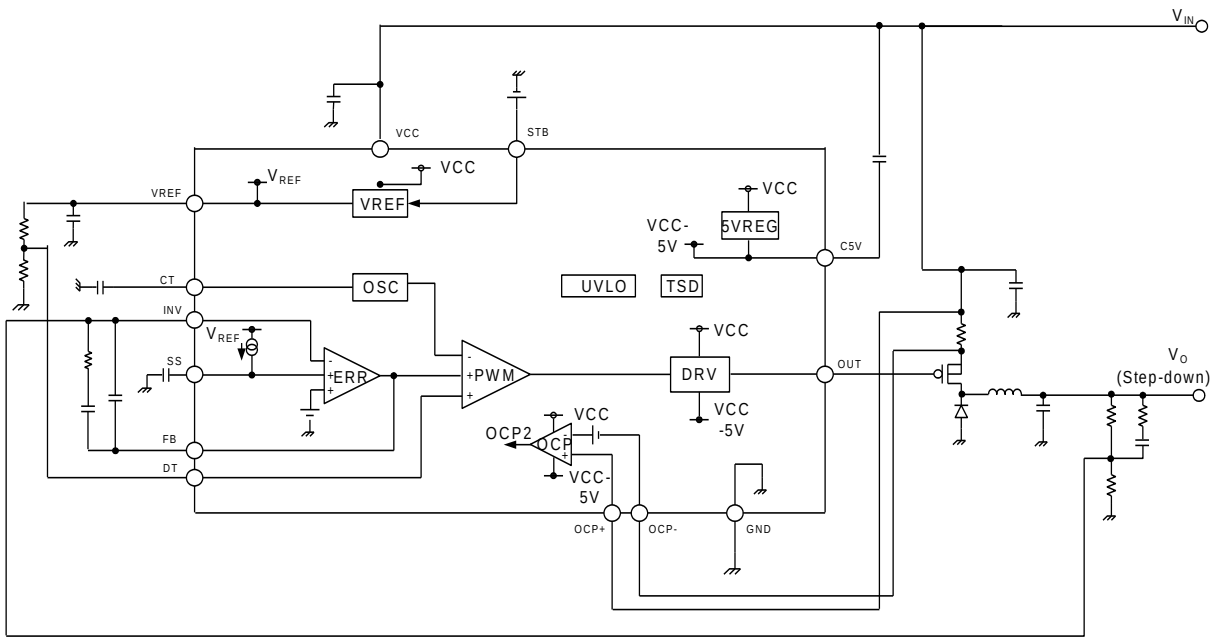
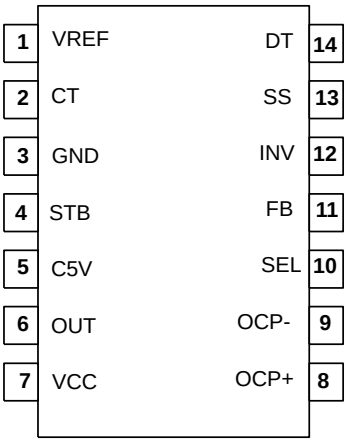


Figure 1. Typical Application Circuit

Pin Configuration

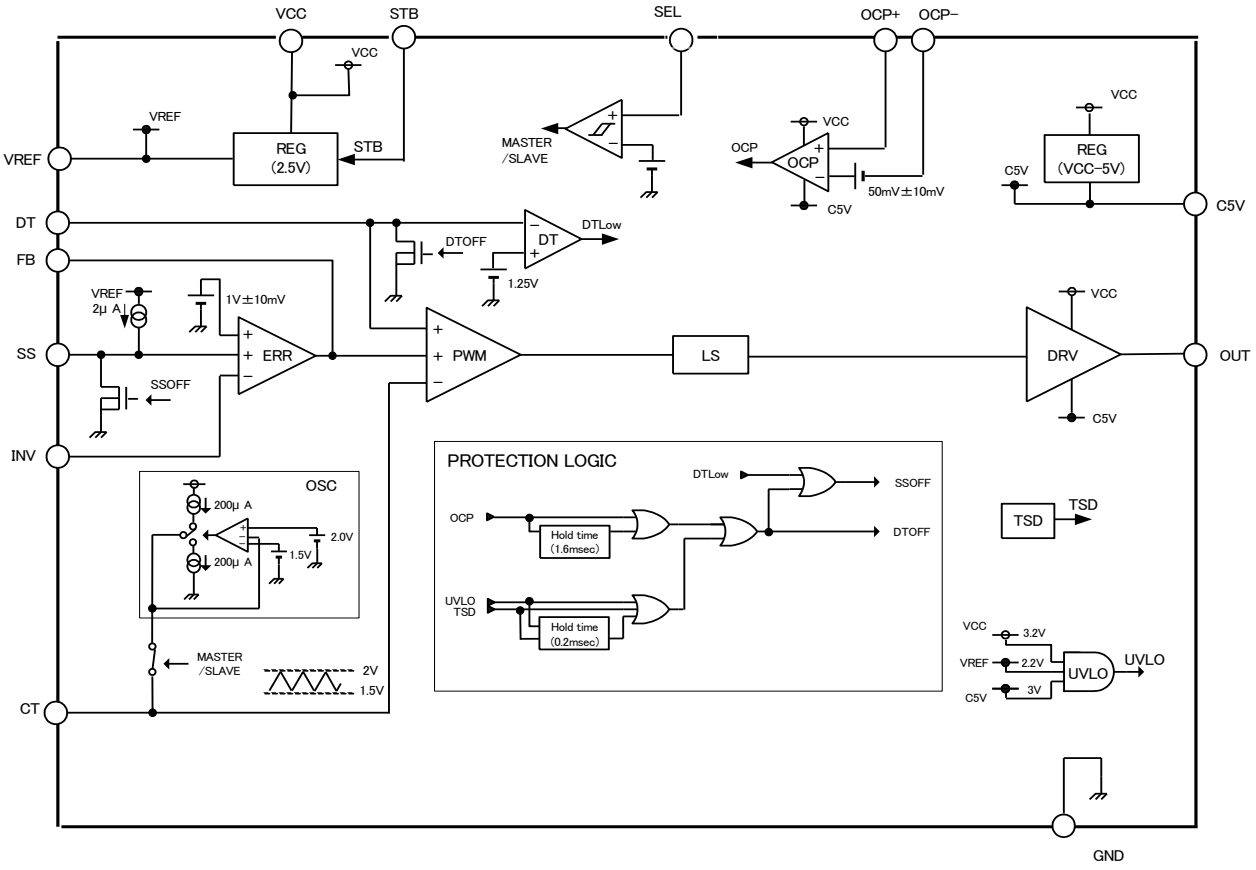
(TOP VIEW)



Pin Description

Pin Number	Pin Name	Function	Pin Number	Pin Name	Function
1	VREF	Reference voltage (2.5V) output terminal	8	OCP +	Output over-current detector + input terminal
2	CT	Timing capacity external terminal	9	OCP -	Output over-current detector - input terminal
3	GND	Ground	10	SEL	Master/Slave mode setting terminal
4	STB	Standby mode setting terminal	11	FB	Output error amplifier output terminal
5	C5V	Output L side voltage (V_{CC}-5V)	12	INV	Output error amplifier - input terminal
6	OUT	Output	13	SS	Output soft start time setting terminal
7	VCC	Power terminal	14	DT	Output dead time setting terminal

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	36	V
Permissible Loss	Pd	0.50 (Note 1)	W
OUT Terminal Voltage	V_{OUT}	V_{CC}-7V to V_{CC}	V
C5V Terminal Voltage	V_{C5V}	V_{CC}-7V to V_{CC}	V
OCP Terminal Voltage	V_{OCP}	V_{CC}-7V to V_{CC}	V
Operation Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Joint Temperature	Tjmax	150	°C

(Note 1) When mounted on a 70.0 mm × 70.0 mm × 1.6 mm glass epoxy board. Derate by 4.0 mW/C above Ta=25°C.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. In addition, it is impossible to predict all destructive situations such as short-circuit modes, open circuit modes, etc. Therefore, it is important to consider circuit protection measures, like adding a fuse, in case the IC is operated in a special mode exceeding the absolute maximum ratings.

Recommended Operating Conditions (Ta=25°C)

Item	Symbol	Range	Unit
Supply Voltage	V_{CC}	3.6 to 35	V
Output Terminal Voltage	V_{OUT}	V_{C5V} to V_{CC}	V
Timing Capacity	C_{CT}	47 to 3000	pF
Error Amplifier Input Voltage	V_{INV}	0 to V_{REF}-0.9	V
DT Terminal Input Voltage	V_{DT}	0 to V_{REF}	V
OCP+/- Input Voltage	V_{OCP}	V_{CC}±0.2	V
Oscillation Frequency	f_{OSC}	100 to 1500	kHz
STB Input Voltage	V_{STB}	0 to V_{CC}	V
SEL Input Voltage	V_{SEL}	0 to V_{CC}	V

Electrical Characteristics

(Unless otherwise specified, Ta=25°C, V_{CC}=6V)

Item	Symbol	Standard Value			Unit	Conditions
		Min	Typ	Max		
[VREF Output Unit]						
Output Voltage	V_{REF}	2.450	2.500	2.550	V	I_{OUT}= 0.1mA
Input Stability(Line Reg.)	V_{LI_REG}	-	1	10	mV	V_{CC}= 3.6V to 35V
Load Stability(Load Reg.)	V_{LO_REG}	-	2	10	mV	I_{OUT}= 0.1mA to 2mA
Current Capacity	I_{OMAX}	2	13	-	mA	V_{REF}= (Typ)x0.95
[Triangular Wave Oscillator]						
Oscillation Frequency	f_{OSC}	95	106	117	kHz	C_{CP}= 1800pF
Frequency Fluctuation	f_{DV}	-	0	1	%	V_{CC}= 3.6V to 35V
[Soft Start Unit]						
SS Source Current	I_{SSSO}	1.4	2	2.6	µA	V_{SS}= 0.5V
SS Sink Current	I_{SSSI}	5	12	-	mA	V_{SS}= 0.5V
[Pause Period Adjusting Circuit]						
DT Input Bias Current	I_{DT}	-	0.1	1	µA	V_{DT}= 1.75V
DT Sink Current	I_{DTSI}	1	3.3	-	mA	V_{DT}= 1.75V, (V_{OCP+})-(V_{OCP-})= 0.5V
[Low Input Malfunction Preventing Circuit]						
Threshold Voltage	V_{UTH}	3.0	3.2	3.4	V	VCC Start Detection
Hysteresis	V_{UHYS}	-	0.15	0.25	V	
[Error Amplifier]						
Non-Inverting Input Reference Voltage	V_{INV}	0.99	1	1.01	V	INV= FB
Reference Voltage Supply Fluctuation	dV_{INV}	-	1	6	mV	V_{CC}= 3.6V to 35V
INV Input Bias Current	I_{IB}	-	0	1	µA	V_{INV}= 1V
Open Gain	AV	65	85	-	dB	
Max Output Voltage	V_{FBH}	2.30	-	V_{REF}	V	
Min Output Voltage	V_{FBL}	-	0.6	1.3	V	
Output Sink Current	I_{FBSI}	0.5	1.5	-	mA	V_{FB}= 1.25V, V_{INV}= 1.5V
Output Source Current	I_{FBSO}	50	105	-	µA	V_{FB}= 1.25V, V_{INV}= 0.5V
[PWM Comparator]						
Input Threshold Voltage (f_{OSC}=100kHz)	V_{th0}	1.4	1.5	1.6	V	On Duty 0%
	V_{th100}	1.9	2	2.1	V	On Duty 100%
[Output Unit]						
Output ON Resistance H	R_{ONH}	-	4.0	10	Ω	R_{ONH}= (V_{CC} -V_{OUT})/ I_{OUT}, I_{OUT}= 0.1A
Output ON Resistance L	R_{ONL}	-	3.3	10	Ω	R_{ONL}= (V_{OUT} -V_{C5V})/ I_{OUT}, I_{OUT}= 0.1A
C5V Clamp Voltage	V_{CLMP}	4.5	5	5.5	V	V_{CLMP}= V_{CC}- V_{C5V} , V_{CC} > 7 V
[Over-Current Protection Circuit]						
Over-Current Detection Threshold Voltage	V_{OCPTH}	0.04	0.05	0.06	V	Voltage Between(OCP+) and (OCP-)
OCP-Input Bias Current	I_{OCP-}	-	0.1	10	µA	OCP+= V_{CC}, OCP-= V_{CC}-0.5V
Over-Current Detection Delay Time	t_{DOCPTH}	-	200	400	ns	OCP-= V_{CC}→ V_{CC}-0.2 V
Over-Current Detection Minimum Retention Time	t_{DOCPRE}	0.8	1.6	-	ms	OCP-= V_{CC}-0.2V→ V_{CC}
[Standby Changeover Unit]						
STB Flow-In Current	I_{STB}	-	55	100	µA	V_{STB}= 6V
Standby Mode Setting Range	V_{STBL}	0	-	0.5	V	
Active (Master) Mode Setting Range	V_{STBH}	3.0	-	V_{CC}	V	
SEL Flow-in Current	I_{SEL}	-	15	30	µA	V_{SEL}= 2.5V
Master Mode Setting Range	V_{SELL}	0	-	0.5	V	
Slave Mode Setting Range	V_{SELH}	2.0	-	V_{CC}	V	
[Device Overall]						
Standby Current	I_{CCS}	-	0	1	µA	V_{STB}= 0V
Average Power Consumption	I_{CCA}	1	2.4	4	mA	V_{INV}= 0V, FB= H, V_{DT}= 1.75V

Typical Performance Curves

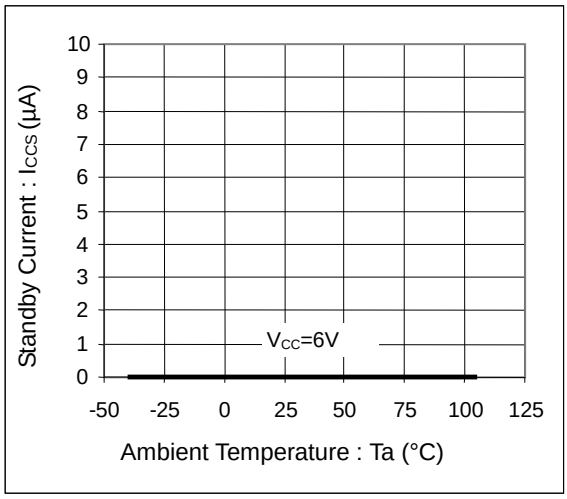


Figure 2. Standby Current vs Ambient Temperature

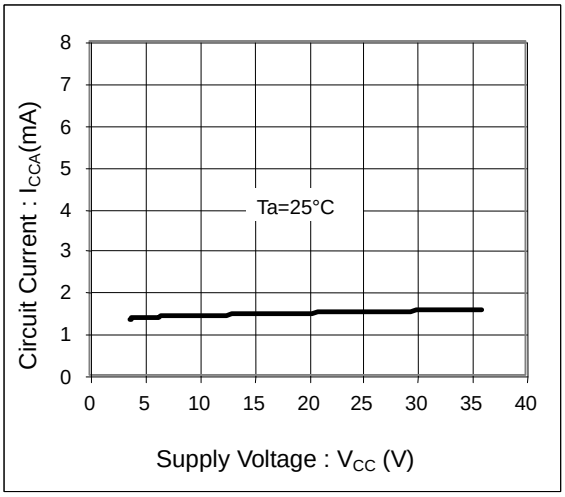


Figure 3. Circuit Current vs Supply Voltage

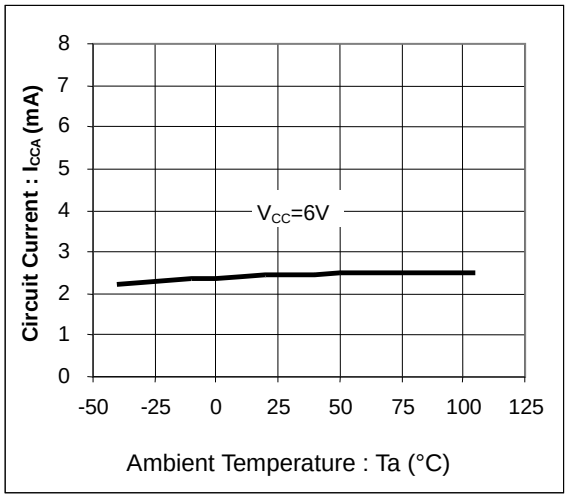


Figure 4. Circuit Current vs Ambient Temperature

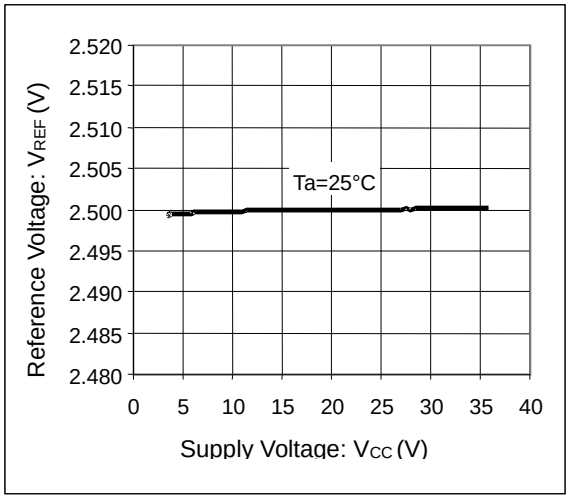


Figure 5. Reference Voltage vs Supply Voltage

Typical Performance Curves – continued

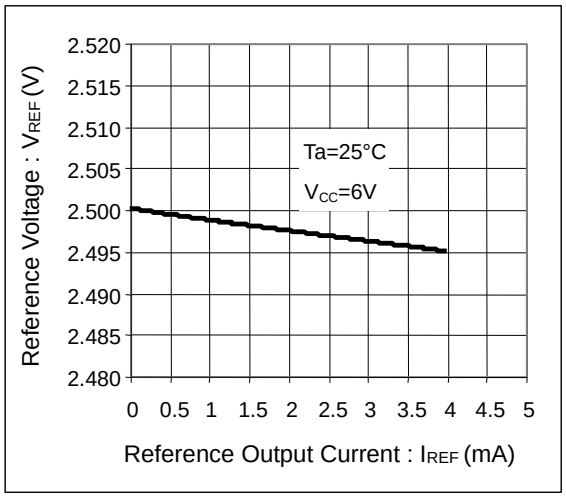


Figure 6. Reference Voltage vs Reference Output Current (VREF Current Capability)

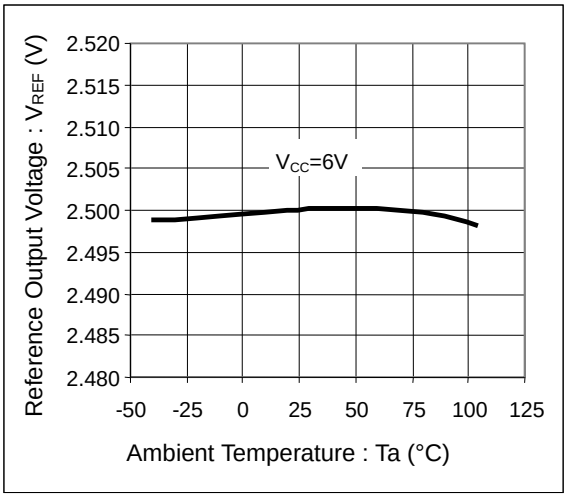


Figure 7. Reference Output Voltage vs Ambient Temperature (VREF Temperature Characteristics)

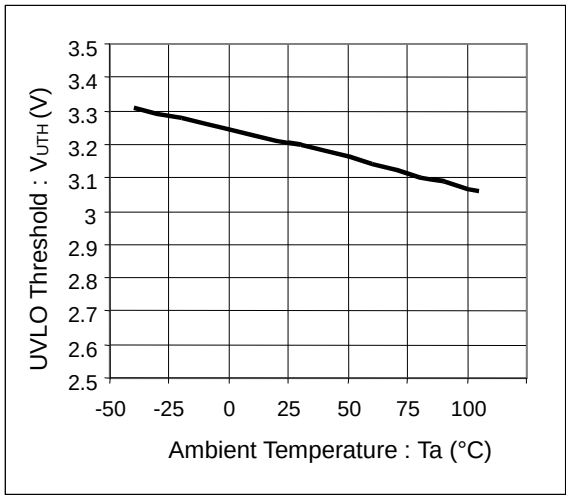


Figure 8. UVLO Threshold vs Ambient Temperature

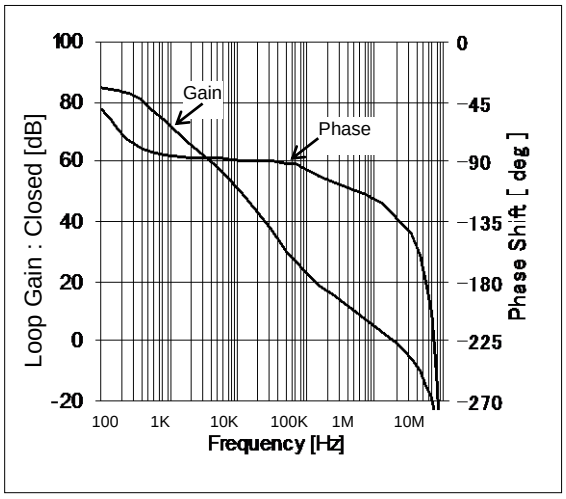


Figure 9. Loop Gain vs Frequency (Error Amplifier I/O Characteristics)

Typical Performance Curves – continued

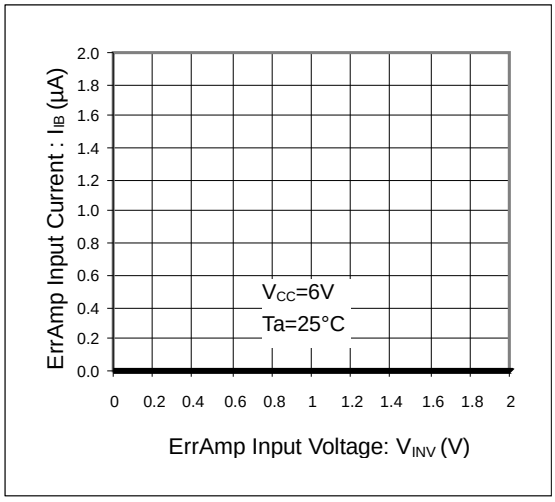


Figure 10. Error Amplifier Input Current vs Error Amplifier Input Voltage

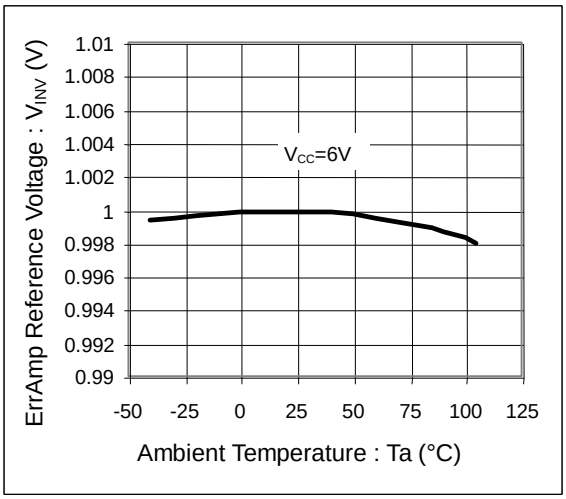


Figure 11. Error Amplifier Reference Voltage vs Ambient Temperature

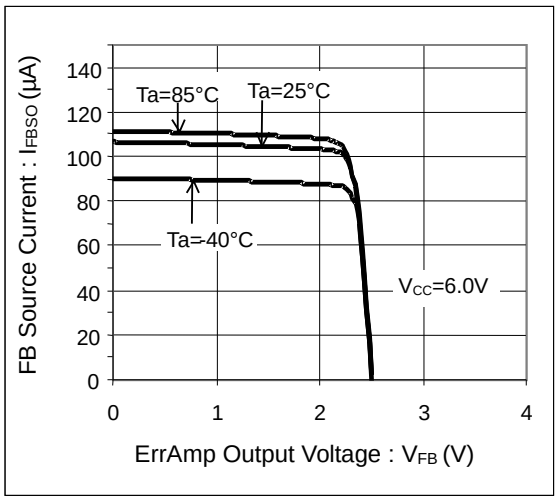


Figure 12. FB Source Current vs Error Amplifier Output Voltage

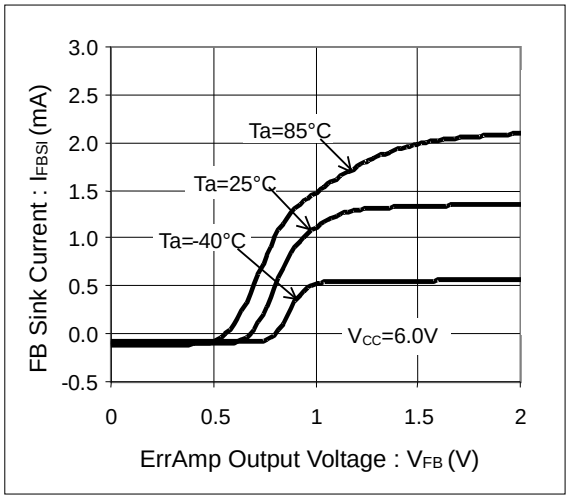


Figure 13. FB Sink Current vs Error Amplifier Output Voltage

Typical Performance Curves – continued

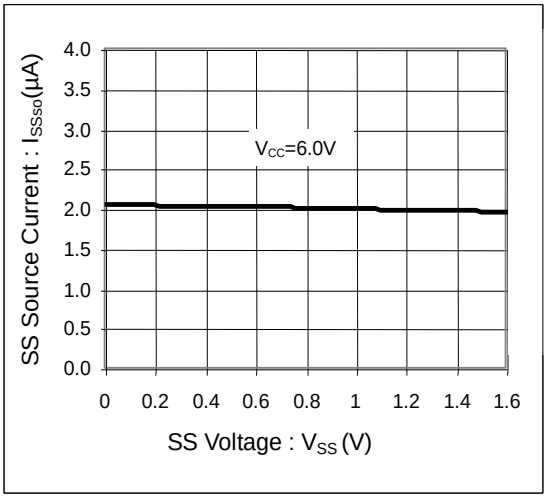


Figure 14. Soft Start Source Current vs Soft Start Voltage

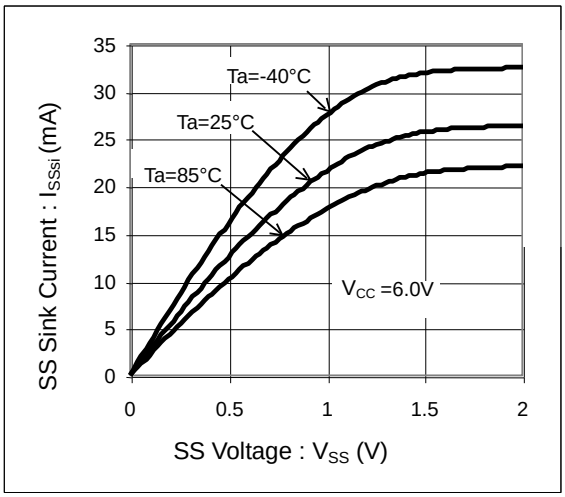


Figure 15. Soft Start Sink Current vs Soft Start Voltage

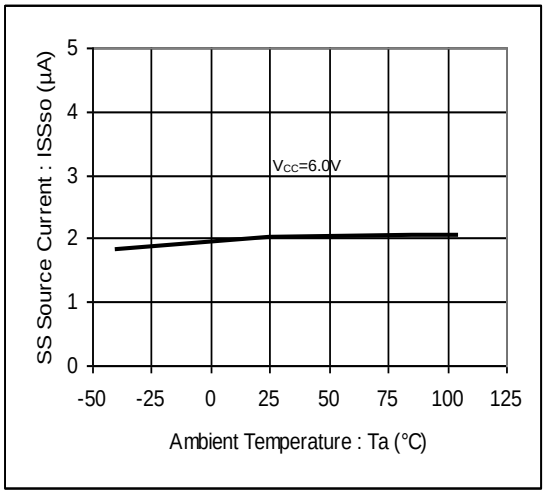


Figure 16. Soft Start Source Current vs Ambient Temperature

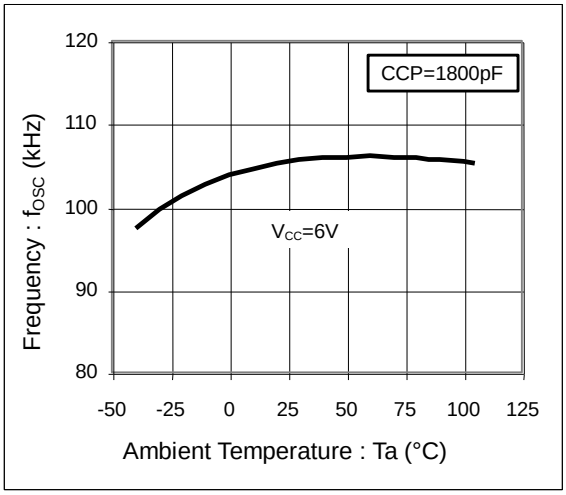


Figure 17. Oscillation Frequency vs Ambient Temperature

Typical Performance Curves – continued

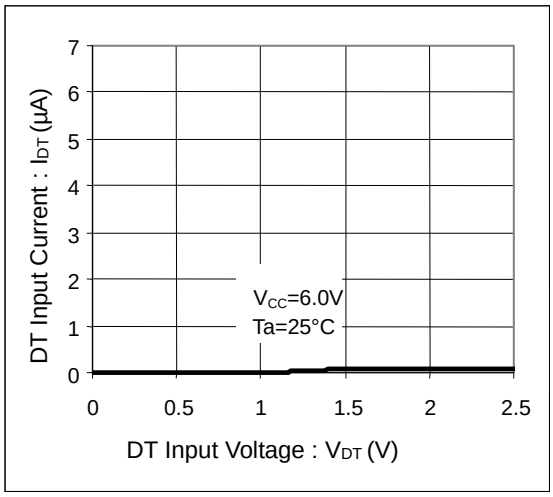


Figure 18. DT Input Bias Current vs DT Input Voltage

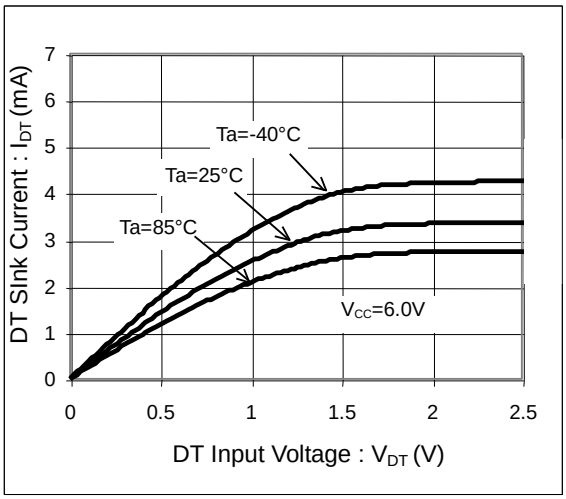


Figure 19. DT Sink Current vs DT Input Voltage

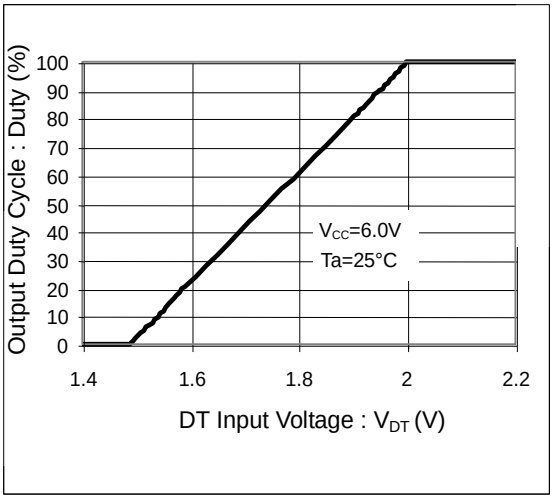


Figure 20. Output Duty Cycle vs DT Input Voltage (100kHz)

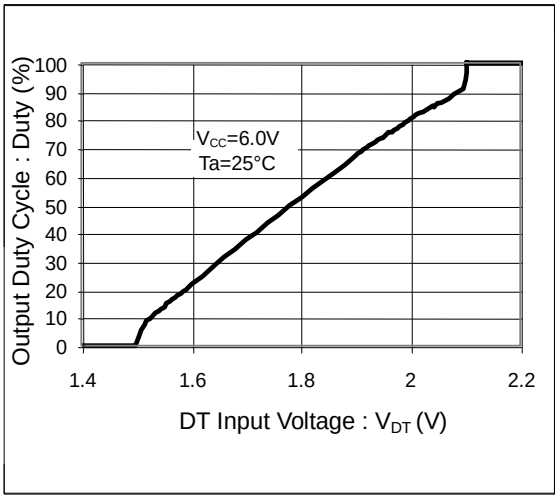


Figure 21. Output Duty Cycle vs DT Input Voltage (1.5MHz)

Typical Performance Curves - continued

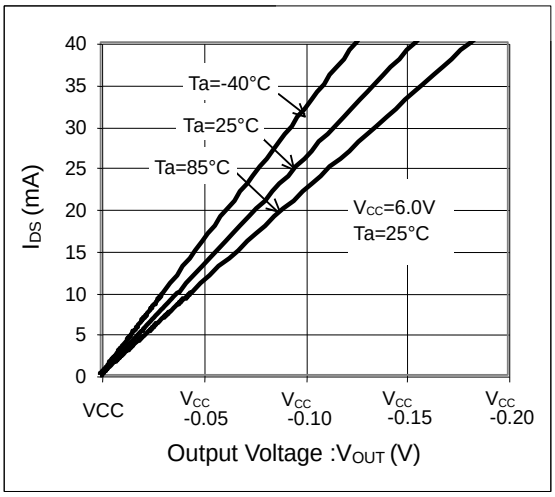


Figure 22. I_{DS} vs Output Voltage
(Output ON Resistance H (R_{ONH}))

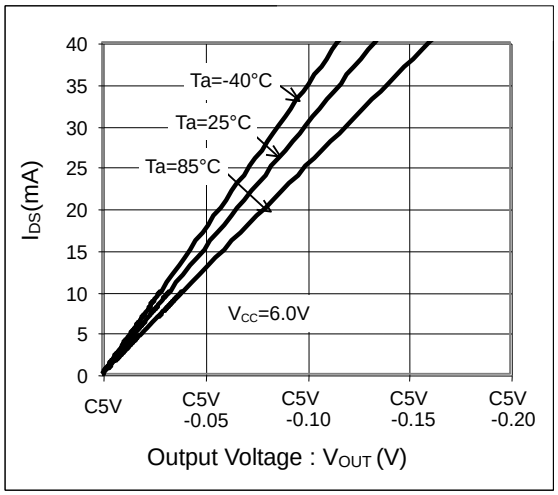


Figure 23. I_{DS} vs Output Voltage
(Output ON Resistance L (R_{ONL}))

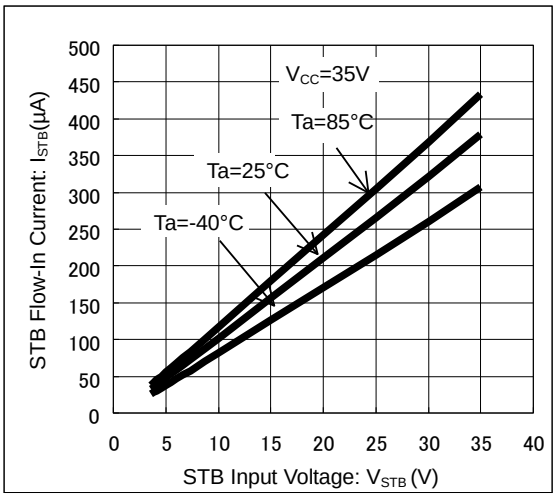


Figure 24. STB Flow-In Current vs STB Input Voltage

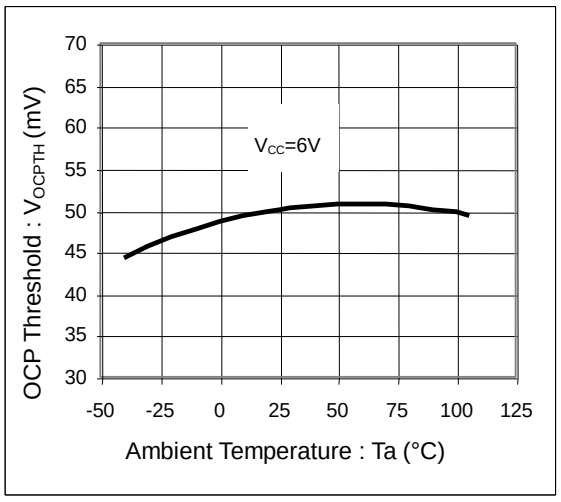


Figure 25. Over-Current Detection Threshold Voltage vs Ambient Temperature

Typical Performance Curves - continued

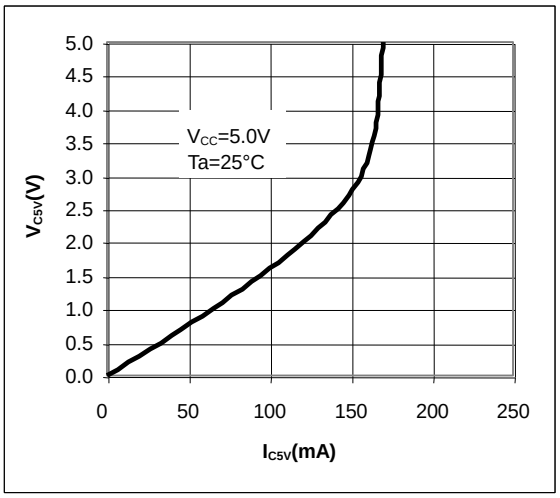


Figure 26. C5V Saturation Voltage

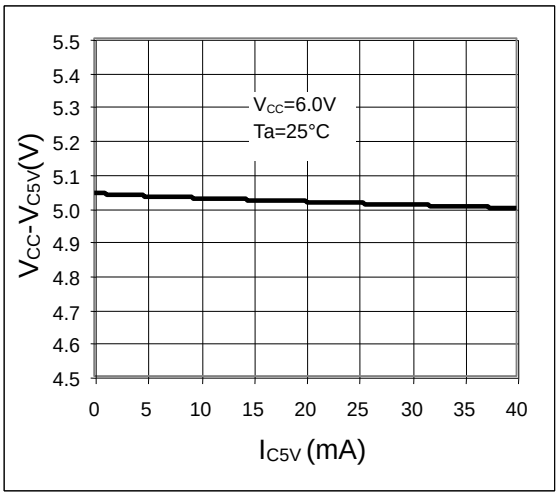


Figure 27. C5V Load Regulation

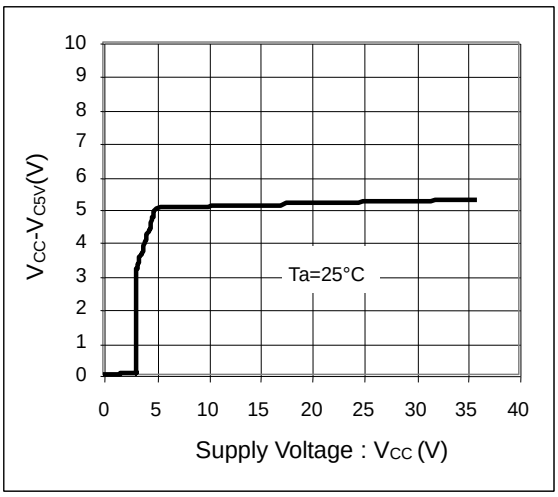


Figure 28. C5V Line Regulation

Application Information

1. Operation Description of Each Block and Function

(1) REG: Reference Voltage Unit

The REG (2.5V) produces a voltage of 2.5V which is more stable than the supply voltage input to VCC terminal. This voltage is used as a reference voltage to the IC's internal circuitry. This voltage is also connected to the VREF terminal. Insert a capacitor of 0.1µF to VREF terminal.

The REG (V_{CC}-5V) produces a voltage of (V_{CC}-5V) which is used as power supply (LDO) of driver circuit (DRV). This voltage is also connected to the C5V terminal. Insert a capacitor of 1µF between VCC and C5V terminals.

(2) ERR Amp: Error Amplifier

In step-down application, the inverting input, INV, of the error amplifier detects output voltage by sending back feedback current from final output stage (on load side) of switching regulator. Resistors R_1 and R_2 that are connected to this input terminal are used for setting the output voltage. The non-inverting input of the amplifier is connected to an internal reference voltage (1.0V).

R_F and C_F, which are connected between FB, the output of the error amplifier, and INV, are for setting of the amplifier's loop gain.

FB is connected to the non-inverting input of PWM Comp.

Setting of output voltage (V_{OUT}) is as follows:

$$V_{OUT} = \frac{R_1 + R_2}{R_2} \times 1.0V$$

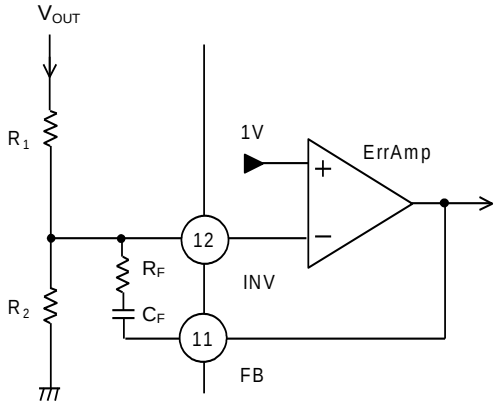


Figure 29

(3) OSC: Triangular Wave Oscillating Unit

This generates a triangular wave which is input to the PWM Comp.

First, timing capacitor, C_{CT}, which is connected between CT terminal and GND, is charged by a constant current of 200 µA which is generated inside the IC. When CT voltage reaches 2.0 V typ, the comparator is switched, and then C_{CT} is discharged by a constant current of 200 µA. Then, when CT voltage reaches 1.5V, the comparator is switched again, and C_{CT} is charged again. This repetition generates the triangular wave.

Oscillation frequency is determined by the externally mounted C_{CT} through the formula below:

$$f_{OSC} \approx I_{CT} / (2 \cdot C_{CT} \cdot \Delta V_{OSC})$$

where:

I_{CT} is the CT sink/source current 200 µA typ

ΔV_{OSC} is the triangular wave amplifying voltage = $(V_{t0} - V_{t100}) = 0.50V$ Typ

The error from the formula is caused by the delay introduced to the internal circuit when operated at a high frequency. See the graph in Figure 30 for the setting.

This triangular wave can be probed through CT terminal. It is also possible to use an external oscillator by switching to slave mode which is described later. Waveform input here in principle must be a triangular wave of Vpeak = (1.5V ⇔ 2.0V) which is equivalent to internal oscillation circuit.

External input voltage range

V_{CT} : 1.4 V < V_{CT} < 2.3 V

Standard external C_{CT} range

C_{CT} : (Min) 47 pF – (Max) 3000 pF

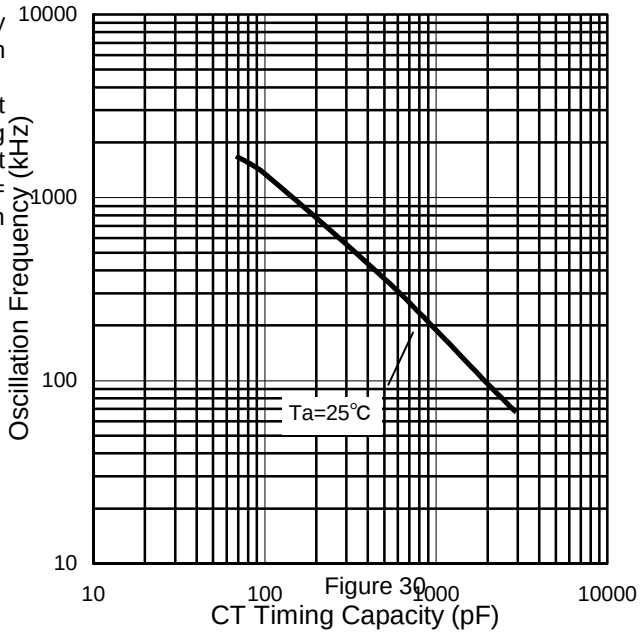


Figure 30

(4) Soft Start : Soft Start Function

It is possible to provide SS terminal (pin 13) with soft start function by connecting C_{SS} as shown in figure 31.
Soft start time t_{SS} is shown by the formula below:

$$t_{SS} = C_{SS} \cdot \frac{V_{INV}}{I_{SSSO}}$$

where:

C_{SS} is the SS terminal connection capacitance

V_{INV} is the Error amplifier reference voltage (1V typ)

I_{SSSO} is the SS source current (2μA typ)

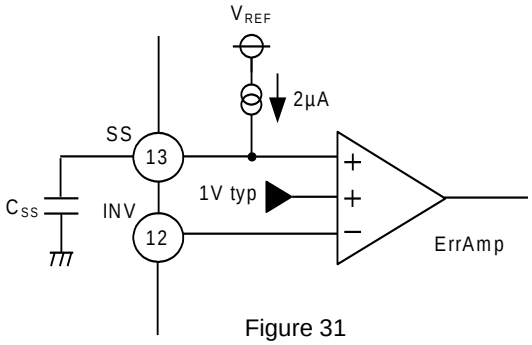


Figure 31

(Ex) When C_{SS} = 0.01 μF

$$t_{SS} = \frac{0.01 \times 10^{-6} \times 1}{2 \times 10^{-6}}$$

$$= 5[\text{msec}]$$

In order for soft start to function, soft start time must be set longer than the start time of power supply and STB.
It is also possible to provide soft start by connecting the resistors (R_1, R_2) and capacitor (C_{DT}) to DT terminal (14pin) as shown in figure 32.

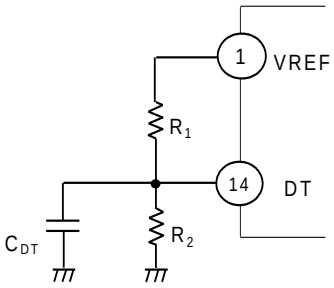


Figure 32

(5) PWM Comp - DEAD TIME: Pause Period Adjusting Circuit - Dead Time

Dead time can be set by applying voltage dividing resistors between VREF and GND to DT terminal.
PWM Comp compares the input dead time voltage (DT terminal voltage) and error voltage from Err Amp (FB terminal voltage) with triangular wave, and turns the output off and on. When dead time voltage < error voltage, duty of output is determined by dead time voltage. (When dead time setting is not used, pull up DT terminal to VREF terminal with resistor approx 10 k ohms.)
Dead time voltage V_{DT} in Figure 31 is shown by the formula below:

$$V_{DT} = V_{REF} \cdot \frac{R_2}{R_1 + R_2}$$

Relation between V_{DT} and Duty [See the graph on the right.]

	Duty 100%			Duty 0%		
	Min	Typ	Max	Min	Typ	Max
When f = 100kHz	1.9	2.0	2.1	1.4	1.5	1.6
When f = 1.5MHz	1.95	2.1	2.25	1.35	1.5	1.65

[Unit : V]

Be careful when oscillation frequency is high, the upper/lower amplitude limit of the triangular wave (V_{th100}/V_{th0}) increases due to the shift in the delay time of the comparator.

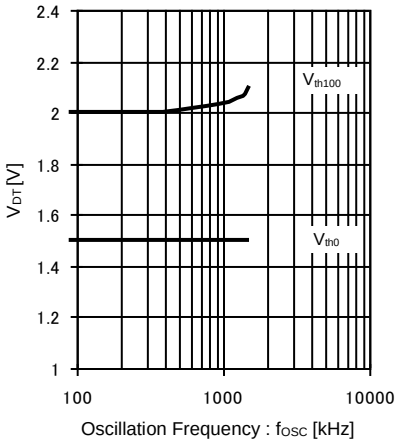


Figure 33

(6) OCP Comp: Over-current Detection Circuit

This function provides protection by forcibly turning off the output when abnormal over-current flows due to shorting of output, etc. When the voltage across the sense resistor, which is between the terminals OCP+(8pin) and OCP-(9pin), exceeds the over-current detection voltage of 50 mV (typ), which is determined as over-current condition, the switching operation is stopped immediately by setting OUT to HIGH and DT, SS and FB to LOW.
Switching operation is automatically restored when the voltage between the terminals OCP+ and OCP- is below over-current detection voltage.
In addition, although hysteresis, etc. are not set here, the minimum detection retention time of 1.6 ms (typ) is set to suppress the heating of FET, etc. (See the timing chart.)
To disable over-current detection, short both OCP+ and OCP- terminals to VCC pin.

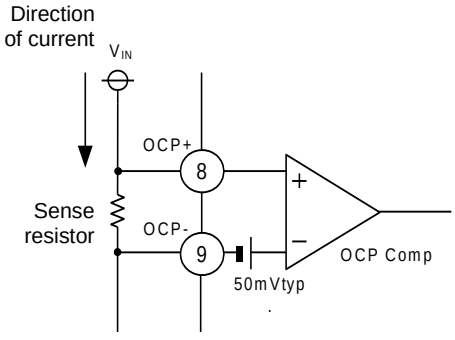


Figure 34

(7) STB /SEL: Standby/Master/Slave Function

Standby mode and normal mode can be switched by STB terminal (4pin).

(a) When STB<0.5V, standby mode is set.
Output stops (OUT=HIGH), REG stops and there is no circuit current (I_{SC} = 0 μA).

(b) When STB>3.0V, normal operation mode is set.
All circuits operate. Use the controller normally in this range.

Master mode and slave mode can be switched by SEL terminal (10pin).

(a) When SEL<0.5V, master mode is set.
All circuits operate.

(b) When SEL>2.0V, slave mode is set.
Operation statusis set, but OSC block is stopped, CT terminal is High-Z here, and triangular wave is not outputted (PWM circuit and protection circuit perform the same operation as usual.). Therefore, if the controller is used in this mode, triangular wave is not outputted, operation is unstable, and normal output cannot be obtained. Be careful when using the IC in this mode.

(8) OUT (Output: External FET Gate Drive)

OUT terminal (6pin) is capable of directly driving the gate of external (PchMOS) FET. Amplitude of output is restricted between VCC and C5V (V_{CC}-5V), and is not restricted by input voltage to gate, which allows broad selection of FET.
However, for precaution when selecting FET, there is a restriction that input capacitance of gate is determined by current capability of C5V and permissible loss of IC. Refer to the permissible range on the graph in figure 35 when determining FET.

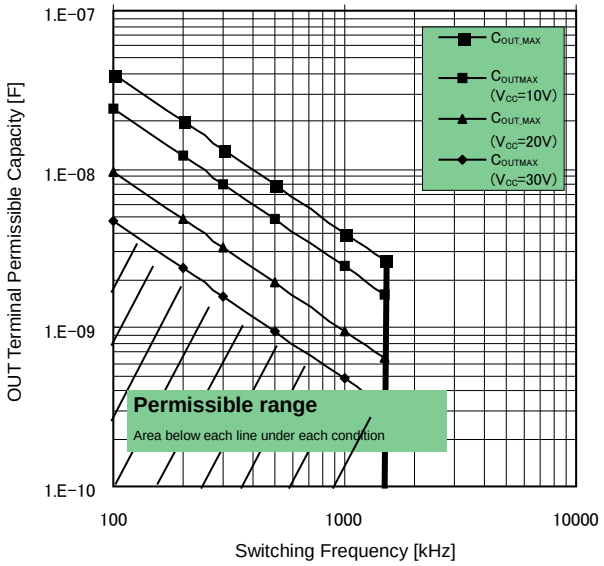


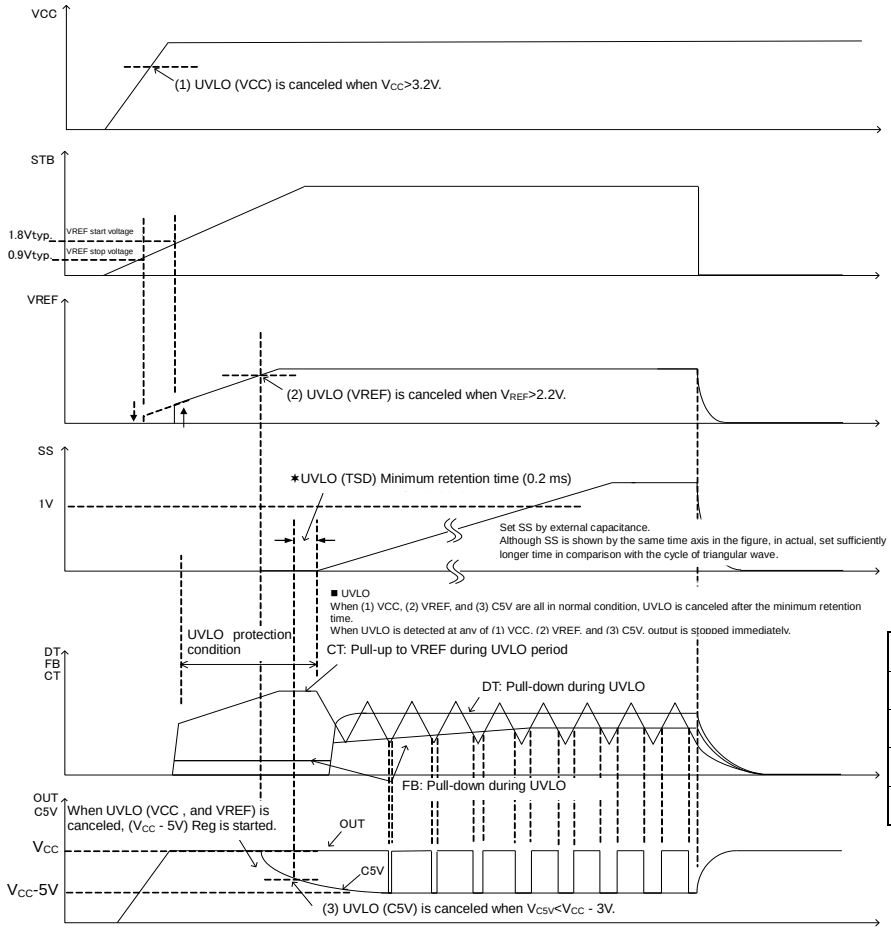
Figure 35

(9) Protection: Other Protection Functions

This IC is equipped with low input malfunction prevention circuit (UVLO) and abnormal temperature protection circuit (TSD) besides over-current detection circuit (OCP).
Low input malfunction prevention circuit is for preventing unstable output when input voltage is low.
Three voltages are monitored: VCC (3.2V), VREF(2.35V), and C5V(V_{CC}-3V), and they have output only when the UVLO for the three voltages are canceled. (See the timing chart.)
Abnormal temperature protection circuit is for protecting the IC from destruction by preventing thermal runaway when the IC is operating above the rated temperature. (It does not operate normally.)
Apply a design with allowable margin for heating in consideration of permissible loss.

2. Timing Chart

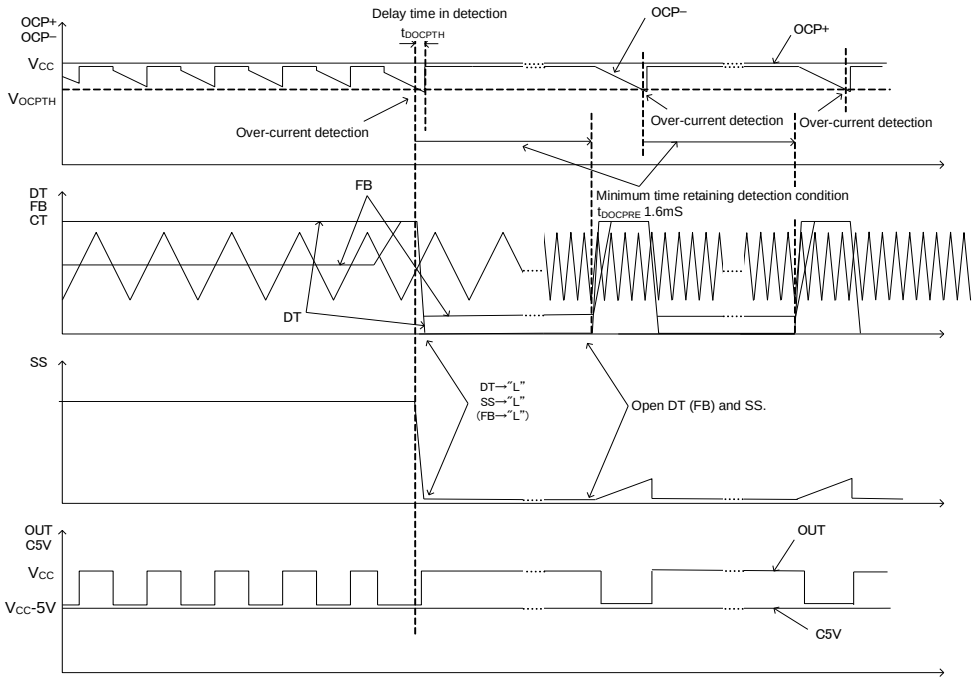
◎ Starting characteristics (UVLO cancel) and standby operation



UVLO Voltage [unit: V]

Item	Min	Typ	Max
Threshold Voltage (VCC)	3.0	3.2	3.4
Hysteresis	-	0.15	0.25
Threshold Voltage (VREF)	2.0	2.2	2.4
Threshold Voltage (C5V)	-	3.0	3.4

◎ Over-current detection (When output is shorted: Over-current detection and cancel are repeated at a specified time interval.)



3. Example of Application Circuit

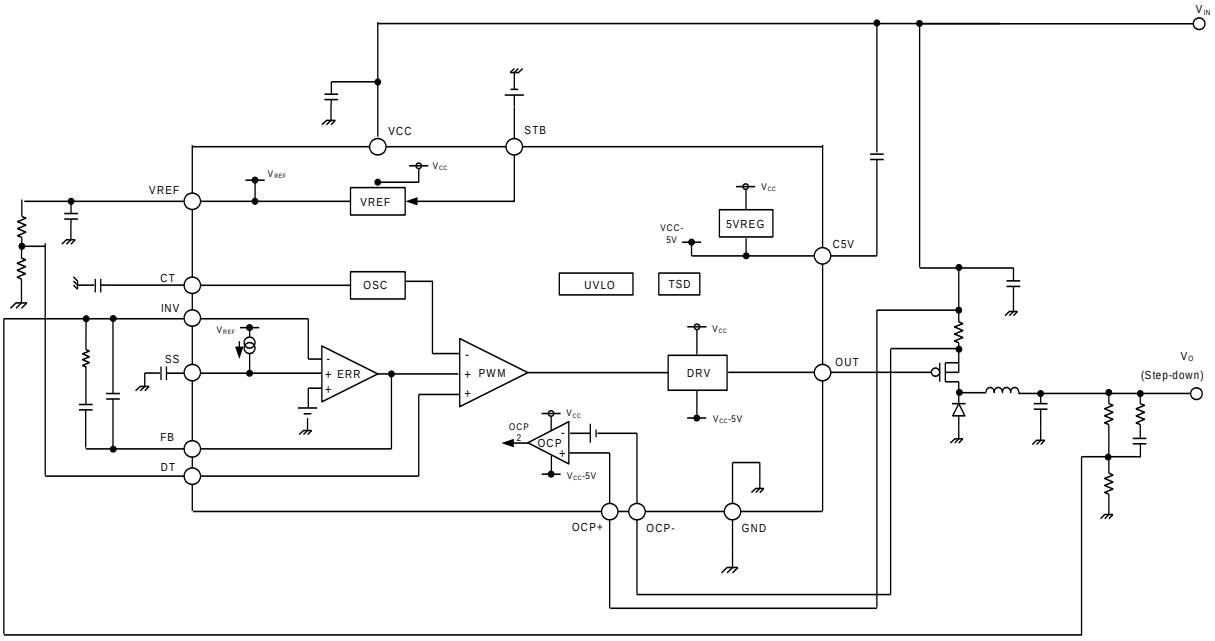


Figure 36

(1) Setting of Output Unit Coil (L) and Capacitor (C_O)

In a step-down application, set the coil and capacitor as follows:

<Setting of L-Value>

When load current gets high, the current flowing through the coil gets continuous, and the relation below is established:

$$L = \frac{t_{SW}}{\Delta I_L} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

where:

V_{IN} is the input voltage

t_{SW} is 1/(switching frequency)

$Delta\ I_L$ is ripple current of coil

Normally set Delta I_L below 30% of the maximum output current (I_{OMAX}).

When L-value is increased, the ripple current (Delta I_L) decreases. In general, the greater the L-value, the smaller the permissible current of coil gets, and when the current exceeds permissible current, the coil is saturated and L-value changes. Contact the coil manufacturer and check permissible current.

<Setting of Output Capacitor C_O>

Select an output capacitor C_O by ESR (equivalent series resistance) property of capacitor.

Output ripple voltage (Delta Vo) is almost the ESR of the output capacitor, therefore,

$$\Delta V_{OUT} \approx \Delta I_L \times ESR$$

where:

ESR is the equivalent series resistance of output capacitor C_O

The relation above is established.

Ripple component of output capacitor is small enough to be neglected in comparison with ripple component of ESR in many cases. As for C_O value, it is recommended to use a sufficiently large capacitor with a capacitance that satisfies ESR condition.

<Switching Element>

Decide the switching element by using the peak current. Peak current I_{SW} <peak> flowing through the switching element is equal to the peak current flowing through the coil, therefore the equation below is established.

$$I_{SW}(peak) = I_{OUT} + \Delta I_L / 2$$

Select a switching element of permissible current and having enough margin over the peak current calculated by the equation above.

For Noise reduction and efficiency improvement, select a FET having an input capacitance(Ciss and Qg), On resistance as small as possible, and a Schottky diode having an inter-terminal capacitance, reverse recovery time trr and forward voltage V_F as small as possible

< Input capacitor C_{IN} >

The bypass capacitor of VCC is used by both electrolytic capacitor and ceramic capacitor. The ceramic capacitor is placed near each channel Pow-FET drain pin as possible because of supplied output switching current instantaneously from input capacitor(C_{IN}).

In case of using an electrolytic capacitor, confirm permissible ripple current.

(2) Example of Over-current Protection Circuit

Insert a sense resistor between the source and VIN of output Pch-FET for detecting over-current as shown in Figure 37.

Refer to the formula below for determining the value of the sense resistor. Provide margin for permissible loss.

$$R_{SENSE} = \frac{V_{OCPTH}}{I_{OCP}}$$

where:

V_{OCPTH} is over-current detection voltage (50 mV typ)

I_{OCP} is over-current detection setting current

I_{OCP} is a peak current I_{SW} (peak) here, and the amperage for output load is an over-current setting amperage minus ripple current component (Delta I_L/2), etc. (See the formula on P16.)

There is a time delay of approximately 200ns from detection until the output is stopped (pulse of approximately 100 ns causes delay time but detection is made), and an error may be caused from the value above. In addition, the input to over-current detection unit is very sensitive that wrong detection due to noise may be possible. When wrong detection occurs, try to eliminate noise by using resistors R_1 and R_2 or capacitors C_1, C_2, C_3, and C_4 shown in Figure 37.

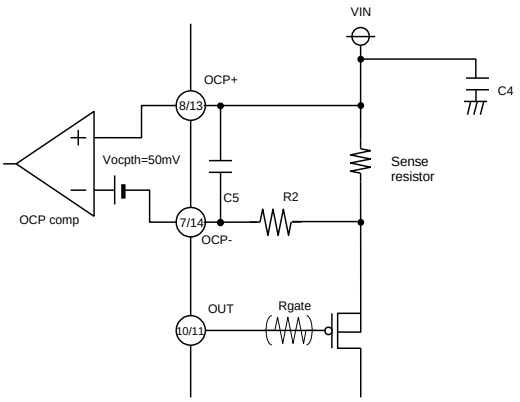


Figure 37

◆ To take measure to switching noise for OCP+/- input.

The input of over current protection(OCP) block is too sensitive to stop each ON pulse for protecting external components. The response time of OCP is about 100nsec(Max 200nsec) , but OCP block can respond at 20nsec to 30nsec to bigger pulse.

Therefore, it is possible to miss-operate by switching noise. (See Figure 38)

To prevent miss-operation of OCP, a low pass filter should be insert in OCP+ and OCP- pins.(Refer Figure 37) When cut off frequency of the low pass filter decreases, OCP- voltage become blunt, and it prevents to miss-operates OCP detection from turning on switching noise. But, in over-decreasing, the detection current level is bigger. In most cases, it is set R2=10ohm to 47ohm , C5=1000pF to 2200pF, and cut off frequency is over 10 times of OSC frequency.

In case the effect of inserting low pass filter is not enough, the switching noise must decrease on application board to use below item.

- High current pattern must be shorted as possible on PCB.
- Bypass capacitor C4 is nearly and using high value.
- Using Gate resister Rgate.

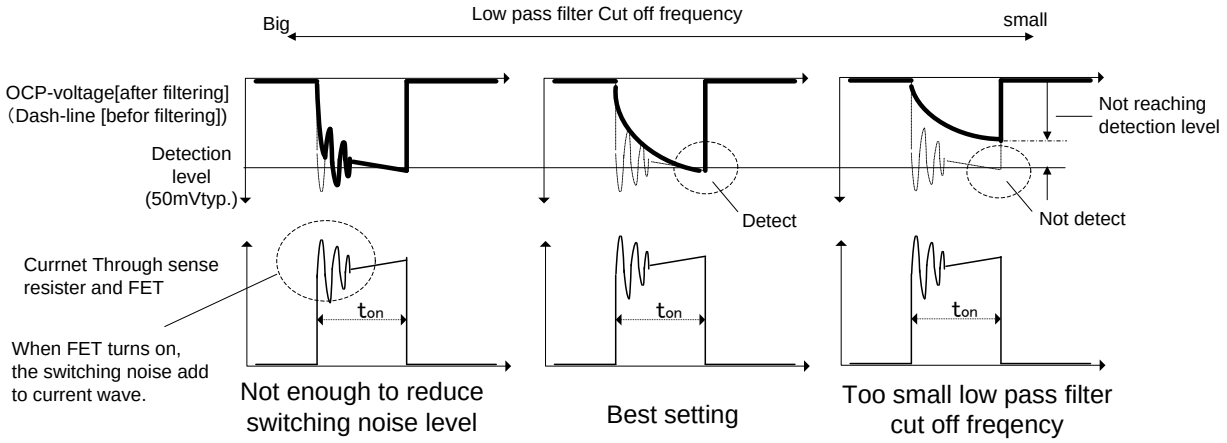


Figure 38

Other attention, the voltage between VCC and OCP+/OCP- pin must be under 0.2V. So the capacitor must be not connected between OCP+/- and GND pin. Common mode differential input range of OCP+/OCP- is provided from Vcc+0.7V to Vcc-2.5V.

(3) Example of Master/Slave (Sync Multi-Ch Output) Operation Circuit

This IC is set to slave mode by setting the input of STB terminal at 2.5V±0.1V, and multi-channel output is enabled with frequency synchronized. (Figure 39) However, CT terminal has a high impedance in slave mode , and triangular wave is generated by CT waveform of master mode IC. Therefore the example of master/slave circuit below is recommended to avoid malfunction by start/stop timing of master IC and slave IC. As for output, it is recommended to control ON/OFF reliably with DT terminal.

Also, oscillation frequency is determined by capacitor (C_{CT}) connected to CT. When the slave ICs are large in number and oscillation frequency is high, parasitic capacitance due to board wiring in contact with CT cannot be ignored, and preset frequency may drift. Care must be considered.

An example of master/slave circuit configuration is shown below.

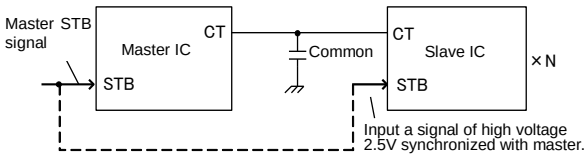


Figure 39

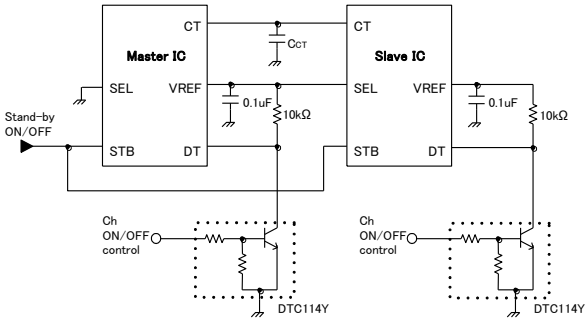


Figure 40. Example of Master/Slave

(4) About Board Layout

In order to make full use of the IC's performance, fully understand the items below besides the general precautions.

(a) OCP+/OCP- outputs are sensitive. Please refer to (2)Example of Over-current Protection Circuit

(b) Try to make the wiring as short as possible to avoid noise and keep away from noise line(Especially OCP+/-,FB and CT are sensitive lines) .

(c) Please put layout for dummy pattern of C,R around OCP and phase compensation circuit.

(d) Switching of large current is likely to generate noise. Try to make the large current route (VIN, Rsense, FET, L, Di, and Cout) as thick and short as possible, and try to apply one-point grounding for GND. OUT terminal is also a switching line, and it must be wired as short as possible. (When multi-layer board is used, shielding by intermediate layer also seems to be effective.)

(e) Please put Bypass capacitors nearby IC and FET/Di.

(f) C_{CT} and C_{VREF} are voltage references, so they must be wired with the shortest distance to GND to be protected against external influence.

(g) The VCC and GND nodes should both be wide to reduce line impedance and to keep the noise and voltage drop low.So be careful not to allow common impedance to GND lines of sensitive functions(Ex. Capacitor of CT and VREF).

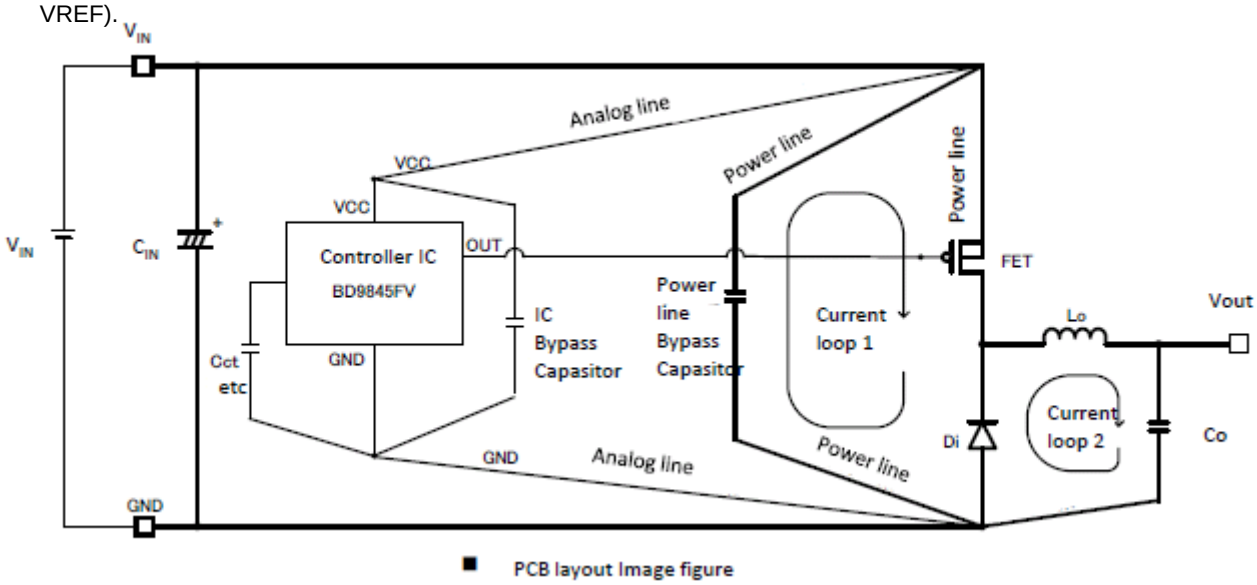
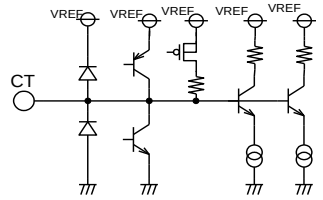
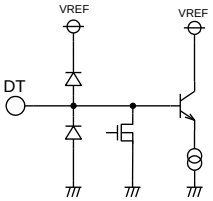
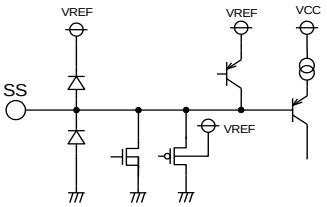
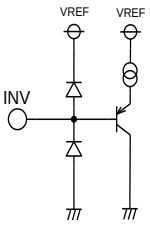
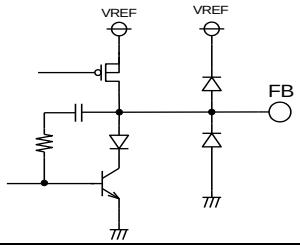
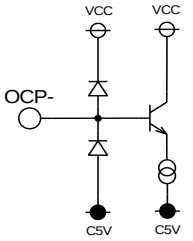
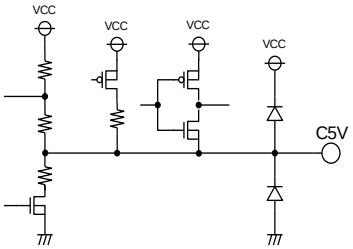
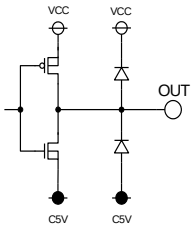
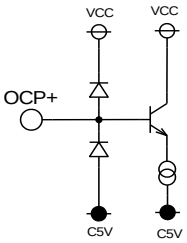
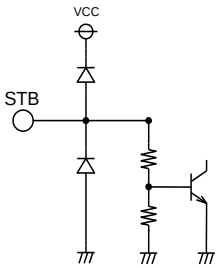
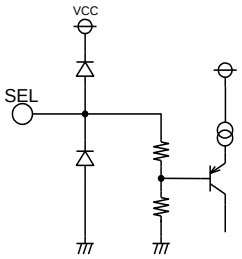
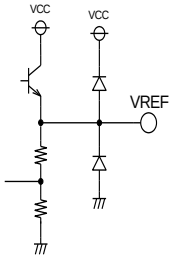


Figure 41

When only one channel is used, connect unused channels as shown above.

I/O Equivalent Circuit

2pin(CT)	14pin (DT)	13pin (SS)
		
12pin (INV)	**11pin (FB)**	**9pin (OCP-)**
		
5pin (C5V)	**6pin (OUT)**	**8pin (OCP+)**
		

4pin (STB)	10pin (SEL)	1pin (VREF)	3pin (GND) , 7pin (VCC)
			

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. **Regarding the Input Pin of the IC**
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

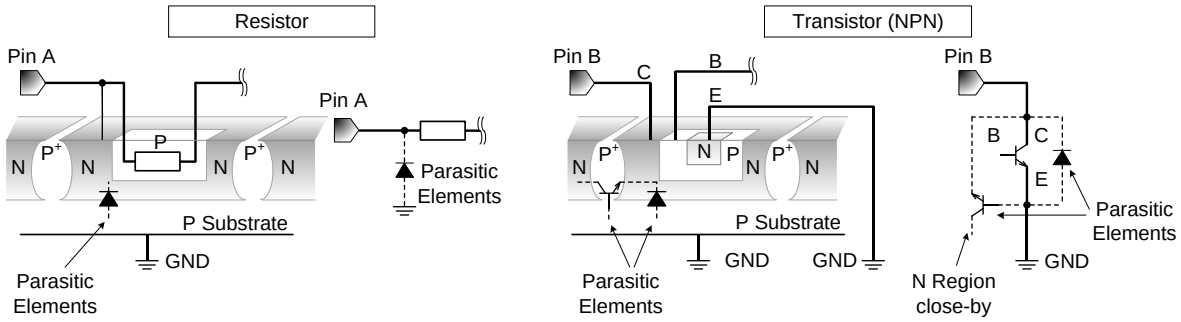
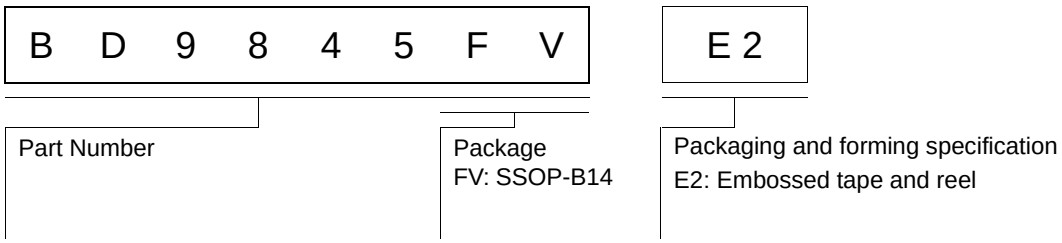
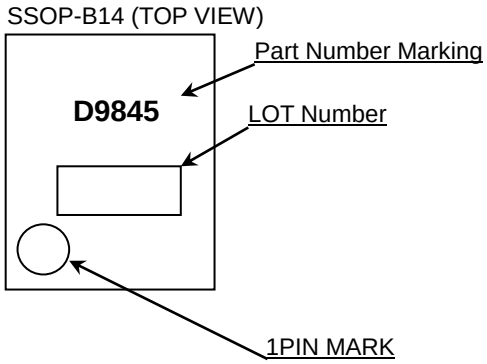


Figure 42. Example of monolithic IC structure

Ordering Information

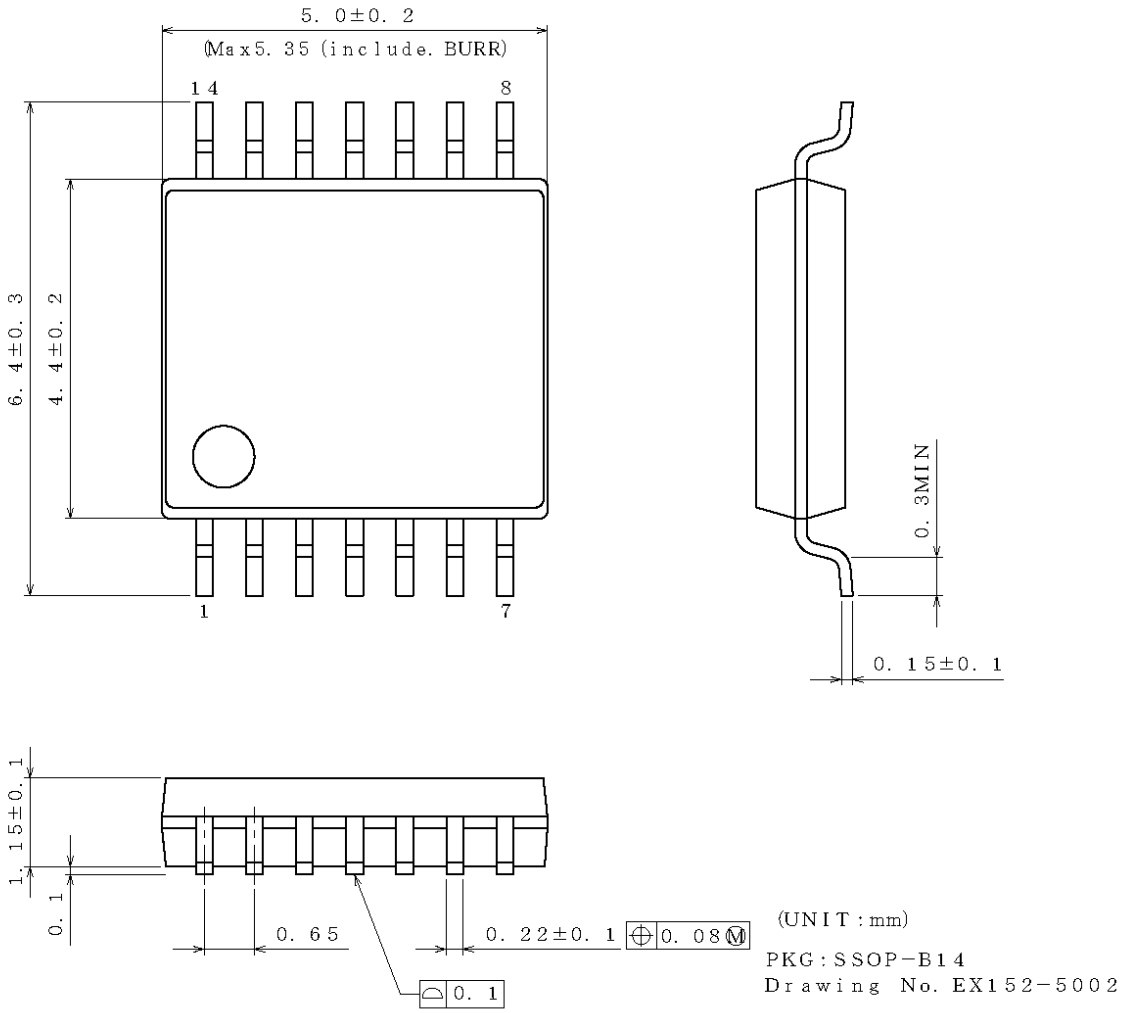


Marking Diagram



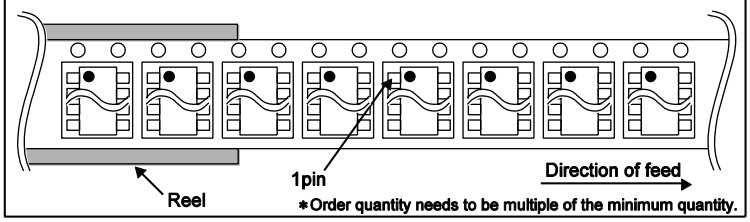
Physical Dimension, Tape and Reel information

Package Name	SSOP-B14



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
06.Nov.2015	001	New Release

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

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3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

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General Precaution

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