FAIRCHILD SEMICONDUCTOR®

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SG5851A
Low-Cost, Green-Mode, PWM Controller for Flyback Converters

Features

- Green-Mode PWM
- Supports the “Blue Angel” Standard
- Low Startup Current: 9μA
- Low Operating Current: 3mA
- Leading-Edge Blanking
- Constant Output Power Limit
- Universal Input
- Built-in Synchronized Slope Compensation
- Current Mode Operation
- Cycle-by-cycle Current Limiting
- Under-Voltage Lockout (UVLO)
- Programmable PWM Frequency with Frequency Hopping
- V_{DD} Over-Voltage Protection (Auto Restart)
- Gate Output Voltage Clamped at 17V
- Low Cost
- Few External Components Required

Applications

- Power Adaptors
- Open-Frame SMPS

Description

This highly integrated PWM controller provides several enhancements designed to meet the low standby-power needs of low-power SMPS. To minimize standby power consumption, the proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency under light-load conditions. This green-mode function enables the power supply to meet power conservation requirements.

The BiCMOS fabrication process enables reducing the startup current to 9μA and the operating current to 3mA. To further improve power conservation, a large startup resistance can be used. Built-in synchronized slope compensation ensures the stability of peak-current-mode control. Proprietary internal compensation provides a constant output power limit over a universal AC input range ($90V_{AC}$ to $264V_{AC}$). Pulse-by-pulse current limiting ensures safe operation even during short circuits.

To protect the external power MOSFET from being damaged by supply over voltage, the output driver is clamped at 17V. SG5851A controllers, available in an SOP package, can be used to improve the performance and reduce the production cost of power supplies.

Ordering Information

Part Number	Operating Temperature Range	Package	Eco Status	Packing Method
SG5851ASY	-40°C to +105°C	8-pin Small Outline Package (SOP)	Green	Tape & Reel
SG5851ADY	-40°C to +105°C	8-pin Dual in-line Package (DIP)	Green	Tube

For Fairchild’s definition of “green” Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Application Diagram

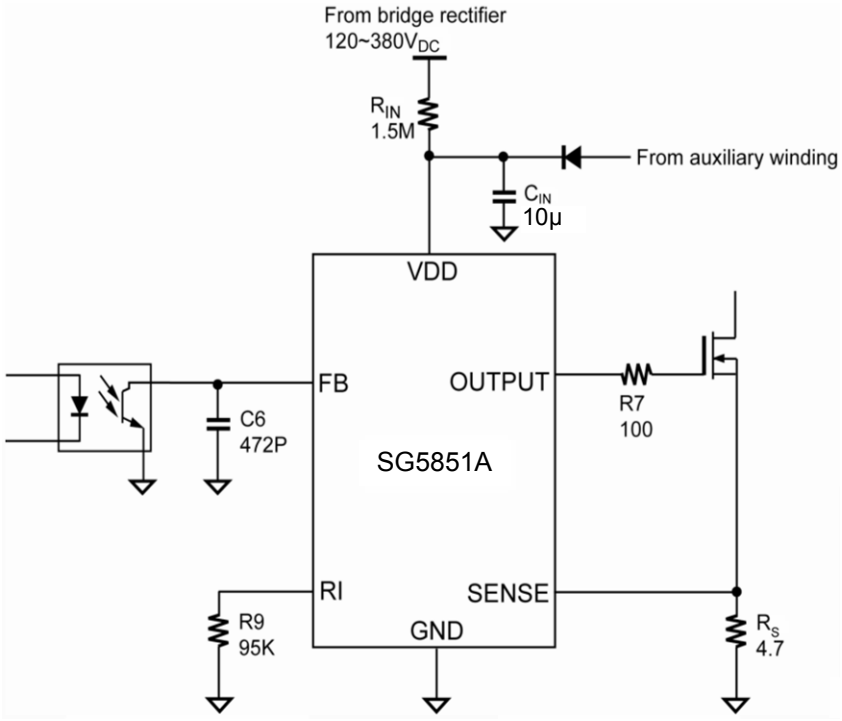


Figure 1. Typical Application

Block Diagram

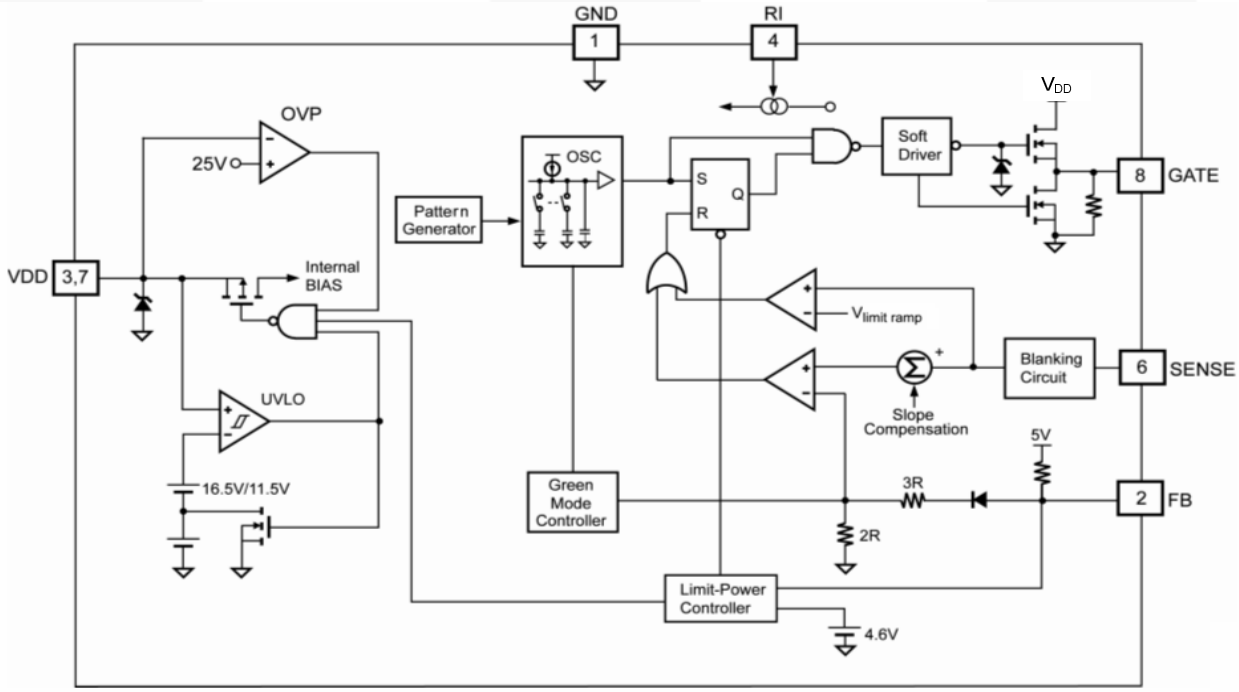
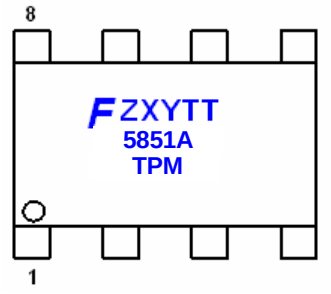


Figure 2. Function Block Diagram

Marking Information



F- Fairchild logo
Z- Plant code
X- 1 digit year code
Y- 1 digit week code
TT: 2 digits die run code
T: Package type (S=SOP, D=DIP)
P: Y: Green compound
M: Manufacture flow code

Figure 3. Marking Information

Pin Configuration

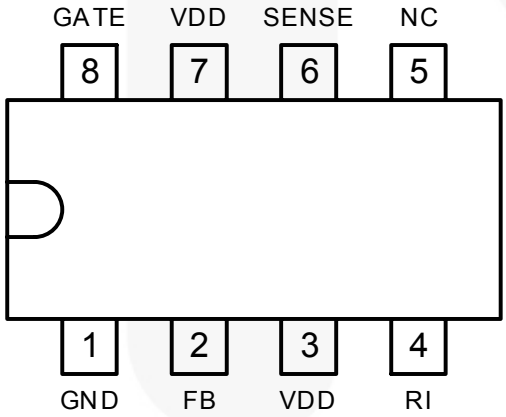


Figure 4. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	GND	**Ground**
2	FB	**Feedback**
3	VDD	**Power Supply**
4	RI	**Reference Setting**. A resistor connected from the RI pin to ground generates a constant current source used to charge an internal capacitor and determine the switching frequency. Increasing the resistance reduces the amplitude of the current source and reduces the switching frequency. A 95kΩ resistor, R_I, results in a 13μA constant current, I_I, and a 70kHz switching frequency.
5	NC	**No Connection**
6	SENSE	**Current Sense**. This pin senses the voltage across a resistor. When the voltage reaches the internal threshold, PWM output is disabled. This activates over-current protection. This pin also provides current amplitude information for current-mode control.
7	VDD	**Power Supply**
8	GATE	**Driver Output**. The totem-pole output driver for driving the power MOSFET.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltage, are given with respect to GND pin. Stresses beyond those listed under “absolute maximum ratings “may cause permanent damage to the device.

Symbol	Parameter	Min.	Max.	Unit
V_{VDD}	DC Supply Voltage		30	V
V_{FB}	Input Voltage to FB Pin	-0.3	7.0	V
V_{SENSE}	Input Voltage to Sense Pin	-0.3	7.0	V
P_D	Power Dissipation		300	mW
T_J	Operating Junction Temperature		+150	°C
θ_{JA}	Thermal Resistance (Junction-to-Air)		141	°C/W
T_{STG}	Storage Temperature Range	-55	+150	°C
T_L	Lead Temperature (Wave soldering, or IR 10 seconds)		+260	°C
ESD	Electrostatic Discharge Capability, Human Body Model, JESD22-A114		3.0	KV
	Electrostatic Discharge Capability, Machine Model, JESD22-A115		200	V

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Ambient Temperature	-40		+105	°C

Electrical Characteristics

V_{DD}=15V, T_A=25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD} Section						
V_{DD-OP}	Continuous Operation Voltage				22	V
V_{DD-ON}	Turn-on Threshold Voltage		15.5	16.5	17.5	V
V_{DD-OFF}	Turn-off Threshold Voltage		10.5	11.5	12.5	V
I_{DD-ST}	Startup Current	V_{DD}=V_{DD-ON} – 0.1V		9	15	µA
I_{DD-OP}	Operating Supply Current	V_{DD}=15V, GATE with 1nF to GND		3.0	3.5	mA
V_{DD-OVP}	V_{DD} Over-Voltage Protection Level	Auto Restart	24	25	26	V
$t_{D-VDDOVP}$	V_{DD} Over-Voltage Protection Debounce	Auto Restart		100		µs
Feedback Input Section						
$V_{FB-OPEN}$	FB Output High Voltage		5			V
V_{FB-OL}	FB Open-loop Trigger Level		4.3	4.6	4.9	V
t_{D-OLP}	Delay Time of FB Pin Open-Loop Protection			56		ms
V_{FB-N}	Green-Mode Entry FB Voltage		2.60	2.85	3.10	V
V_{FB-G}	Green-Mode Ending FB Voltage			2.2		V
S_G	Green-Mode Modulation Slope	R_I=95KΩ	40	70	100	Hz/mV
V_{OZ-OFF}	FB Threshold Voltage for Zero-Duty			1.75		V
Current-Sense Section						
Z_{SENSE}	Input Impedance		10			KΩ
t_{PD}	Delay to Output	V_{DD}=13.5 to 22V	40	55	100	ns
V_{STHFL}	Flat Threshold Voltage for Current Limit			1		V
V_{STHVA}	Valley Threshold Voltage for Current Limit		0.75	0.80	0.85	V
t_{LEB}	Leading-Edge Blanking Time		250	310	370	ns
DCY_{SAW}	Duty Cycle of SAW Limit	Maximum Duty Cycle		45		%
Oscillator Section						
f_{OSC}	Center Frequency	R_I=95KΩ	65	70	75	KHz
	Hopping Range			±4.9		
t_{HOP}	Hopping Period	R_I=95KΩ		3.7		ms
f_{OSC-G}	Green-Mode Frequency	R_I=95KΩ		22		KHz
f_{DV}	Frequency Variation vs. V_{DD} Deviation	V_{DD}=13.5 to 22V	0	0.2	2.0	%
f_{DT}	Frequency Variation vs. Temperature Deviation	T_A=-20 to +85°C			2	%

Continued on the following page…

Electrical Characteristics

V_{DD}=15V, T_A=25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Output Section						
DCY_{MAX}	Maximum Duty Cycle		70	75	80	%
V_{GATE-L}	Output Voltage Low	V_{DD}=15V, I_O=20mA			1.5	V
V_{GATE-H}	Output Voltage High	V_{DD}=13.5V, I_O=20mA	8			V
t_r	Rising Time	V_{DD}=15V, C_L=1nF		120		ns
t_f	Falling Time	V_{DD}=15V, C_L=1nF		65		ns
$V_{GATE-CLAMP}$	Output Clamp Voltage	V_{DD}=22V	16	17	18	V

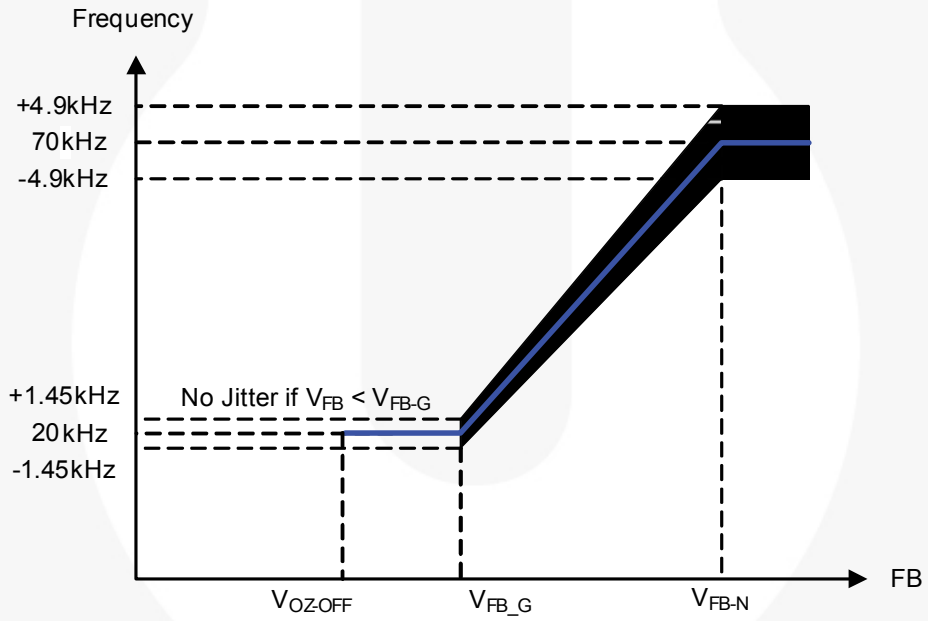


Figure 5. PWM Frequency

Functional Description

SG5851A devices integrate many useful designs into one controller for low-power, switch-mode, power supplies. The following descriptions highlight some of the features of the SG5851A series.

Startup Current

The startup current is only 9μA, which allows a startup resistor with a high resistance and a low-wattage to supply the startup power for the controller. A 1.5MΩ, 0.25W, startup resistor and a 10μF/25V V_{DD} hold-up capacitor are sufficient for an AC-to-DC power adapter with a wide input range ($90V_{AC}$ to $264V_{AC}$).

Operating Current

The operating current has been reduced to 3mA, which results in higher efficiency and reduces the V_{DD} hold-up capacitance requirement.

Green-Mode Operation

The proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency under light-load conditions. On-time is limited to provide stronger protection against brownouts and abnormal conditions. The feedback current, which is sampled from the voltage feedback loop, is taken as the reference. Once the feedback current exceeds the threshold current, the switching frequency starts to decrease. Green mode dramatically reduces power consumption under light-load and zero-load conditions. Power supplies using SG5851A meet even the strictest regulations regarding standby power consumption.

Oscillator Operation

A resistor connected from the RI pin to ground generates a constant current source used to charge an internal capacitor. The charge time determines the internal clock speed and the switching frequency. Increasing the resistance reduces the amplitude of the input current and reduces the switching frequency. A 95kΩ resistor, R_I, results in a 13μA constant current, I_I, and a 70kHz switching frequency. The relationship between R_I and the switching frequency is:

$$f_{PWM} = \frac{6650}{R_I(k\Omega)}(kHz) \quad (1)$$

The range of the oscillation frequency is designed to be within 50kHz ~ 80kHz.

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs at the sense-resistor. To avoid premature termination of the switching pulse, a 310ns leading-edge blanking time is built in. Conventional RC filtering can therefore be omitted. During this blanking period, the current-limit comparator is disabled and it cannot switch off the gate driver.

Constant Output Power Limit

When the SENSE voltage across the sense resistor, R_S, reaches the threshold voltage (~1.00V), the output GATE drive is turned off after propagation delay, t_{PD}. This propagation delay introduces an additional current proportional to $t_{PD} \bullet V_{IN}/L_p$. The propagation delay is nearly constant regardless of the input line voltage V_{IN}. Higher input line voltages result in larger additional currents. At high input line voltages, the output power limit is higher than at low input line voltages.

To compensate for this output power limit variation across a wide AC input range, the threshold voltage is adjusted by adding a positive ramp. This ramp signal rises from 0.80V to 1.00V, then flattens out at 1.00V. A smaller threshold voltage forces the output GATE drive to terminate earlier. This reduces the total PWM turn-on time and makes the output power equal to that of low-line input. This proprietary internal compensation ensures a constant output power limit for a wide AC input voltage range ($90V_{AC}$ to $264V_{AC}$).

Under-Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 16.5V and 11.5V. During startup, the hold-up capacitor must be charged to 16.5V through the startup resistor to enable SG5851A. The hold-up capacitor continues to supply V_{DD} until power can be delivered from the auxiliary winding of the main transformer. V_{DD} must not drop below 11.5V during the startup process. This UVLO hysteresis window ensures that the hold-up capacitor is adequate to supply V_{DD} during startup.

Gate Output

The BiCMOS output stage is a fast totem-pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 17V Zener diode to protect power MOSFET transistors against undesired over-voltage gate signals.

Built-in Slope Compensation

The sensed voltage across the current sense resistor is used for current mode control and pulse-by-pulse current limiting. Built-in slope compensation improves stability and prevents sub-harmonic oscillations due to peak-current-mode control. The SG5851A has a synchronized, positively-sloped ramp built-in at each switching cycle. The slope of the ramp is:

$$\frac{0.36 \times Duty}{Duty(\max.)} \quad (2)$$

Noise Immunity

Noise from the current sense or the control signal can cause significant pulse-width jitter, particularly in continuous-conduction mode. While slope compensation helps alleviate these problems, further precautions should be taken. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the SG5851A, and increasing power MOS gate resistance improve performance.

Typical Performance Characteristics

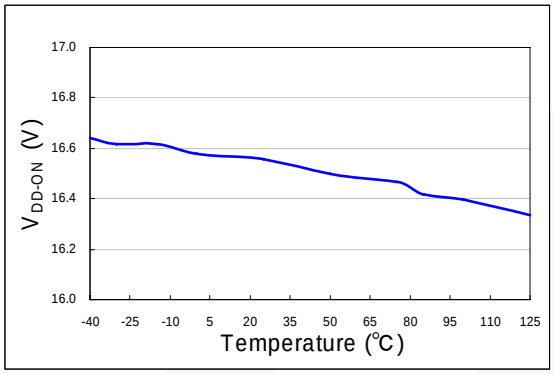


Figure 6. V_{DD-ON} vs. T_A

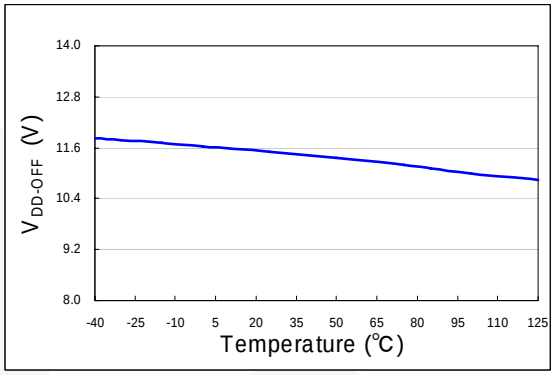


Figure 7. V_{DD-OFF} vs. T_A

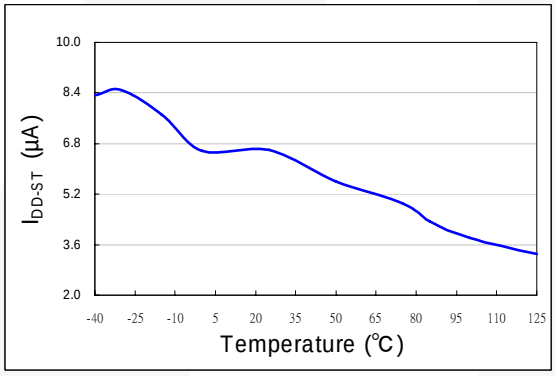


Figure 8. I_{DD-ST} vs. T_A

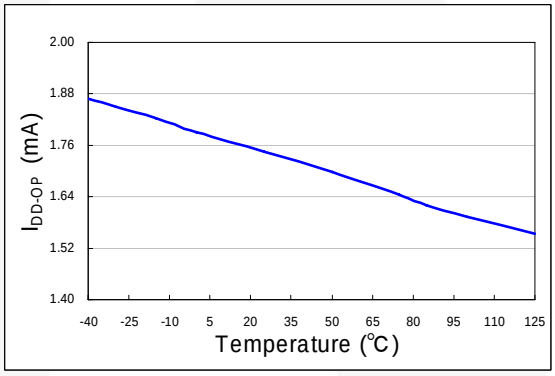


Figure 9. I_{DD-OP} vs. T_A

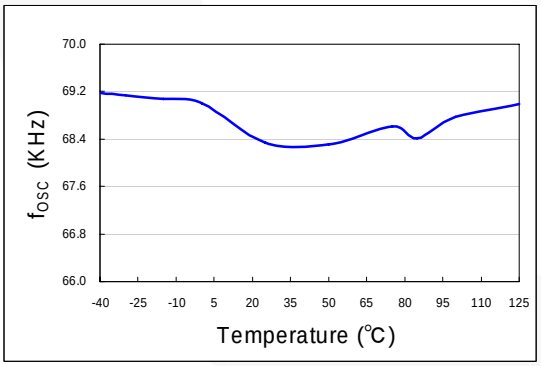


Figure 10. f_{OSC} vs. T_A

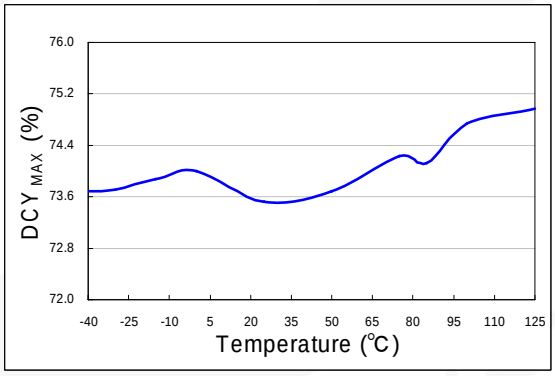


Figure 11. DCY_{MAX} vs. T_A

Typical Performance Characteristics (Continued)

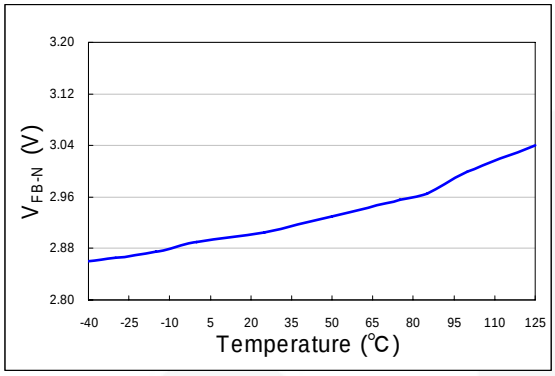


Figure 12. V_{FB-N} vs. T_A

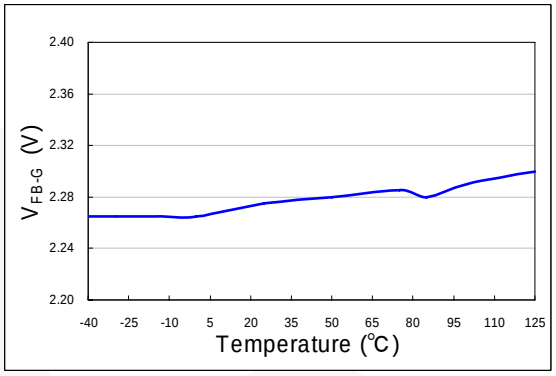


Figure 13. V_{FB-G} vs. T_A

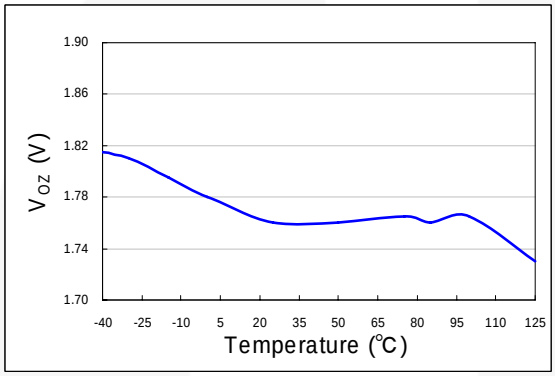


Figure 14. V_{OZ} vs. T_A

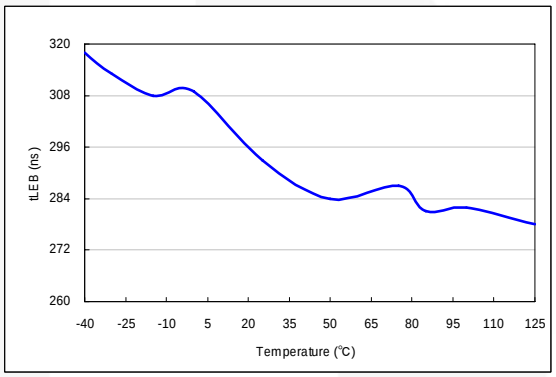
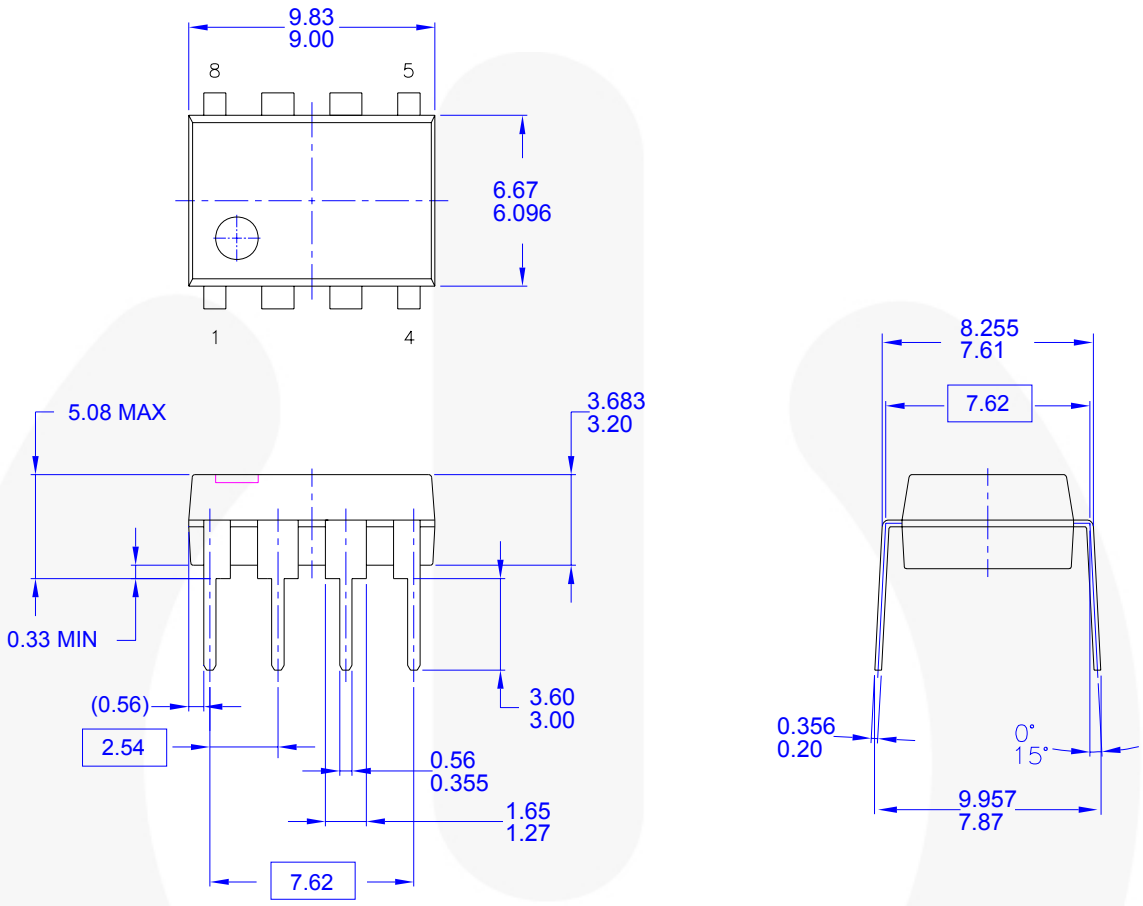


Figure 15. t_{LEB} vs. T_A

Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

E) DRAWING FILENAME AND REVSION: MKT-N08FREV2.

Figure 16. 8-Lead, PDIP, JEDEC MS-001, .300 Inch Wide

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Mechanical Dimensions (Continued)

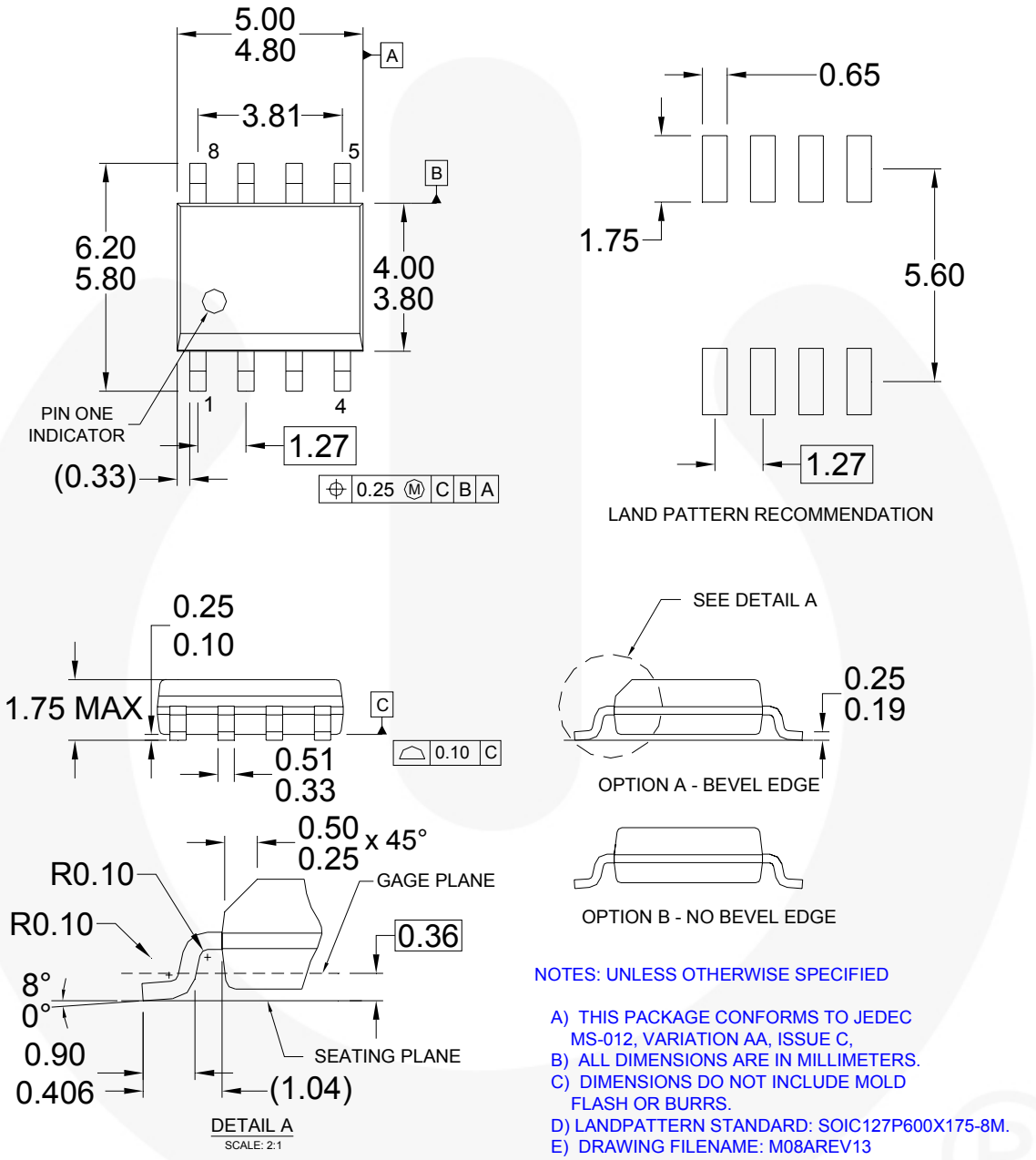

Figure 17. 8-Lead, SOIC,JEDEC MS-012, .150 Inch Narrow Body

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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