NCP4683

300 mA, Low Dropout Regulator

The NCP4683 is a CMOS Linear voltage regulator with 300 mA output current capability. The device has high output voltage accuracy, low supply current and high ripple rejection. The NCP4683 is easy to use, with output current fold−back protection circuit included. A Chip Enable function is included to save power by lowering supply current. The line and load transient responses are very good, thus this regulator is suitable for use as a power supply for communication equipment.

Features

- Operating Input Voltage Range: 1.40 V to 5.25 V
- Output Voltage Range: 0.8 V to 3.6 V (available in 0.1 V steps)
- Output Voltage Accuracy: ±1.0% (V_{OUT} > 2.0 V)
- Supply Current: 50 μA
- Dropout Voltage: 0.25 V (I_{OUT} = 300 mA, V_{OUT} = 2.8 V)
- High PSRR: 70 dB (f = 1 kHz)
- Line Regulation: 0.02%/V Typ.
- Stable with Ceramic Capacitors: 1.0 μF or more
- Current Fold Back Protection
- Available in UDFN4 1.0 x 1.0 mm, SC−70, SOT23 Packages
- These are Pb−Free Devices

Typical Applications

- Battery−powered Equipment
- Networking and Communication Equipment
- Cameras, DVRs, STB and Camcorders
- Home Appliances

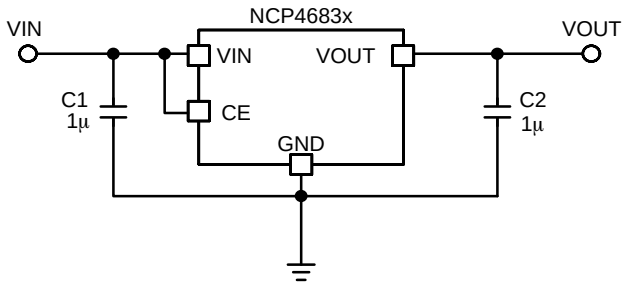

Figure 1. Typical Application Schematic

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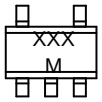
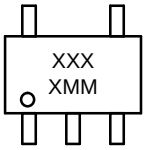
MARKING DIAGRAMS

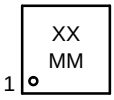
SOT−23−5
CASE 1212



SC−70
CASE 419A



UDFN4
CASE 517BR



XX, XXX, XXXX = Specific Device Code
M, MM = Date Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 18 of this data sheet.

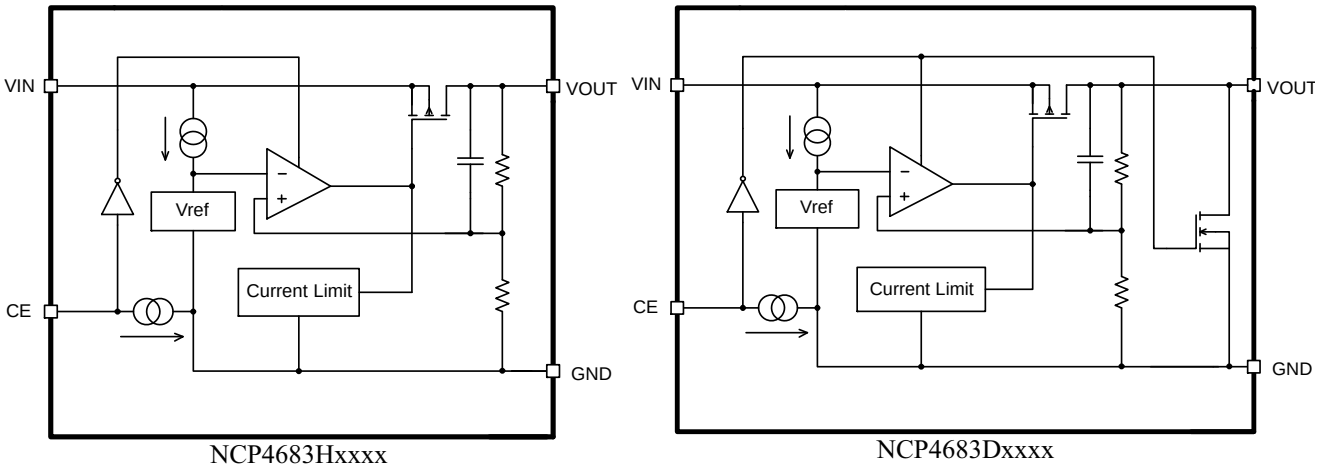


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. UDFN1010*	Pin No. SC−70	Pin No. SOT23	Pin Name	Description
1	4	5	V_{OUT}	Output pin
2	3	2	GND	Ground
3	1	3	CE	Chip enable pin (Active “H”)
4	5	1	V_{IN}	Input pin
−	2	4	NC	No connection

*Tab is GND level. (They are connected to the reverse side of this IC.
The tab is better to be connected to the GND, but leaving it open is also acceptable.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	6.0	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} + 0.3	V
Chip Enable Input	V_{CE}	−0.3 to 6.0	V
Output Current	I_{OUT}	400	mA
Power Dissipation UDFN1010	P_D	400	mW
Power Dissipation SC−70		380	
Power Dissipation SOT23		420	
Junction Temperature	T_J	−40 to 150	°C
Storage Temperature	T_{STG}	−55 to 125	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, UDFN 1.0 x 1.0 mm Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	250	°C/W
Thermal Characteristics, SOT23 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	238	°C/W
Thermal Characteristics, SC−70 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	263	°C/W

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 85°C$; $V_{IN} = V_{OUT(NOM)} + 1$ V or 2.5 V, whichever is greater; I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 1.0 μF, unless otherwise noted. Typical values are at T_A = +25°C.

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	1.40		5.25	V
Output Voltage	T_A = +25°C	$V_{OUT} \ge 2.0$ V	V_{OUT}	x0.99		x1.01	V
		$V_{OUT} < 2.0$ V		−20		20	mV
	$-40°C \le T_A \le 85°C$	$V_{OUT} \ge 2.0$ V		x0.97		x1.03	V
		$V_{OUT} < 2.0$ V		−60		60	mV
Output Voltage Temp. Coefficient	$-40°C \le T_A \le 85°C$		$\Delta V_{OUT}/\Delta T_A$		±80		ppm/°C
Line Regulation	$V_{OUT(NOM)} + 0.5$ V $\le V_{IN} \le 5.0$ V		$Line_{Reg}$		0.02	0.10	%/V
Load Regulation	I_{OUT} = 1 mA to 300 mA		$Load_{Reg}$		15	40	mV
Dropout Voltage	I_{OUT} = 300 mA	V_{OUT} = 0.8 V	V_{DO}		0.56	0.72	V
		V_{OUT} = 0.9 V			0.51	0.65	
		$1.0 \le V_{OUT} < 1.2$ V			0.46	0.59	
		$1.2 \le V_{OUT} < 1.4$ V			0.39	0.50	
		$1.4 \le V_{OUT} < 1.7$ V			0.35	0.44	
		$1.7 \le V_{OUT} < 2.1$ V			0.30	0.39	
		$2.1 \le V_{OUT} < 2.5$ V			0.26	0.34	
		$2.5 \le V_{OUT} < 3.0$ V			0.25	0.30	
		$3.0 \le V_{OUT} < 3.6$ V			0.22	0.29	
Output Current			I_{OUT}	300			mA
Short Current Limit	V_{OUT} = 0 V		I_{SC}		60		mA
Quiescent Current			I_Q		50	75	μA
Standby Current	V_{CE} = 0 V, T_A = 25°C		I_{STB}		0.1	1.0	μA
CE Pin Threshold Voltage	CE Input Voltage “H”		V_{CEH}	1.0			V
	CE Input Voltage “L”		V_{CEL}			0.4	
CE Pull Down Current			I_{CEPD}		0.3		μA
Power Supply Rejection Ratio	$V_{IN} = V_{OUT} + 1$ V or V_{IN} = 3 V, ΔV_{IN} = 0.2 V_{pk-pk}, I_{OUT} = 30 mA, f = 1 kHz		PSRR		65		dB
Output Noise Voltage	f = 10 Hz to 100 kHz, I_{OUT} = 30 mA, V_{OUT} = 1.2 V, V_{IN} = 3.2 V		V_N		65		μV_{rms}
Low Output Nch Tr. On Resistance	V_{IN} = 4 V, V_{CE} = 0 V, D version only		R_{LOW}		50		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

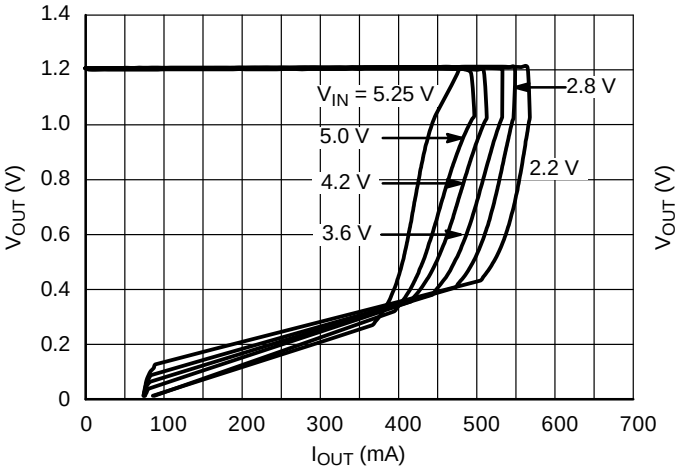


Figure 3. Output Voltage vs. Output Current 1.2 V Version (T_J = 25°C)

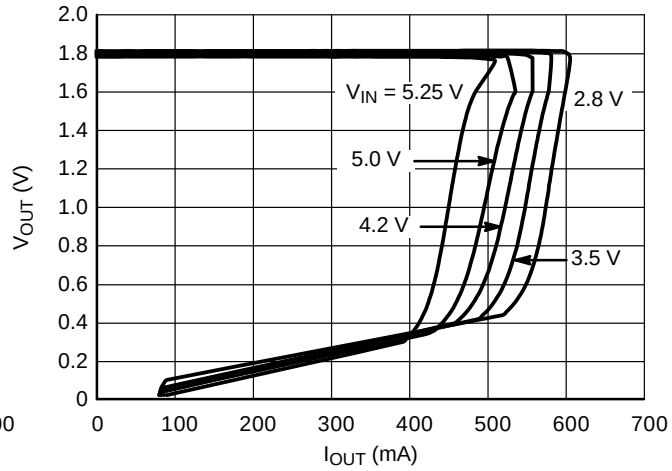


Figure 4. Output Voltage vs. Output Current 1.8 V Version (T_J = 25°C)

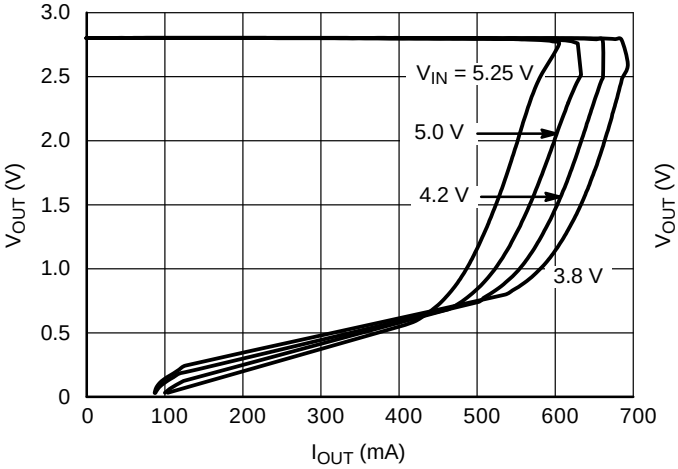


Figure 5. Output Voltage vs. Output Current 2.8 V Version (T_J = 25°C)

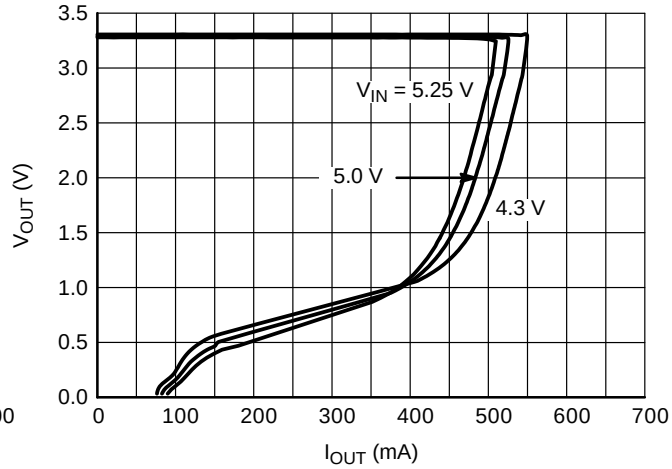


Figure 6. Output Voltage vs. Output Current 3.3 V Version (T_J = 25°C)

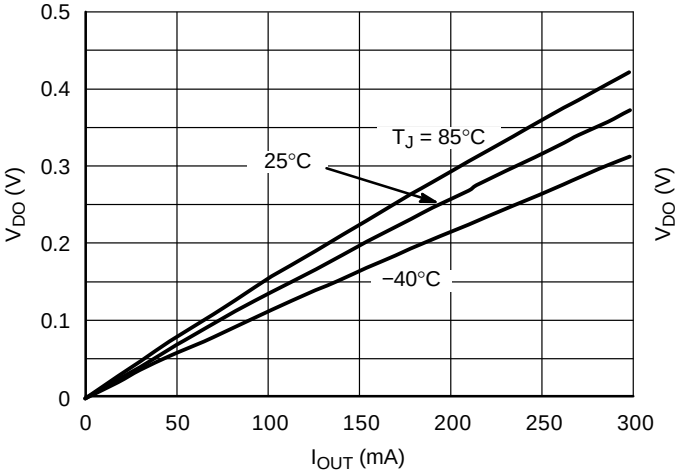


Figure 7. Dropout Voltage vs. Output Current 1.2 V Version

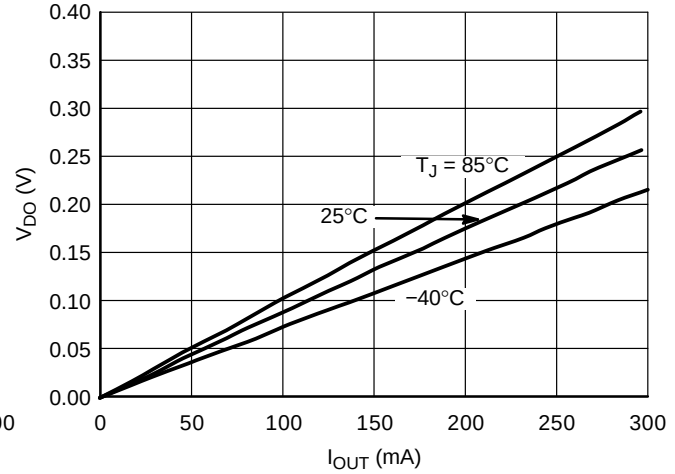


Figure 8. Dropout Voltage vs. Output Current 1.8 V Version

TYPICAL CHARACTERISTICS

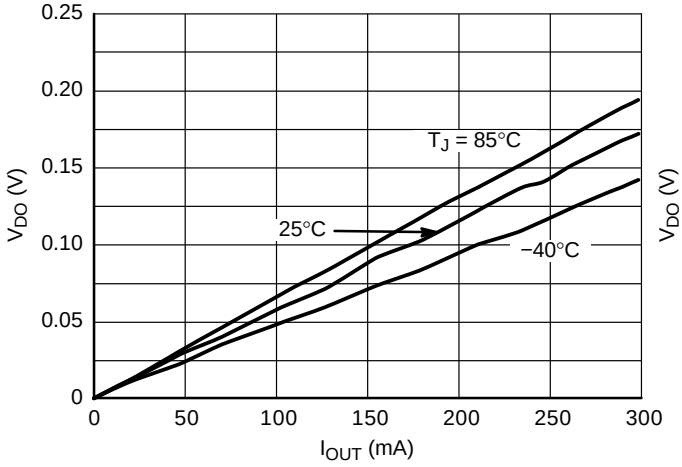


Figure 9. Dropout Voltage vs. Output Current 2.8 V Version

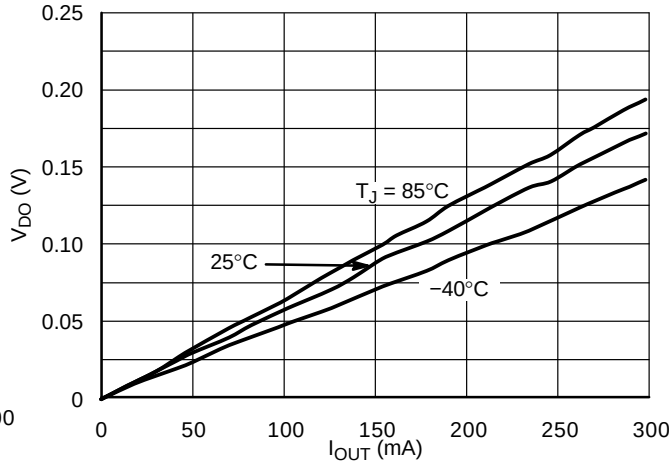


Figure 10. Dropout Voltage vs. Output Current 3.3 V Version

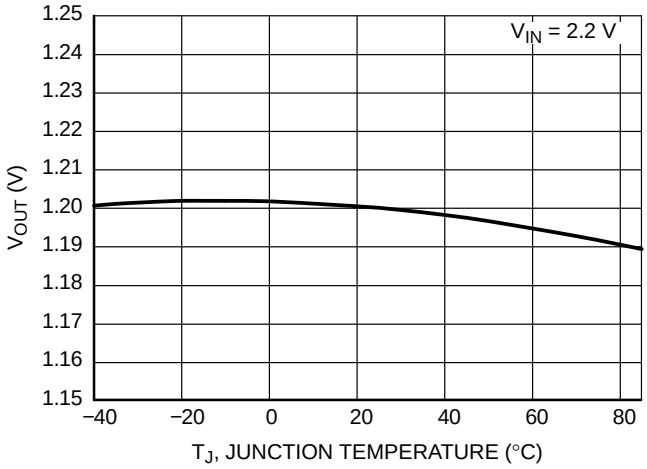


Figure 11. Output Voltage vs. Temperature, 1.2 V Version

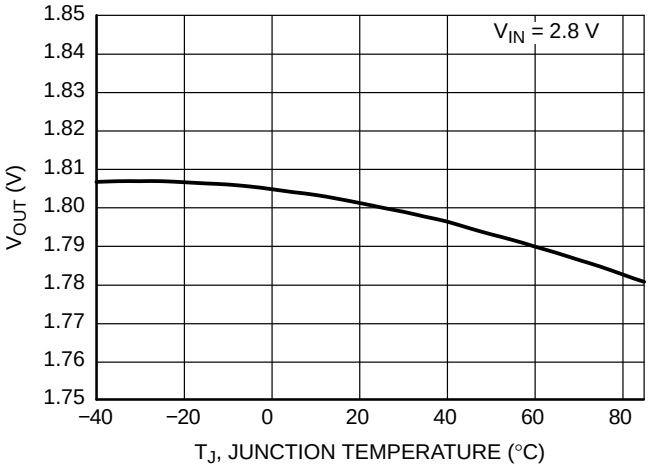


Figure 12. Output Voltage vs. Temperature, 1.8 V Version

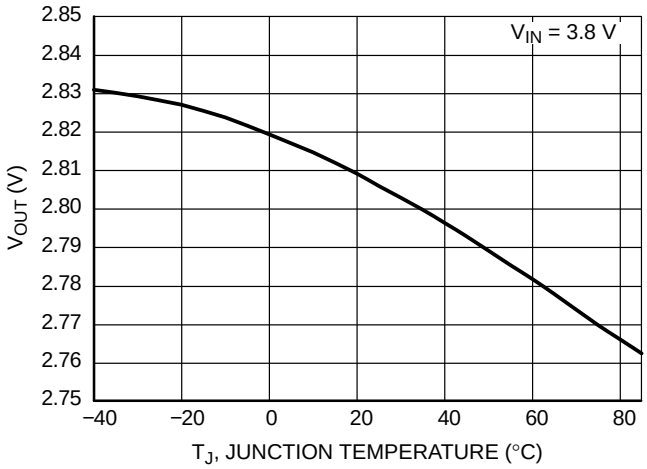


Figure 13. Output Voltage vs. Temperature, 2.8 V Version

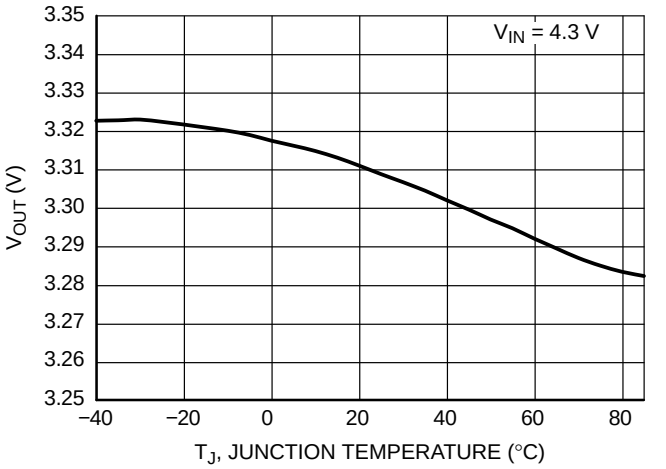


Figure 14. Output Voltage vs. Temperature, 3.3 V Version

TYPICAL CHARACTERISTICS

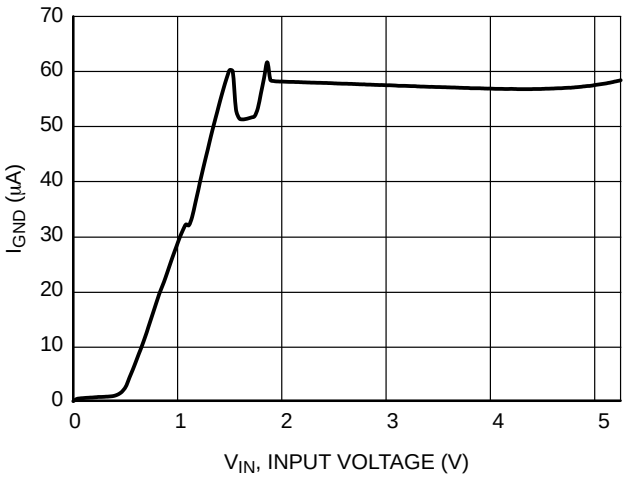


Figure 15. Supply Current vs. Input Voltage, 1.2 V Version

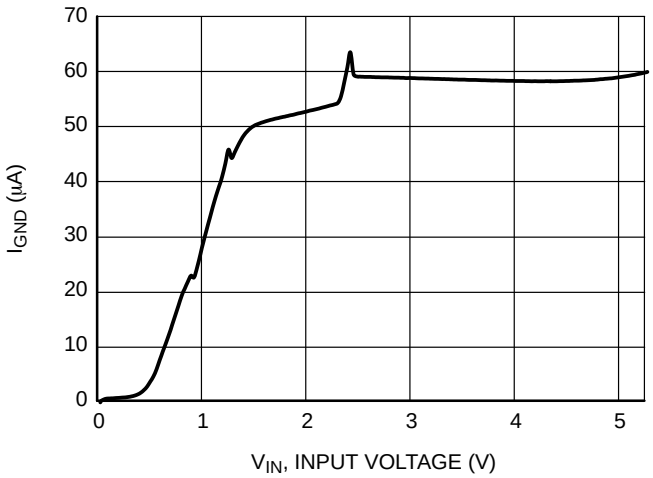


Figure 16. Supply Current vs. Input Voltage, 1.8 V Version

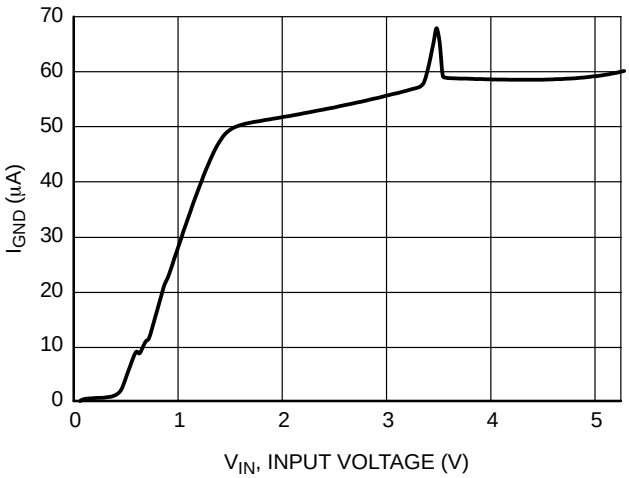


Figure 17. Supply Current vs. Input Voltage, 2.8 V Version

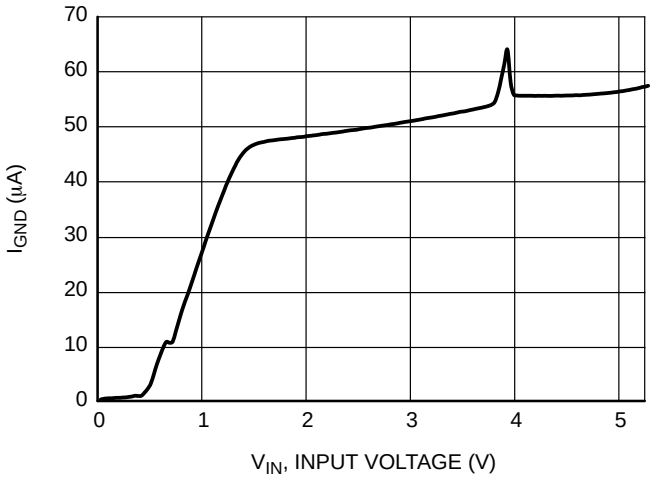


Figure 18. Supply Current vs. Input Voltage, 3.3 V Version

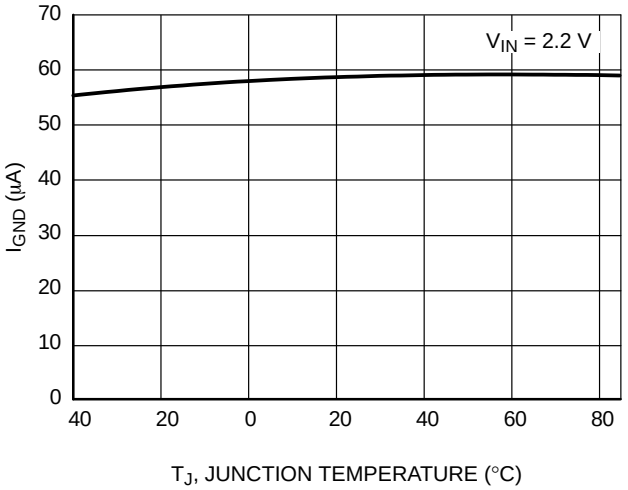


Figure 19. Supply Current vs. Temperature, 1.2 V Version

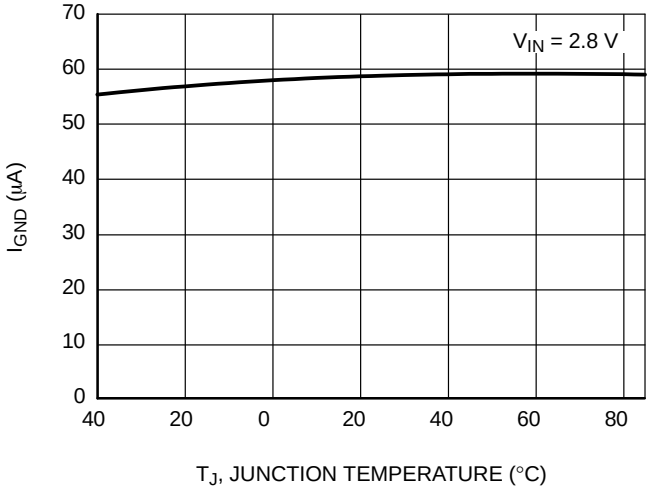


Figure 20. Supply Current vs. Temperature, 1.8 V Version

TYPICAL CHARACTERISTICS

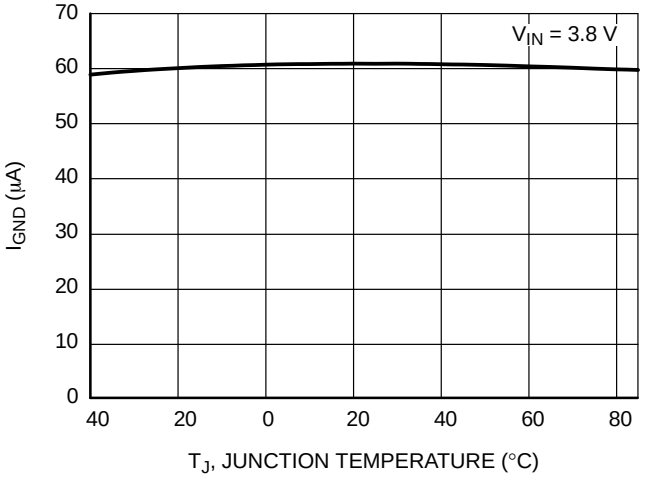


Figure 21. Supply Current vs. Temperature, 2.8 V Version

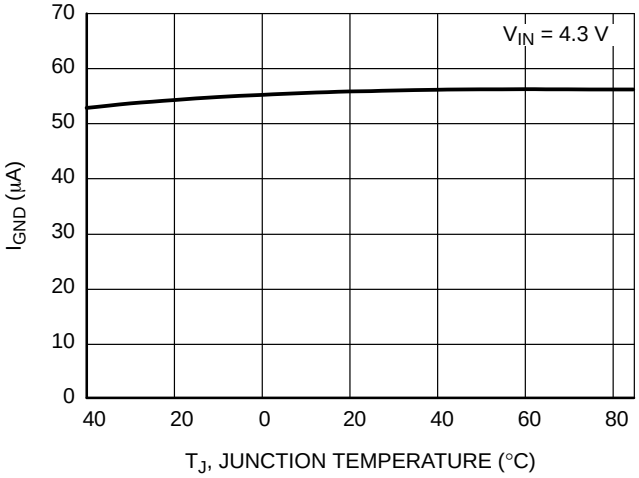


Figure 22. Supply Current vs. Temperature, 3.3 V Version

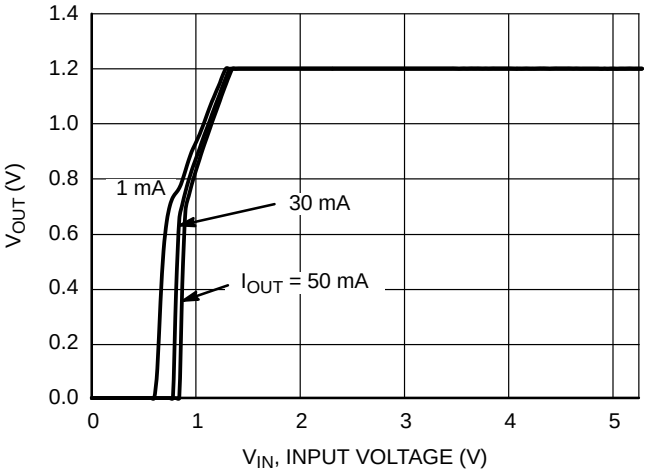


Figure 23. Output Voltage vs. Input Voltage, 1.2 V Version

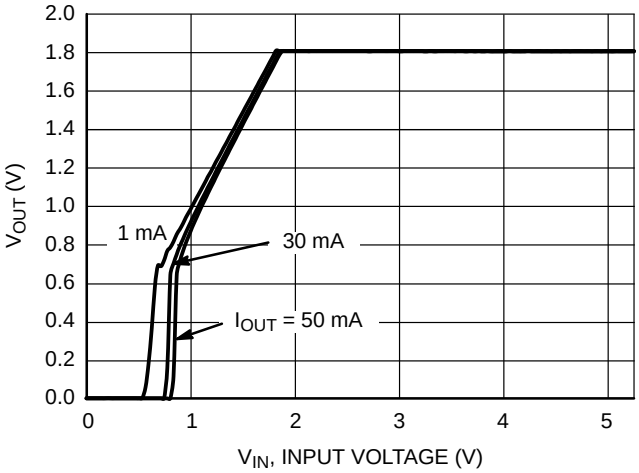


Figure 24. Output Voltage vs. Input Voltage, 1.8 V Version

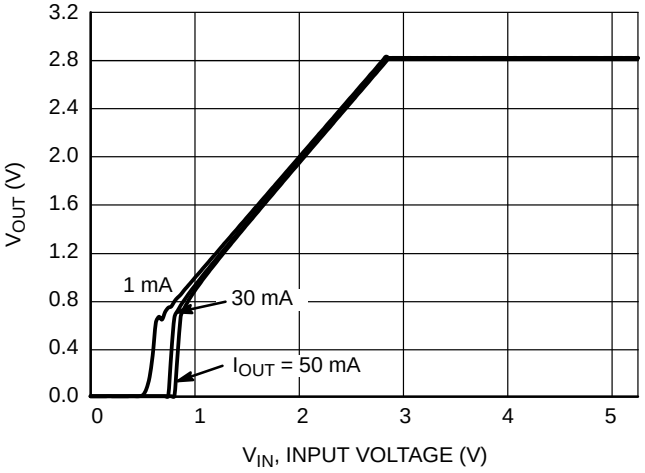


Figure 25. Output Voltage vs. Input Voltage, 2.8 V Version

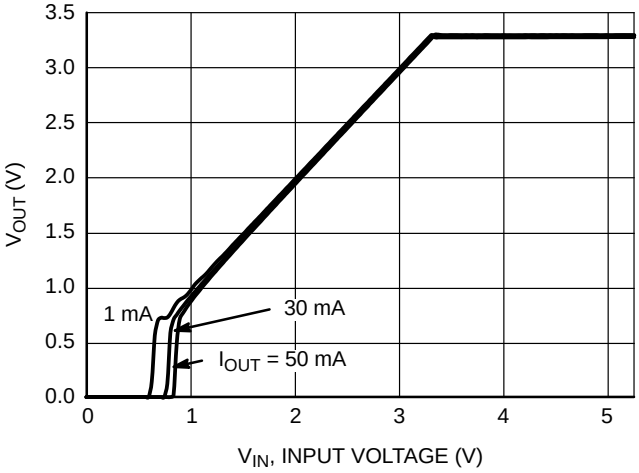


Figure 26. Output Voltage vs. Input Voltage, 3.3 V Version

TYPICAL CHARACTERISTICS

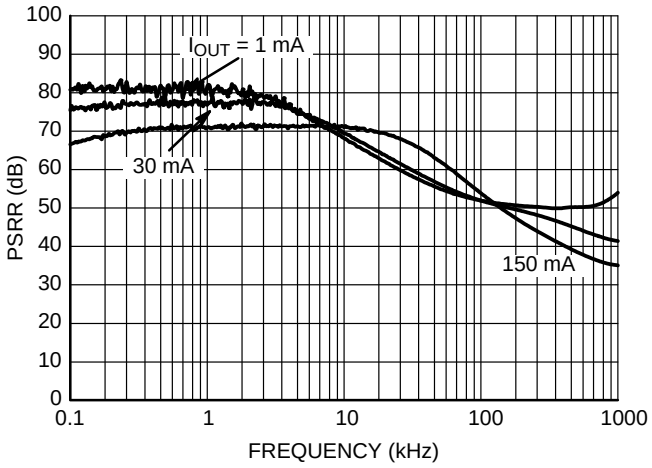


Figure 27. PSRR, 1.2 V Version, V_{IN} = 3.0 V

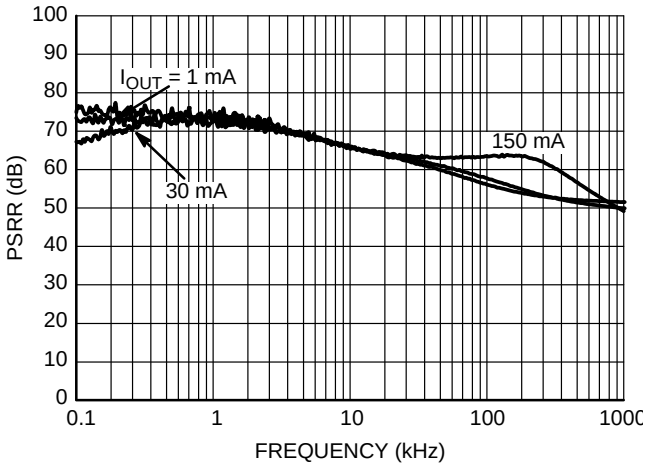


Figure 28. PSRR, 1.8 V Version, V_{IN} = 3.0 V

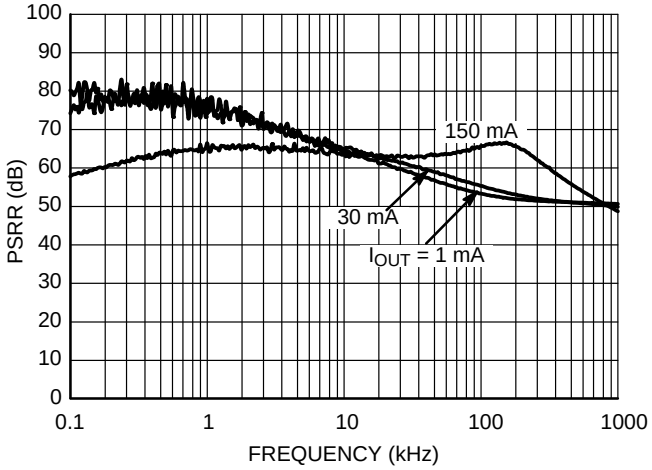


Figure 29. PSRR, 2.8 V Version, V_{IN} = 3.8 V

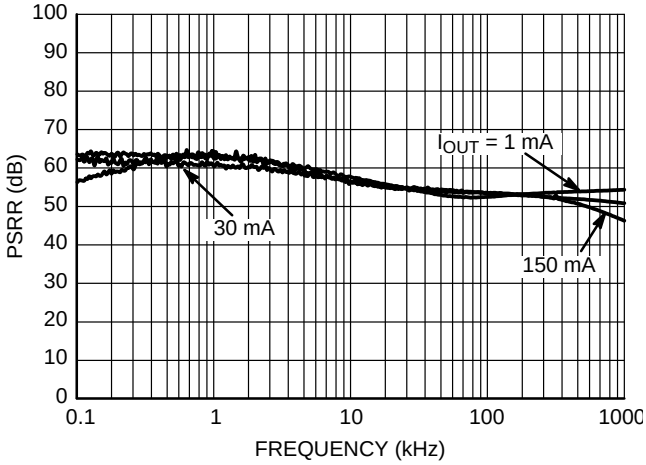


Figure 30. PSRR, 3.3 V Version, V_{IN} = 4.3 V

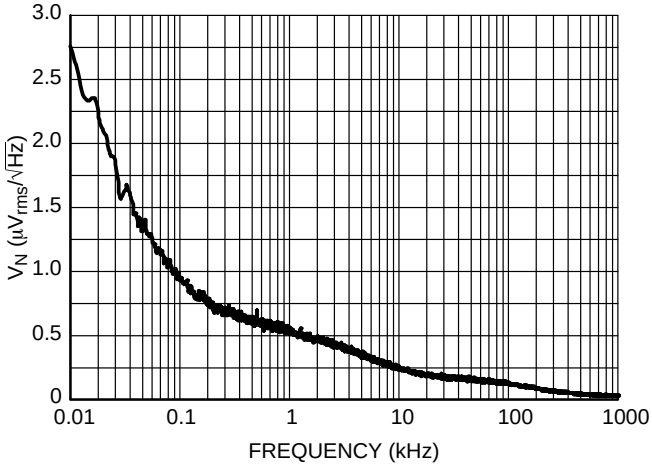


Figure 31. Output Voltage Noise, 1.2 V Version, V_{IN} = 2.2 V

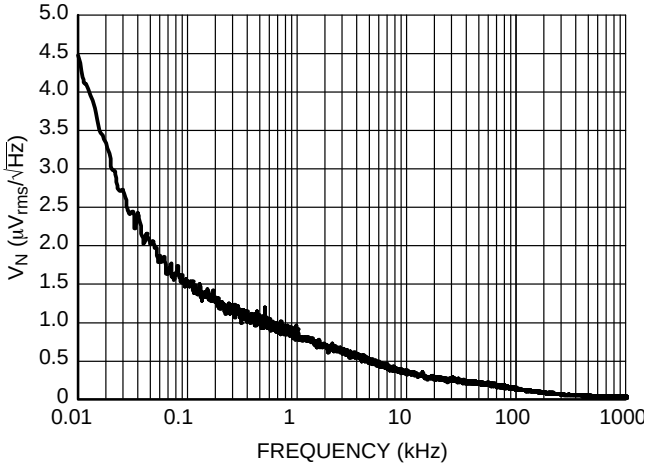


Figure 32. Output Voltage Noise, 1.8 V Version, V_{IN} = 2.8 V

TYPICAL CHARACTERISTICS

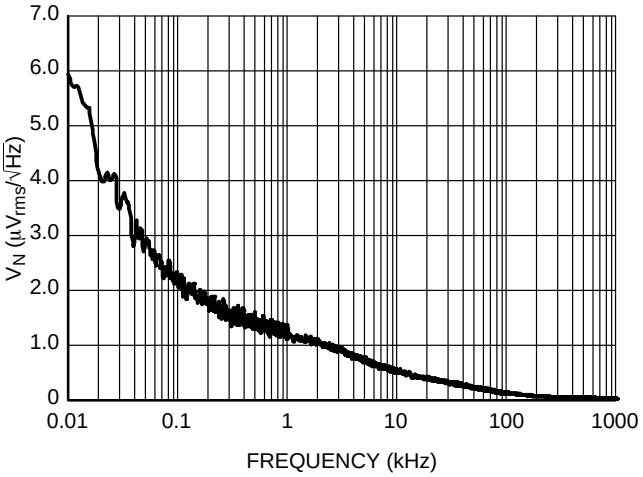


Figure 33. Output Voltage Noise, 2.8 V Version, V_{IN} = 3.8 V

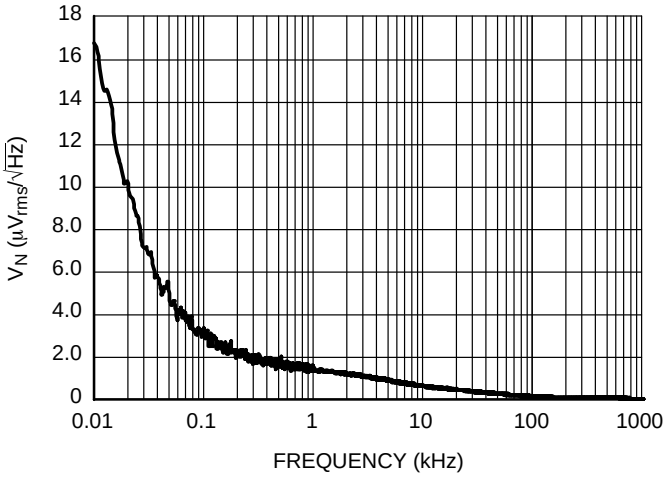


Figure 34. Output Voltage Noise, 3.3 V Version, V_{IN} = 4.3 V

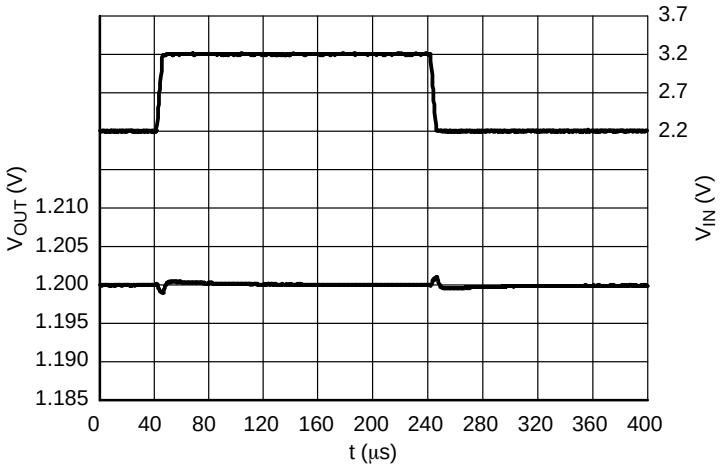


Figure 35. Line Transients, 1.2 V Version, $t_R = t_F$ = 5 μs, I_{OUT} = 30 mA

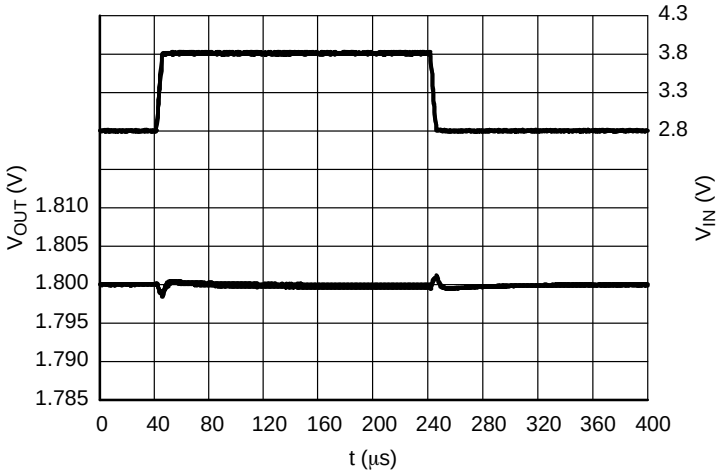


Figure 36. Line Transients, 1.8 V Version, $t_R = t_F$ = 5 μs, I_{OUT} = 30 mA

TYPICAL CHARACTERISTICS

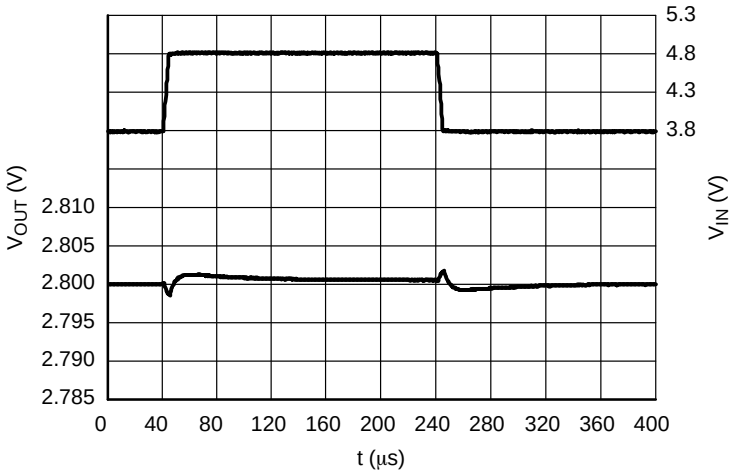


Figure 37. Line Transients, 2.8 V Version, $t_R = t_F = 5$ μs, $I_{OUT} = 30$ mA

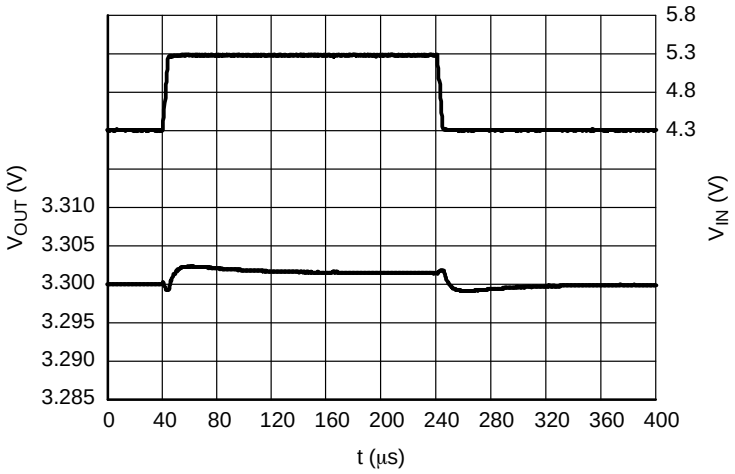


Figure 38. Line Transients, 3.3 V Version, $t_R = t_F = 5$ μs, $I_{OUT} = 30$ mA

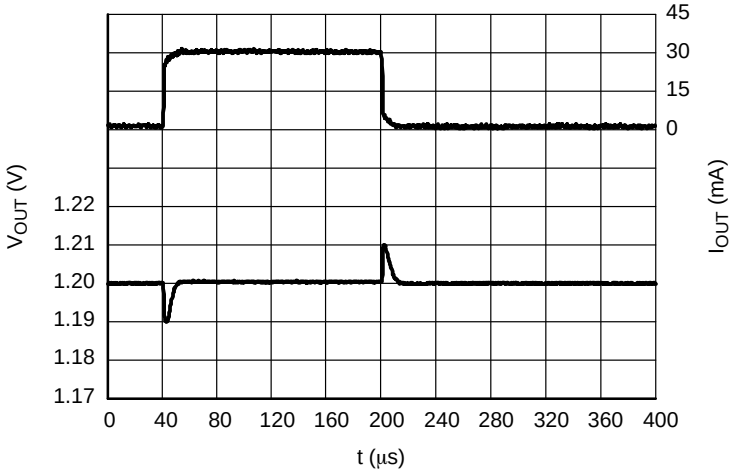


Figure 39. Load Transients, 1.2 V Version, $I_{OUT} = 1 – 30$ mA, $t_R = t_F = 0.5$ μs, $V_{IN} = 1.8$ V

TYPICAL CHARACTERISTICS

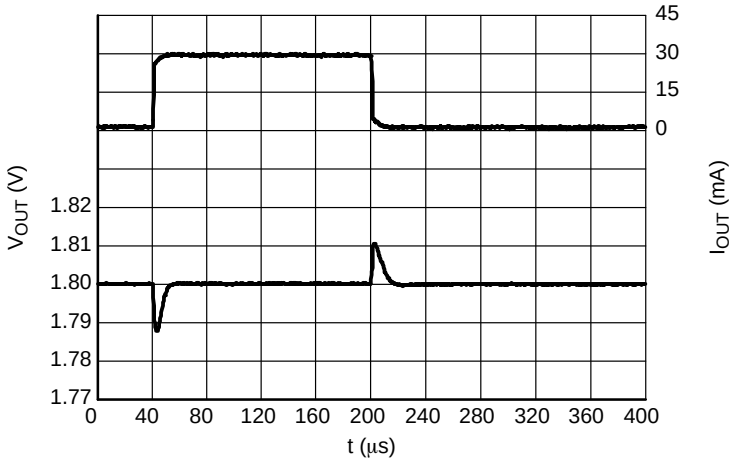


Figure 40. Load Transients, 1.8 V Version, I_{OUT} = 1 – 30 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 2.8 V

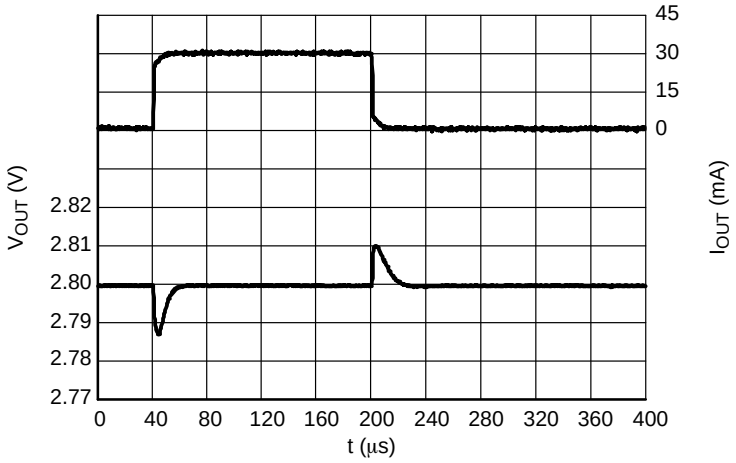


Figure 41. Load Transients, 2.8 V Version, I_{OUT} = 1 – 30 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 3.8 V

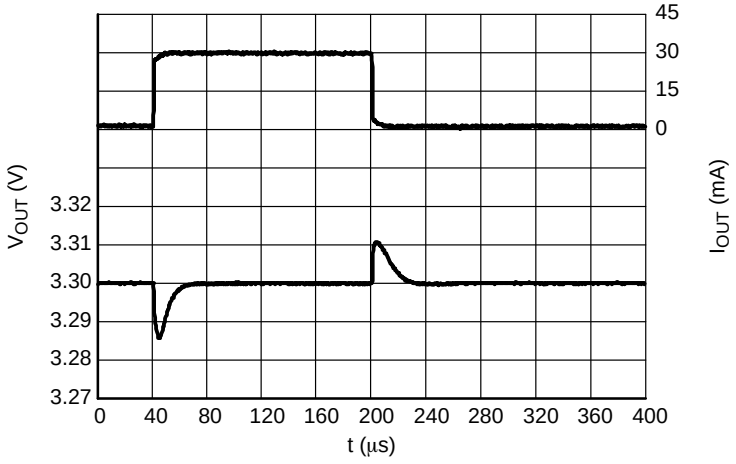


Figure 42. Load Transients, 3.3 V Version, I_{OUT} = 1 – 30 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 4.3 V

TYPICAL CHARACTERISTICS

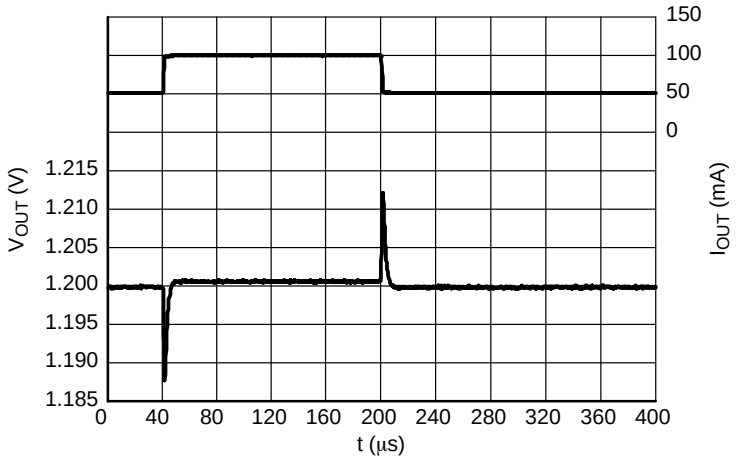


Figure 43. Load Transients, 1.2 V Version, I_{OUT} = 50 – 100 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 1.8 V

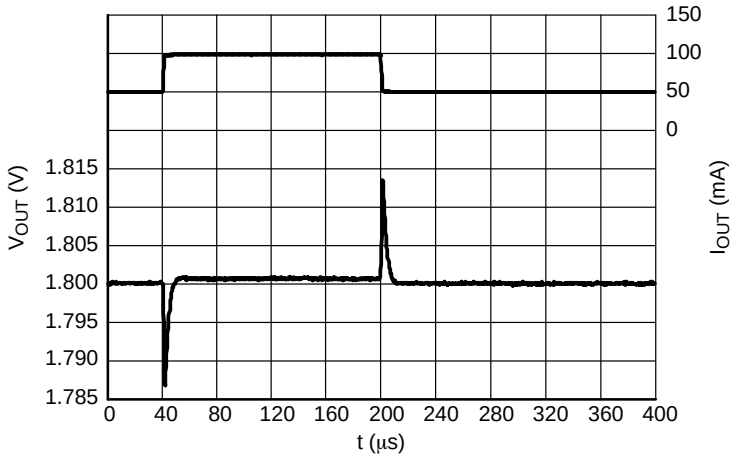


Figure 44. Load Transients, 1.8 V Version, I_{OUT} = 50 – 100 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 2.8 V

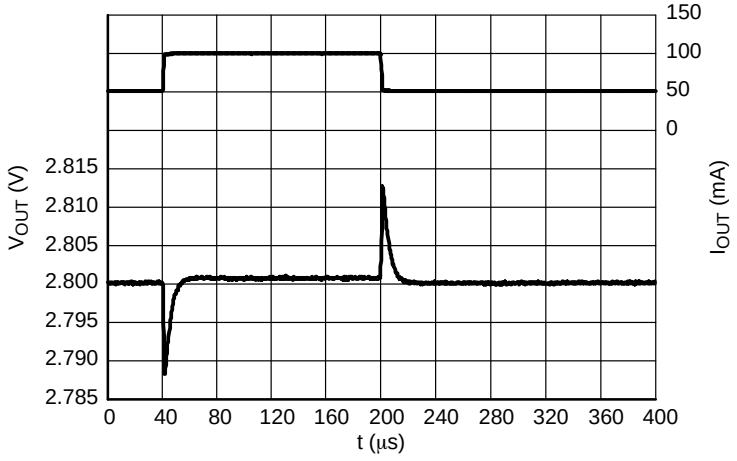


Figure 45. Load Transients, 2.8 V Version, I_{OUT} = 50 – 100 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 3.8 V

TYPICAL CHARACTERISTICS

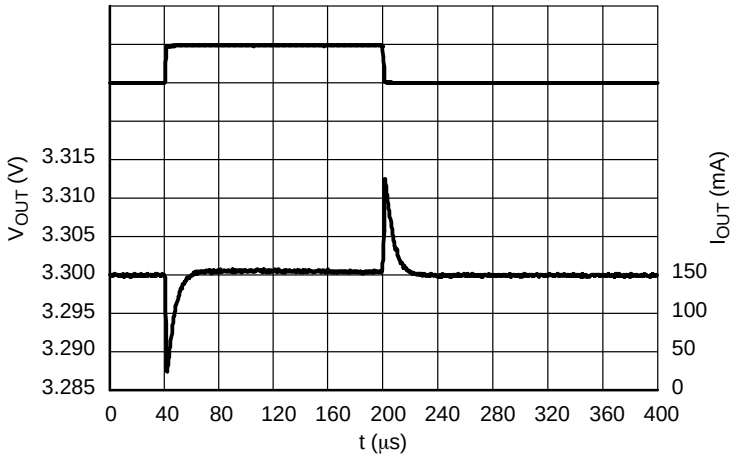


Figure 46. Load Transients, 3.3 V Version, I_{OUT} = 50 – 100 mA, t_R = t_F = 0.5 μs, V_{IN} = 4.3 V

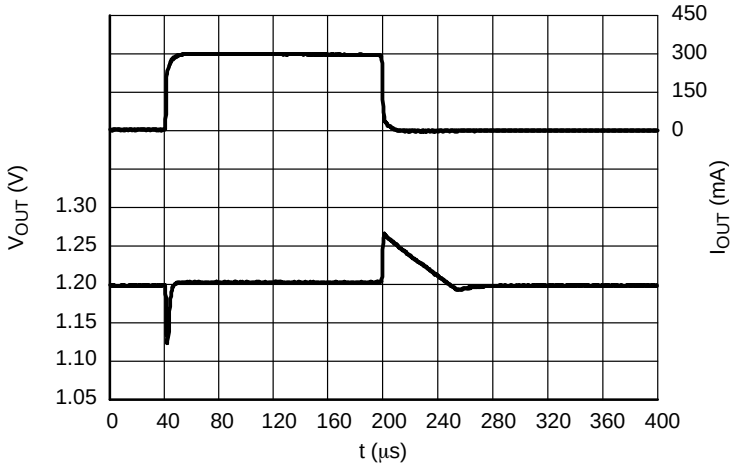


Figure 47. Load Transients, 1.2 V Version, I_{OUT} = 1 – 300 mA, t_R = t_F = 0.5 μs, V_{IN} = 2.2 V

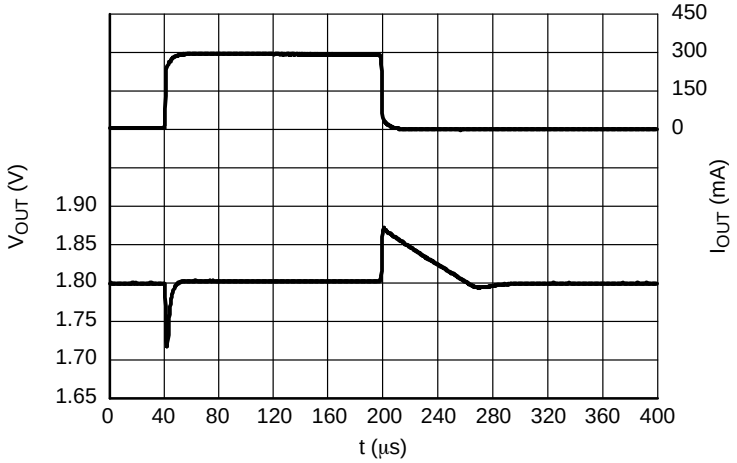


Figure 48. Load Transients, 1.8 V Version, I_{OUT} = 1 – 300 mA, t_R = t_F = 0.5 μs, V_{IN} = 2.8 V

TYPICAL CHARACTERISTICS

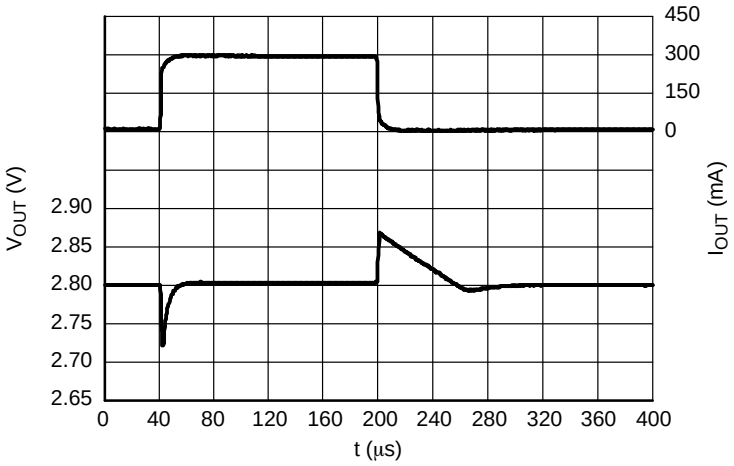


Figure 49. Load Transients, 2.8 V Version, I_{OUT} = 1 − 300 mA, t_R = t_F = 0.5 μs, V_{IN} = 3.8 V

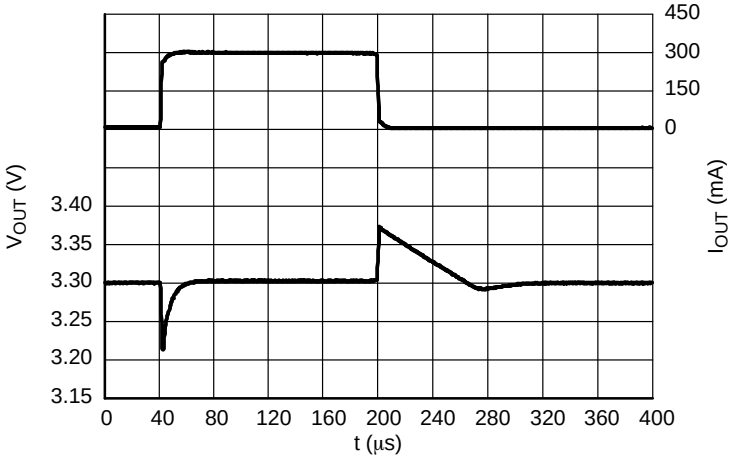


Figure 50. Load Transients, 3.3 V Version, I_{OUT} = 1 − 300 mA, t_R = t_F = 0.5 μs, V_{IN} = 4.3 V

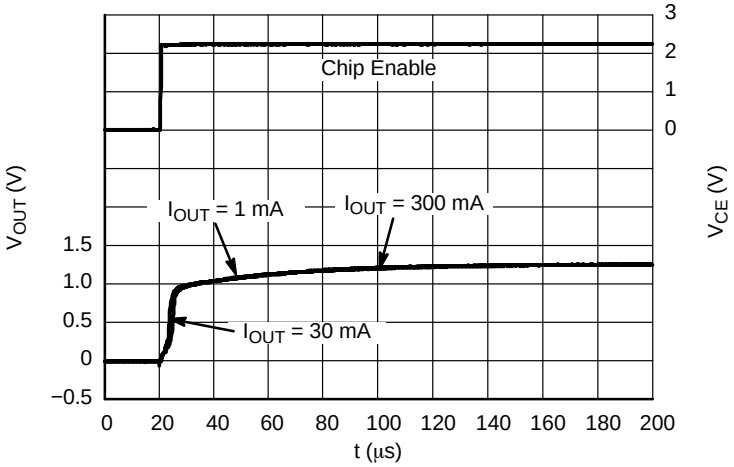


Figure 51. Start−up, 1.2 V Version, V_{IN} = 2.2 V

TYPICAL CHARACTERISTICS

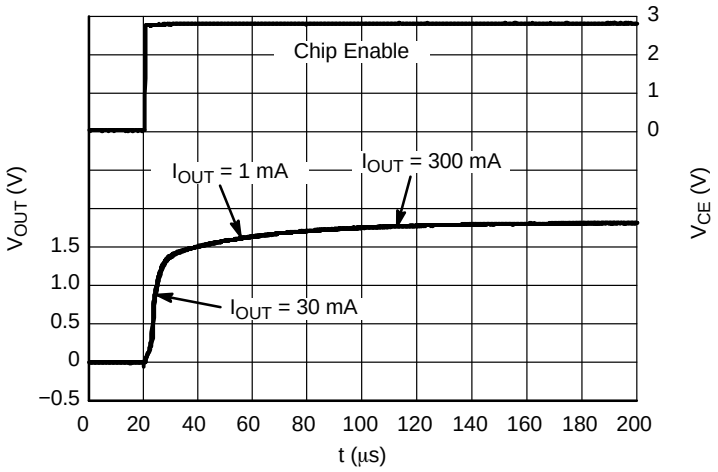


Figure 52. Start−up, 1.8 V Version, V_{IN} = 2.8 V

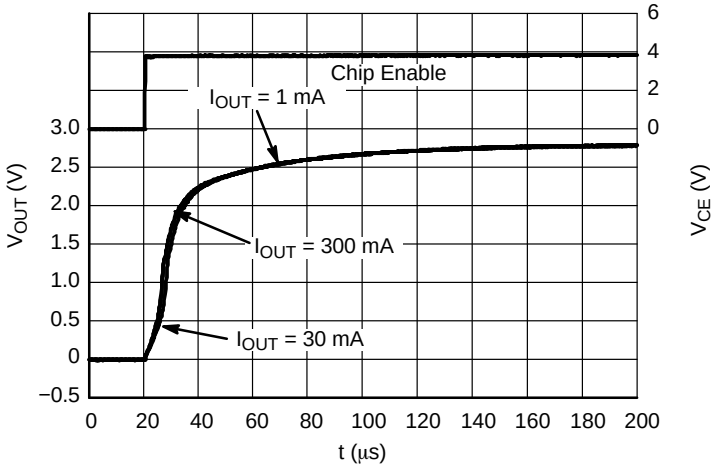


Figure 53. Start−up, 2.8 V Version, V_{IN} = 3.8 V

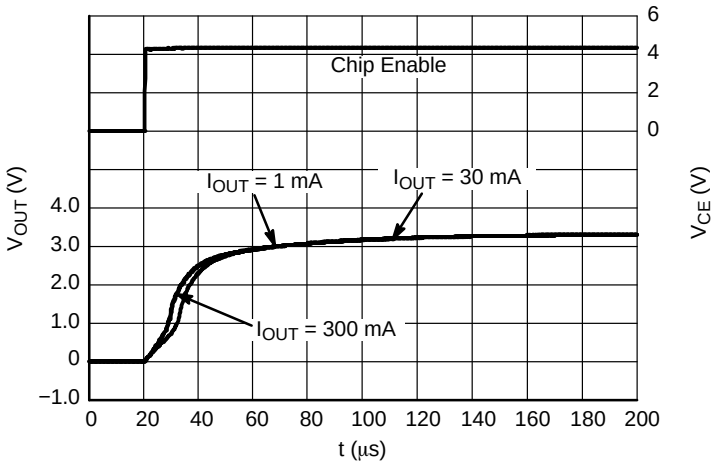


Figure 54. Start−up, 3.3 V Version, V_{IN} = 4.3 V

TYPICAL CHARACTERISTICS

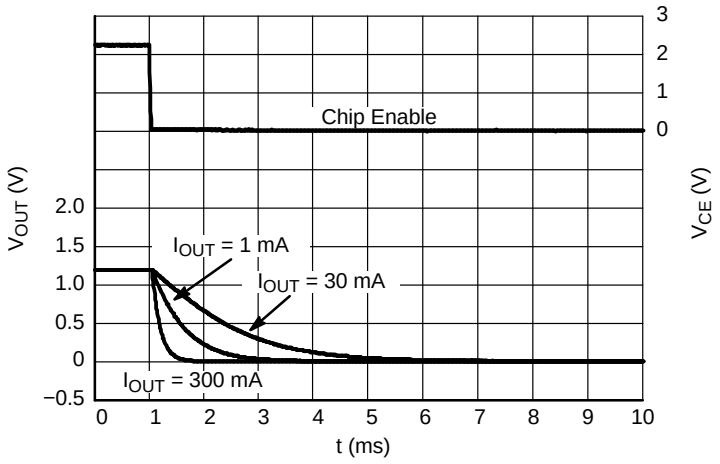


Figure 55. Shutdown, 1.2 V Version B, V_{IN} = 2.2 V

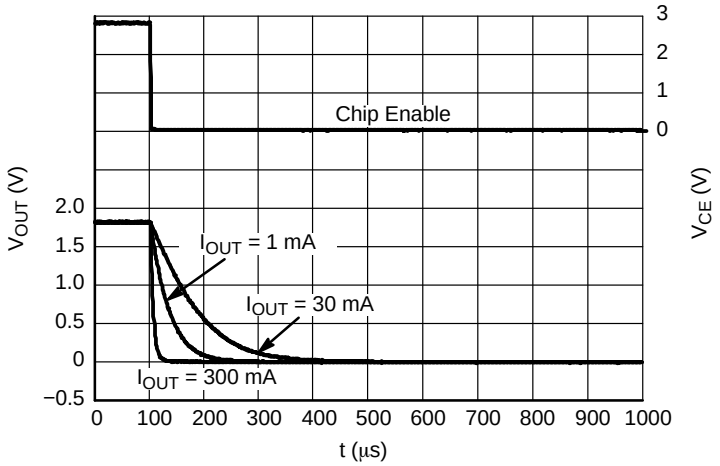


Figure 56. Shutdown, 1.8 V Version D, V_{IN} = 2.8 V

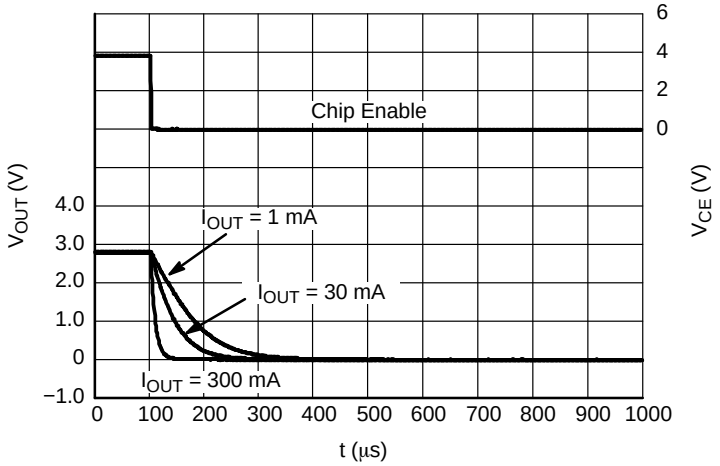


Figure 57. Shutdown, 2.8 V Version D, V_{IN} = 3.8 V

TYPICAL CHARACTERISTICS

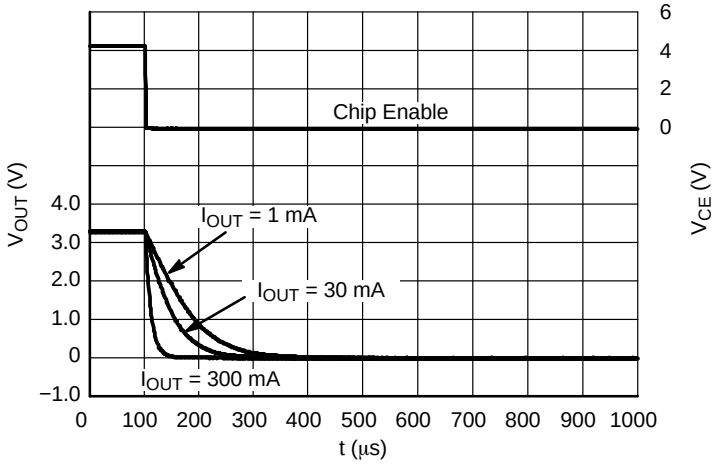


Figure 58. Shutdown, 3.3 V Version D, V_{IN} = 4.3 V

APPLICATION INFORMATION

A typical application circuit for NCP4683 series is shown in Figure 59.

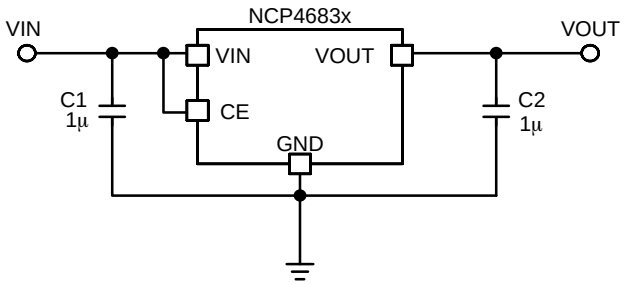


Figure 59. Typical Application Schematic

Input Decoupling Capacitor (C1)

A 1 μF ceramic input decoupling capacitor should be connected as close as possible to the input and ground pin of the NCP4683. Higher values and lower ESR improves line transient response.

Output Decoupling Capacitor (C2)

A 1 μF ceramic output decoupling capacitor is enough to achieve stable operation of the IC. If a tantalum capacitor is used, and its ESR is high, loop oscillation may result. The capacitors should be connected as close as possible to the output and ground pins. Larger values and lower ESR improves dynamic parameters.

Enable Operation

The enable pin CE may be used for turning the regulator on and off. The IC is switched on when a high level voltage is applied to the CE pin. The enable pin has an internal pull down current source. If the enable function is not needed connect CE pin to VIN.

Current Limit

This regulator includes fold−back type current limit circuit. This type of protection doesn't limit current up to current capability in normal operation, but when over current occurs, output voltage and current decrease until over current condition ends. Typical characteristics of this protection type can be observed in the Output Voltage vs. Output Current graphs shown in the typical characteristics chapter of this datasheet.

Output Discharger

The D version includes a transistor between VOUT and GND that is used for faster discharging of the output capacitor. This function is activated when the IC goes into disable mode.

Thermal

As power across the IC increase, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and also the ambient temperature affect the rate of temperature increase for the part. When the device has good thermal conductivity through the PCB the junction temperature will be relatively low in high power dissipation applications.

PCB layout

Make the VIN and GND line as large as practical. If their impedance is high, noise pickup or unstable operation may result. Connect capacitors C1 and C2 as close as possible to the IC, and make wiring as short as possible.

ORDERING INFORMATION

Device	Nominal Output Voltage	Description	Marking	Package	Shipping†
NCP4683DMU09TCG	0.9	Auto discharge	Q1	UDFN4 (Pb−Free)	10000 / Tape & Reel
NCP4683DMU12TCG	1.20	Auto discharge	Q4		
NCP4683DMU18TCG	1.80	Auto discharge	R0		
NCP4683DMU185TCG	1.85	Auto discharge	T0		
NCP4683DMU285TCG	2.85	Auto discharge	T1		
NCP4683DMU31TCG	3.1	Auto discharge	S3		
NCP4683HMU12TCG	1.20	Standard	L4		
NCP4683HMU185TCG	1.85	Standard	P0		
NCP4683DSQ18T1G	1.80	Auto discharge	AH18	SC−70 (Pb−Free)	3000 / Tape & Reel
NCP4683DSQ28T1G	2.80	Auto discharge	AH28		
NCP4683DSQ33T1G	3.30	Auto discharge	AH33		

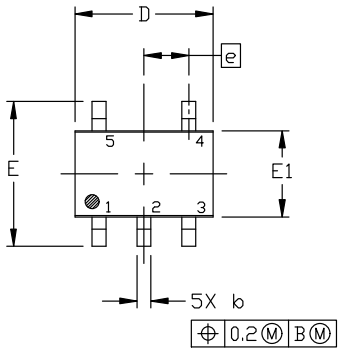
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*Marking codes for XDFN0808 packages are unified.
**To order other package and voltage variants, please contact your ON Semiconductor sales representative.

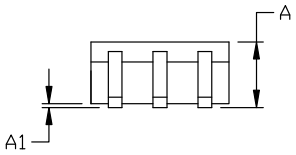
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

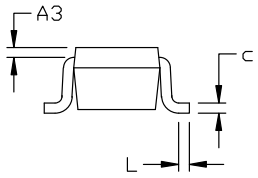
SCALE 2:1

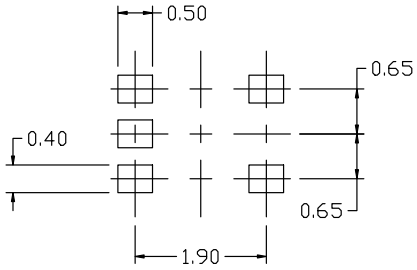
SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE M

DATE 11 APR 2023









RECOMMENDED
MOUNTING FOOTPRINT

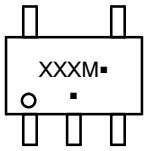
* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

DOCUMENT NUMBER:	98ASB42984B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SC−88A (SC−70−5/SOT−353)	PAGE 1 OF 1

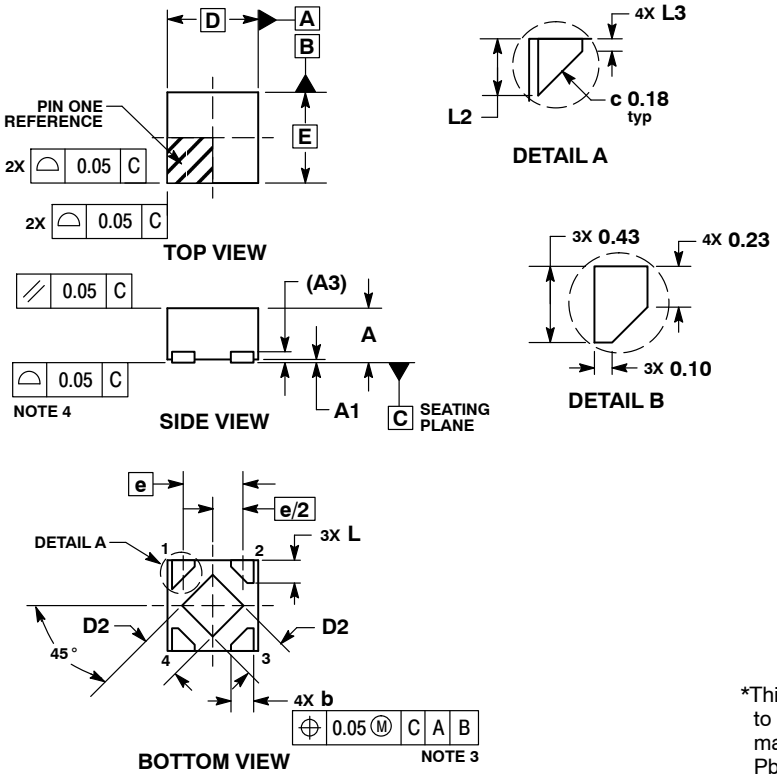
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

UDFN4 1.0x1.0, 0.65P
CASE 517BR−01
ISSUE O

DATE 27 OCT 2010

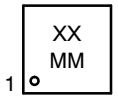
SCALE 4:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.60
A1	0.00	0.05
A3	0.10 REF	
b	0.20	0.30
D	1.00 BSC	
D2	0.43	0.53
E	1.00 BSC	
e	0.65 BSC	
L	0.20	0.30
L2	0.27	0.37
L3	0.02	0.12

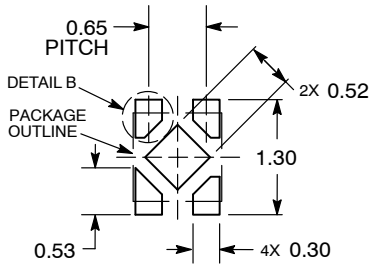
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
MM = Date Code

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON53254E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**UDFN4, 1.0X1.0, 0.65P**	**PAGE 1 OF 1**

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