ESD7484

ESD Protection Diode

4−Line, Ultra Large Bandwidth

ON Semiconductor®

www.onsemi.com

Functional Description

The ESD7484 chip is a monolithic, application specific discrete device dedicated to ESD protection of the HDMI connection. It also offers the same high level of protection for IEEE 1394a and IEEE 1394b/c, USB2.0, Ethernet links, and video lines.

Its ultra high cutoff frequency (5.3 GHz) secures a high level of signal integrity. The device topology provides this integrity without compromising the complete protection of ICs against the most stringent ESD strikes.

Features

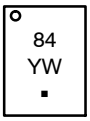
- Wideband Performance
- Flow−Through Layout
- Low Profile with Small Footprint: 1.6 mm x 1.1 mm Package
- 0.4 mm Pitch WLCSP Package
- IEC61000−4−2 Level 4 (At External Pins)
  - ♦ ± 15 kV (Air Discharge)
  - ♦ ± 15 kV (Contact Discharge)
- These Devices are Pb−Free, Halogen Free and are RoHS II Compliant

Applications

- Mobile Phones and Communications Systems
- HDMI Ports at 1.65 Gb/s and up to 3.2 Gb/s
- Video Out Protection

WLCSP10
CASE 567DE

MARKING DIAGRAM



84	= Specific Device Code
Y	= Year
W	= Work Week
▪	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

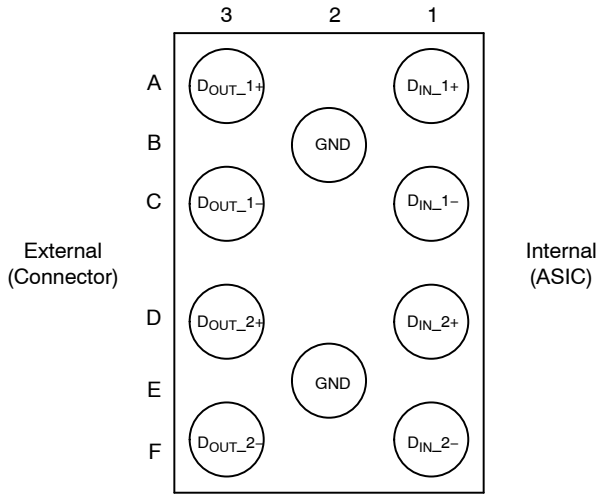


Figure 1. Pin Configuration (Bump View)

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{PP}	ESD IEC61000−4−2, level 4 − air discharge (external pins) ESD IEC61000−4−2, level 4 − contact discharge (external pins)	±15 ±15	kV
P_{PP}	Peak Pulse Power Dissipation (8/20 μs)	70	W
T_J	Maximum Junction Temperature	125	°C
T_{stg}	Storage Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (Note 1)

Symbol	Test Condition	Min	Typ	Max	Unit
V_{BR}	Breakdown Voltage (Ir = 1 mA)	6		9	V
I_{RM}	Leakage Current @ V_{rm} (V_{rm} = 3 V per line)		3	100	nA
C_{line}	V_{line} = 0 V, V_{osc} = 30 mV, F = 1 MHz, Capacitor between I/O and GND		1.6	1.75	pF
	V_{line} = 0 V, V_{osc} = 30 mV, F = 1 MHz, Capacitor between I/O		0.8		
$\Delta C_{I/O-I/O}$	V_{line} = 0 V, V_{osc} = 30 mV, F = 1 MHz, Capacitance Variation between I/O		0.006		pF

1. All parameters specified at T_A = 25°C unless otherwise noted.
2. Standard IEC 61000−4−2 with $C_{Discharge}$ = 150 pF, $R_{Discharge}$ = 330 Ω.

TYPICAL CHARACTERISTICS

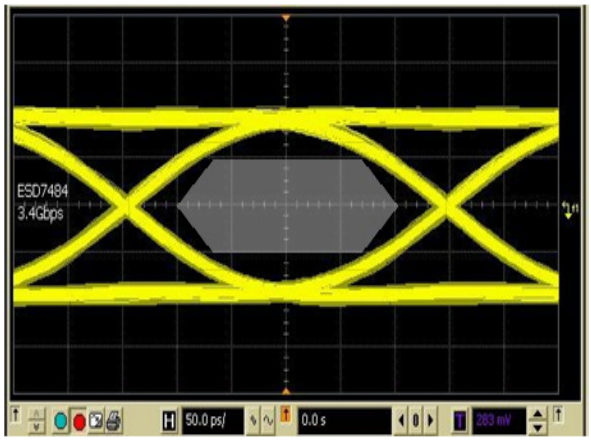


Figure 2. HDMI1.4 Test Conditions
3.4 Gb/s Datarate;
Clears HDMI Source Mask

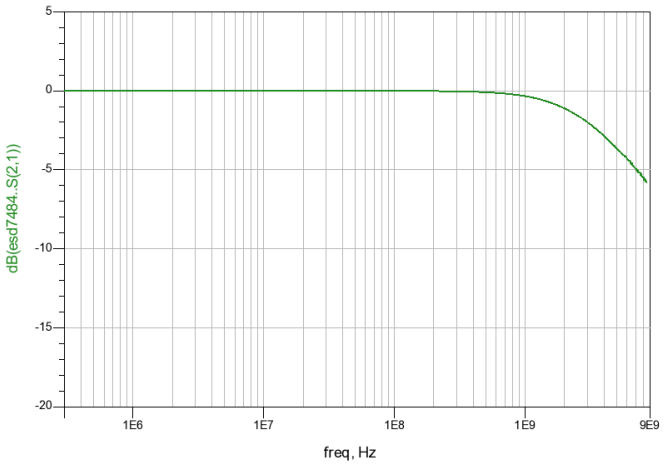


Figure 3. S21 Plot

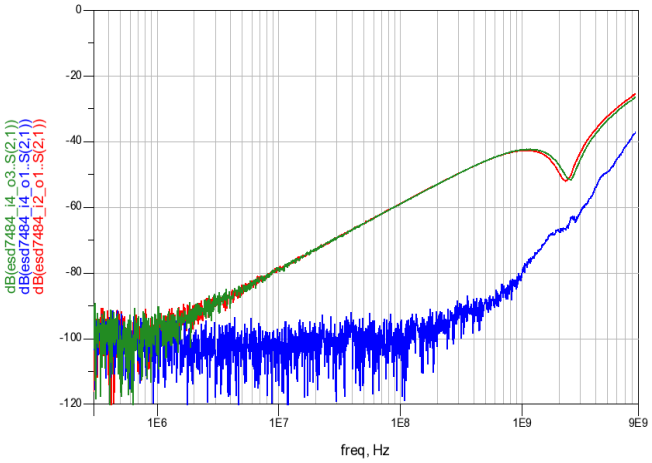


Figure 4. Crosstalk Measurements

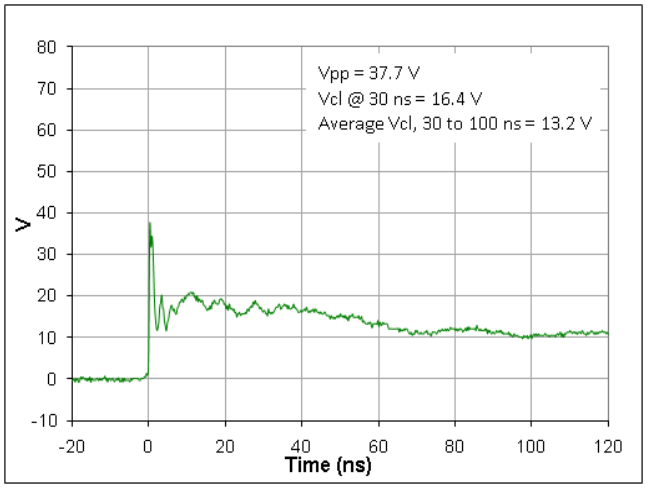


Figure 5. ESD Clamping Voltage Screenshot
Positive 8 kV Contact per IEC61000−4−2

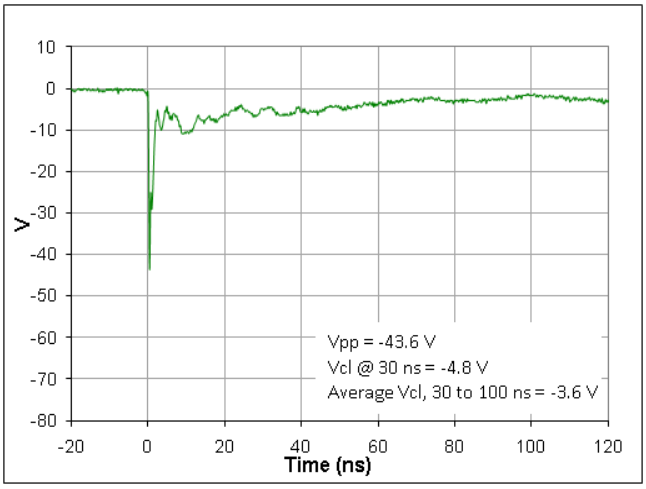


Figure 6. ESD Clamping Voltage Screenshot
Negative 8 kV Contact per IEC61000−4−2

IEC61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

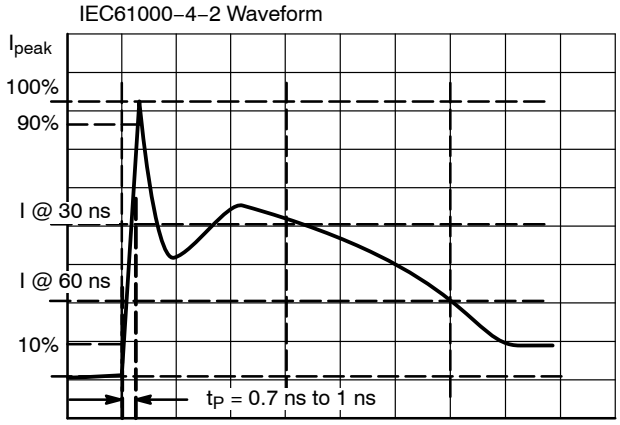


Figure 7. IEC61000−4−2 Spec

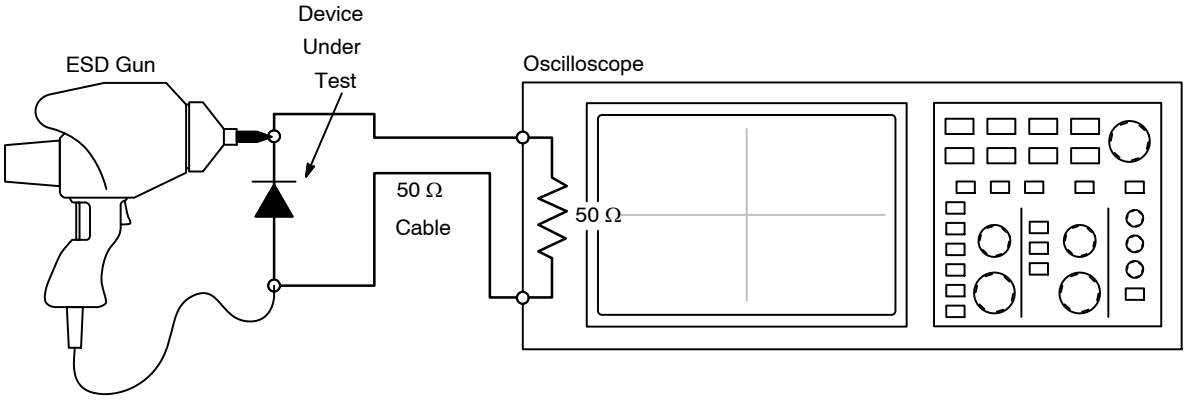


Figure 8. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

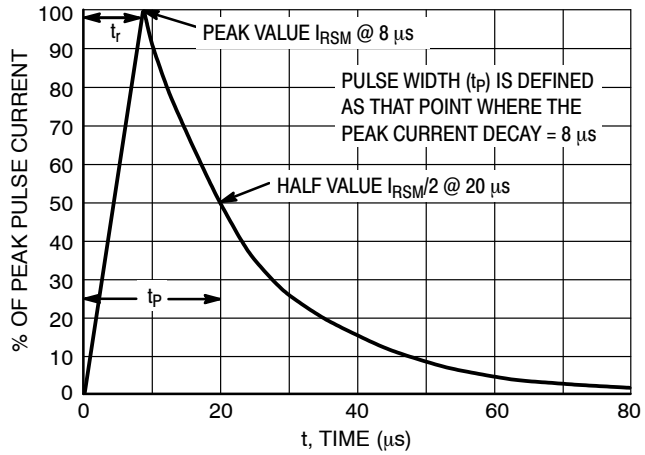


Figure 9. 8 x 20 μs Pulse Waveform

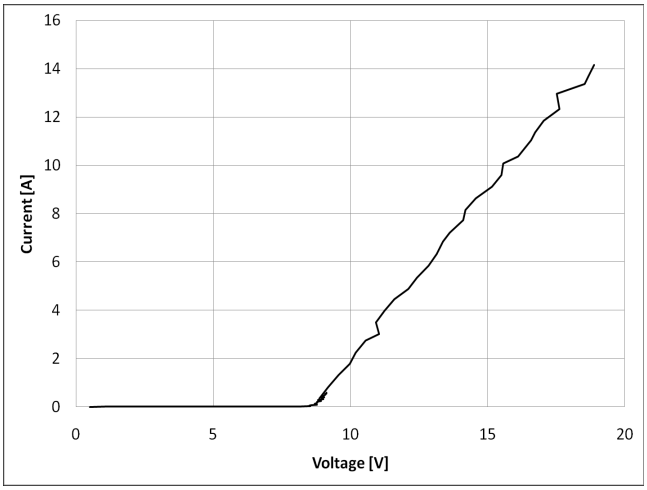


Figure 10. Positive TLP I−V Curve

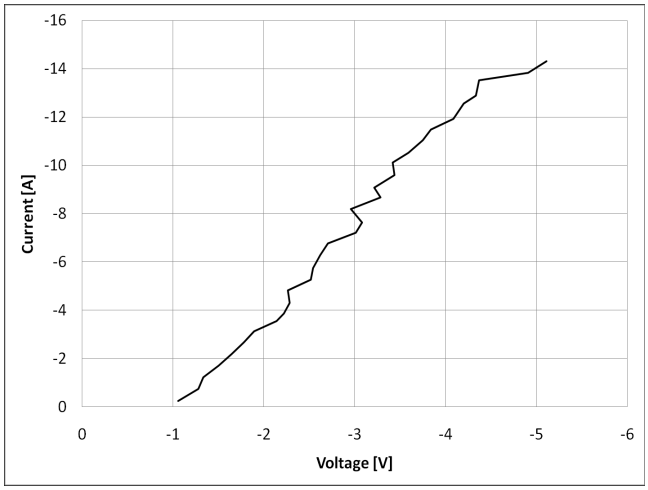


Figure 11. Negative TLP I−V Curve

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 12. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 13 where an 8 kV IEC61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. A typical TLP I−V curve for the ESD7383 is shown in Figures 10 and 11.

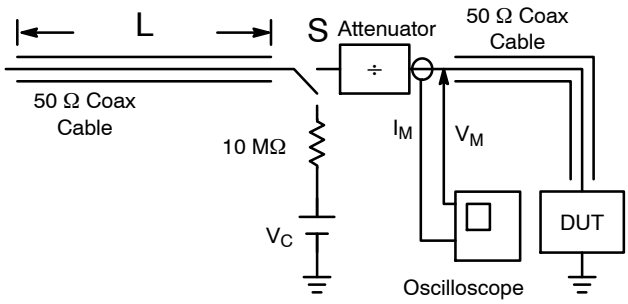


Figure 12. Simplified Schematic of a Typical TLP System

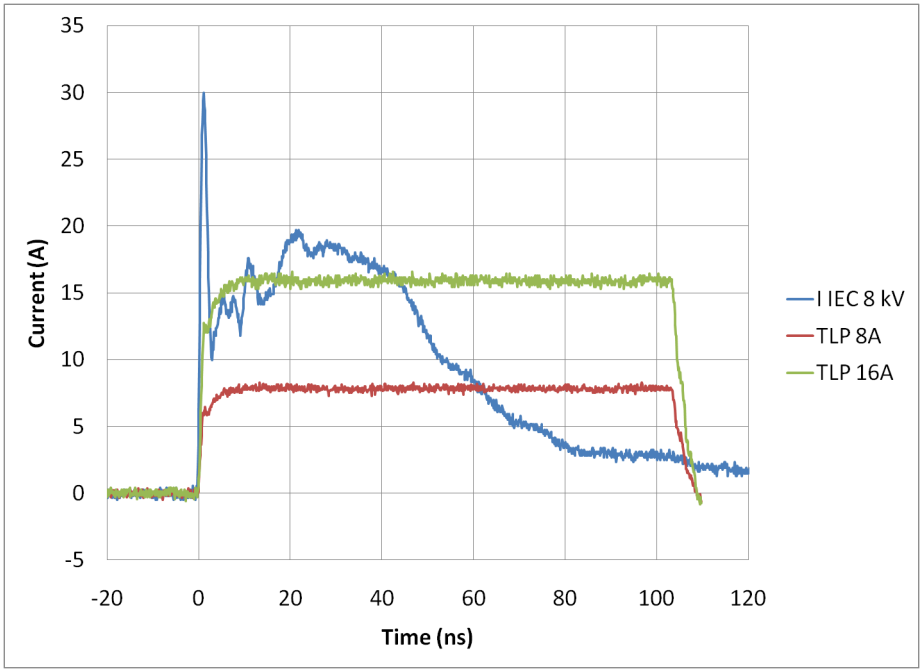


Figure 13. Comparison Between 8 kV IEC61000−4−2 and 8 A and 16 A TLP Waveforms

TYPICAL APPLICATION SCHEMATIC

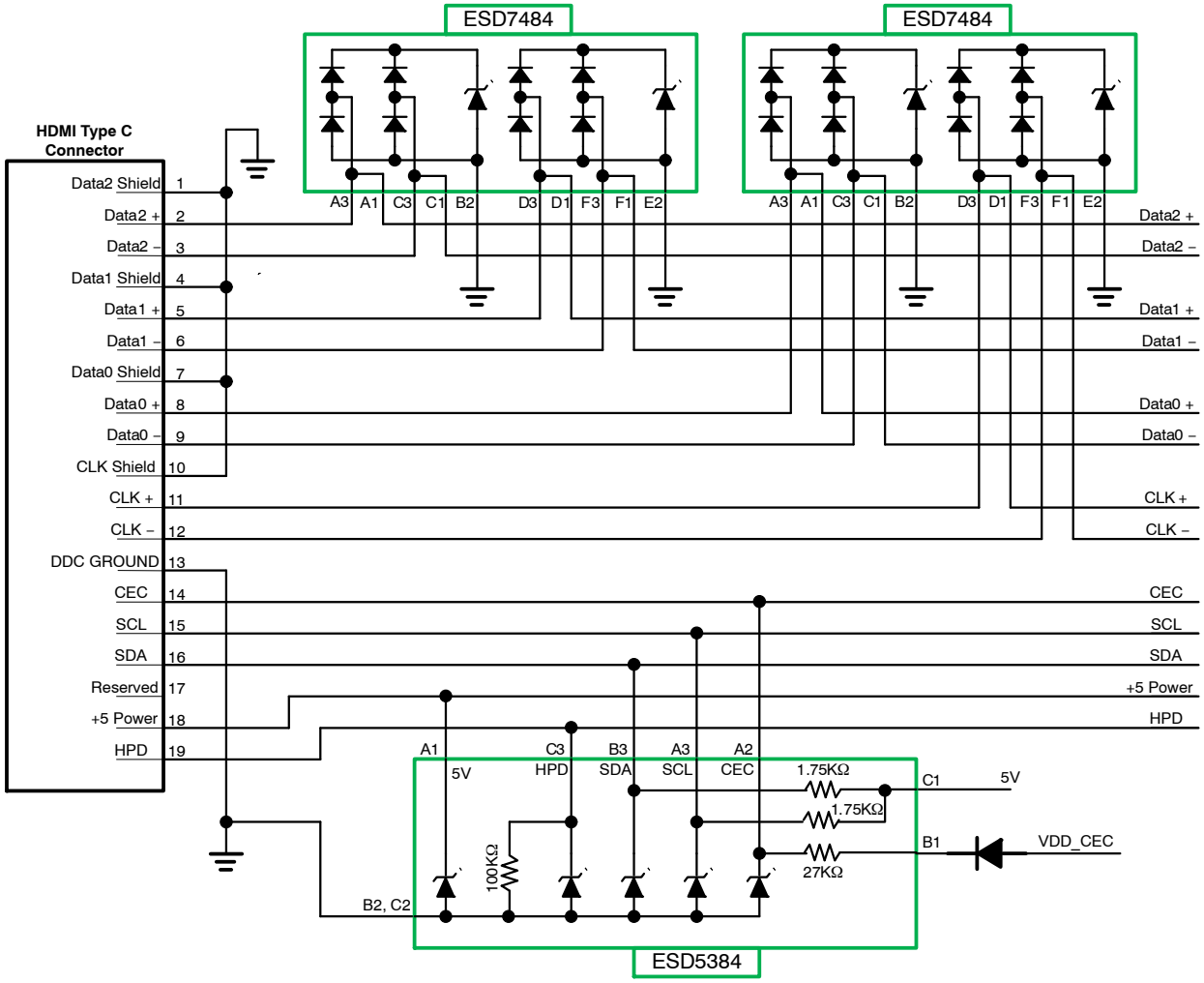


Figure 14. Typical Application Schematic

ORDERING INFORMATION

Part Number	Chip Size (mm)	Pocket Size (mm) B_0 X A_0 X K_0	P_0	P_1	Package	Shipping†
ESD7484	1.6 x 1.1 x 0.615	1.80 x 1.27 x 0.73	4 mm	4 mm	WLCSP10 (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

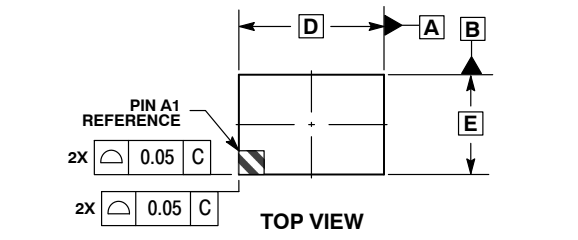
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

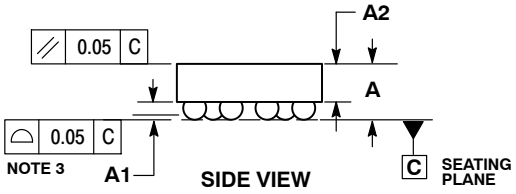
WLCSP10, 1.60x1.10
CASE 567DE−01
ISSUE O

SCALE 4:1

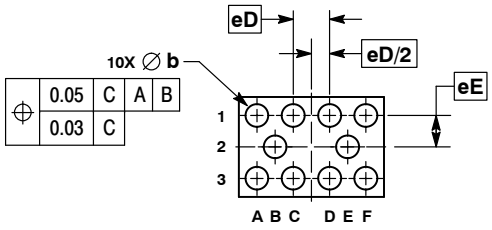
DATE 10 MAY 2011



TOP VIEW



SIDE VIEW

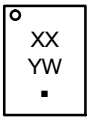


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.57	0.63
A1	0.17	0.24
A2	0.41 REF	
b	0.24	0.29
D	1.60 BSC	
E	1.10 BSC	
eD	0.400 BSC	
eE	0.347 BSC	

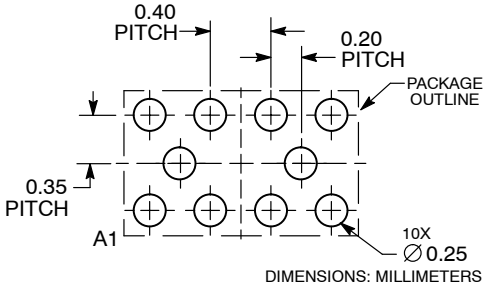
GENERIC MARKING DIAGRAM*



Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**WLCSP10, 1.60X1.10**	**PAGE 1 OF 1**

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